

Testbench Quality Assurance

Functional qualification solution

Overview

Synopsys Testbench Quality Assurance system is the only solution that objectively measures the overall effectiveness of your verification environment. It identifies verification weaknesses that allow bugs to go undetected and lead to functional problems, silicon re-spins, and delays to market. Testbench Quality Assurance system does this with unique automation technology that provides quick feedback on the most serious problems and supports the efficient analysis and correction of problems.

Gaining Confidence in Your Verification Environment

Synopsys Testbench Quality Assurance system provides detailed information on the ability of your verification environment to activate, propagate and detect “systematic faults” that represent potential bugs in your design, exposing significant weaknesses that have gone unnoticed by other tools. The system provides data to identify vulnerabilities in the stimuli, observability, checkers and assertions as well as holes in your verification plan. With the uncertainty removed, your verification efforts will be more reliable and efficient.

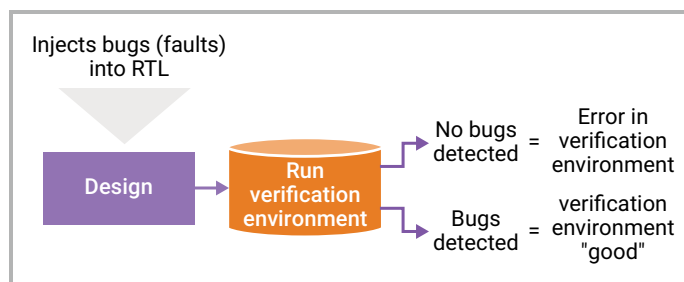


Figure 1: Synopsys Testbench Quality Assurance Functional Qualification Process

Satisfying ISO 26262 for Automotive

Synopsys Testbench Quality Assurance enables testbench qualification. This is needed for the evidence-based verification quality analysis for ISO 26262 Part 8-9 assessments (“Supporting Processes—Verification”).

Operational Modes

Synopsys Testbench Quality Assurance works in the following modes:

1. Verification improvement mode analyzes the verification of your design and identifies specific holes and weaknesses
2. Metric mode objectively measures the overall quality of your verification environment

Verification Improvement Mode

In this mode, Testbench Quality Assurance identifies weaknesses and holes caused by incomplete or missing checkers, assertions and test scenarios or problems in the verification infrastructure. It provides a complete report of the results in HTML format that highlights the problem areas. This mode is used to expose shortcomings and guide improvements in your environment to ensure that RTL bugs do not slip through the process.

Metric Mode

You can also use the system to objectively assess overall functional verification quality. The metric mode uses statistical sampling techniques to analyze the ability of your verification environment to activate, propagate, and detect potential bugs. The scores produced by the metric mode in these areas allow for:

- High-confidence IP exchange
- Better SoC predictability
- Optimized allocation of verification resources

Adopt Functional Qualification Early in the Process

Research has shown that certain faults are more likely than others to expose big weaknesses in the verification environment. Synopsys Testbench Quality Assurance uses a proprietary algorithm to automatically classify and prioritize the faults related to your RTL design. The faults are then injected and qualified in priority order. Subsequent qualifications inherit results from previous runs and focus on the remaining undetected faults. This process allows you to:

- Find and fix big weaknesses early in the verification process
- Expand the set of qualified faults as the environment and design mature
- Achieve incremental improvement over time
- Minimize analysis and debug effort

Broad Support for Languages, Tools and Techniques

Synopsys Testbench Quality Assurance supports the qualification of a range of design languages, including C and C++ for high-level modeling and software implementation, and SystemC, (System) Verilog and VHDL for modeling hardware. There are no restrictions on the test or verification environment.

Testbench Quality Assurance is tightly integrated with the most commonly-used commercial HDL simulators. In addition to Synopsys VCS® functional verification solution, Synopsys Testbench Quality Assurance supports Cadence® Xcelium and Siemens Questa® advanced simulator.

Synopsys Testbench Quality Assurance also supports the qualification of formal verification environments. The process and purpose are analogous to the simulation application. It modifies the RTL code to inject faults and, in this case, invokes the formal verification environment to prove a set of properties. If at least one of the properties fails, that implies that this particular fault can be detected by the existing environment. If the properties pass, then there is something to investigate—perhaps a missing property, an over-constrained situation, or some other problem. Simulation and formal verification qualification results can be merged into a single report to provide an overall measure of verification effectiveness from a combined static and dynamic perspective. Synopsys Testbench Quality Assurance supports Synopsys VC Formal™ verification solution as well as JasperGold® formal verification platform and OneSpin 360 DV™ platform.

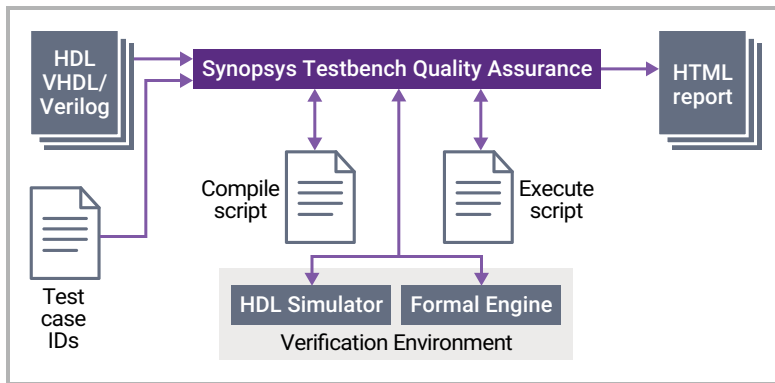


Figure 2: Synopsys Testbench Quality Assurance integrates easily with existing environments

Interoperability

Synopsys Testbench Quality Assurance is easy to insert into existing functional verification flows (Figure 2). It is fully compatible with all current verification methodologies, such as constrained-random stimulus generation and assertion-based approaches. Testbench Quality Assurance also leverages the Synopsys Verdi® debug solution to enable quick debug and analysis of results.

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com or contact your local sales representative.