

Synopsys Verdi Regression Debug Automation

AI-Driven Root-Cause Analysis

Overview

Simulation regressions are run countless times during a project. Every time that a regression fails, teams must often examine thousands of failures and debug their causes. Because the RTL and verification environment code is changing constantly as bugs are fixed and as new features are added and tested, regression failures are an everyday occurrence. Manually processing daily regression failures is a huge burden on engineering resources. Fortunately, artificial intelligence and machine learning technologies provide relief.

Faster Root Cause Analysis

The Synopsys Verdi® Regression Debug Automation (RDA) is an artificial intelligence (AI) driven verification technology for automating the process of finding the root causes of failures in the design under test and testbench. RDA addresses the challenges brought by manual and error-prone processes for dealing with regression failures by automatically classifying and probing raw regression failures through learned behavior leading to an increase of 2X or more faster root cause analysis (RCA) and debug.

The RDA capability inside of the Synopsys Verdi® Automated Debug System automatically classifies the failures into bins based on failure characteristics. Those failures are then automatically triaged to identify if they are part of the design or the testbench. Both design and verification teams perform root cause analysis to root out the causes of the failures within the specific bins.

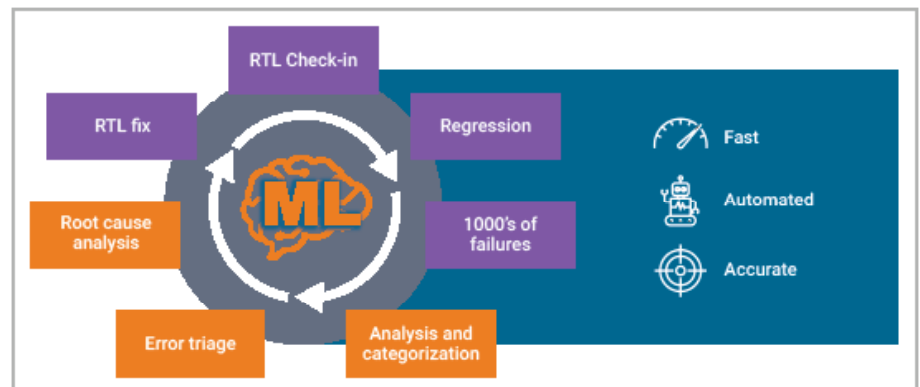


Figure 1: The RDA capability inside the Synopsys Verdi® Automated Debug System accelerates the debug process using artificial intelligence and machine learning technologies.

Key Components of RDA

Regression Debug Automation can be applied to several debug scenarios to save time and resources.

Regression Binning

Regression binning reduces redundant debug work by grouping related failures. These mined relationships are classified into buckets according to error types related to UVM-based messaging, user-defined rules, verification IP, and CPU-based design failures (instruction set errors).

The results are captured and placed into a results file that can be easily visualized and analyzed within Synopsys Verdi. SmartLog technology in Synopsys Verdi RDA can be used to view, filter, and search the results. Messages can be used to invoke interactive debug or other analysis. Regression binning is over 90% accurate and reduces overall triage time by further differentiating between testbench and design-under-test failures.

Debug Facilitator

The debug facilitator engine automatically captures and creates debug checkpoints during the simulation to establish a full state of the environment at the time of failure. The checkpoints are then utilized along with the RCA results to perform interactive and reverse debug in Synopsys Verdi RDA. This enables quick debug and analysis of the identified root cause(s) in the testbench.

Design Under Test Root Cause Analysis

Design under test root cause analysis (DUTRCA) filters out non-design-related bugs then utilizes time-based rollback mechanisms and TraceDiff technologies to automatically narrow down DUT problems. DUTRCA looks for UVM errors and identifies optimal starting points to conduct tracing. It then looks for comparisons between the waveforms to identify difference signal values for finding the root cause. Root cause analysis is automatically done to determine if the issues are related to the testbench or the DUT. DUTRCA provides a report of the results that can be opened in a separate view within Synopsys Verdi RDA for further debug and analysis.

X Root Cause Analysis

Xs are notoriously difficult to debug because they typically cover many cycles and levels of logic, and they result in many fanout cones of logic with a single root cause. X root cause analysis (XRCA) is technology that analyzes single and multiple paths to identify the root causes of x-related issues. If this results in multiple paths being sourced from a single root cause, those paths are grouped into a single group.

Because simulation is pessimistic, many Xs are considered false because of X-pessimism creating false X noise. To eliminate the reporting of false Xs, XRCA utilizes an algorithm to filter out false scenarios from real Xs. Both false and real Xs are reported but in separate sections so that all results can be viewed. Root cause analysis is only conducted on real Xs to increase analysis throughput.

Conclusion

Regression Debug Automation within the Synopsys Verdi system uses AI-driven verification technology to eliminate tedious and error-prone processes for debugging the thousands of failures reported during daily regression runs. This technology automatically bins, probes, and performs root cause analysis of failures accelerating debug by up to 10 times.

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