

# Simulation and Analysis Environment

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**Overview**

Synopsys' Simulation and Analysis Environment (SAE) is a comprehensive transistor-level simulation and analysis environment that is tightly integrated and included with Synopsys' HSPICE®, FineSim® and CustomSim™ circuit simulators. The netlist-based flow of SAE provides intuitive and comprehensive capabilities to efficiently set up and launch simulations, and analyze and explore simulation results to improve the productivity of analog verification.

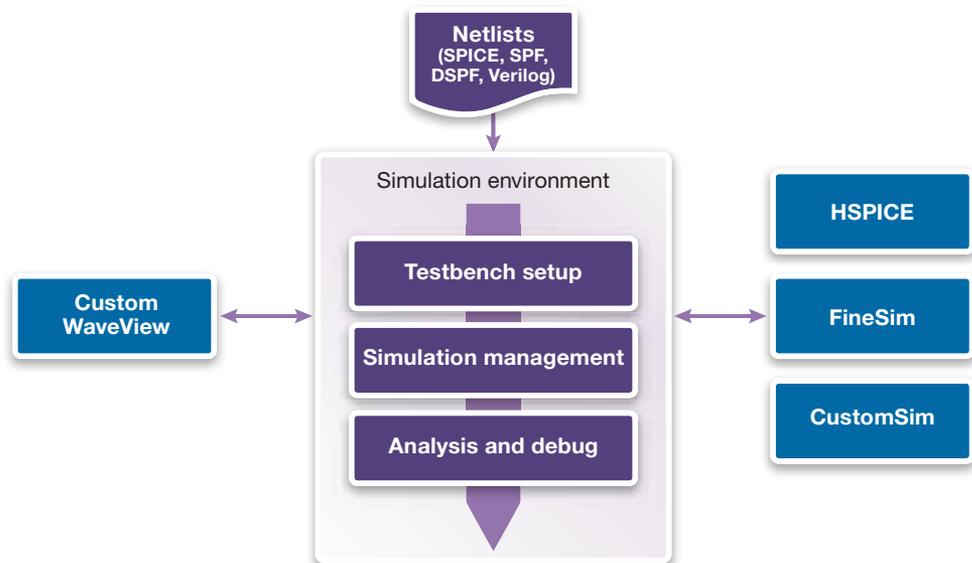


Figure 1. Simulation and Analysis Environment flow

**Key Capabilities**

- ▶ Netlist-based flow for direct import of SPICE, Verilog and DSPF
- ▶ Unified setup for corners, sweeps across multiple testbenches and Monte Carlo analysis
- ▶ Language-sensitive text editor for netlist-based navigation, cross-probing and syntax checking
- ▶ Automated regression capability with industry-standard TCL scripting language
- ▶ Advanced job distribution and monitoring for batch-mode simulations with remote grid support
- ▶ Single common testbench usage for both pre- and post-parasitic phases of design verification
- ▶ Includes Library Manager and Hierarchy Editor capabilities for Multi-user and mixed-signal verification support

- ▶ Integration with Synopsys' Custom WaveView™ graphical waveform viewer for extensive post-processing of waveforms
- ▶ Advanced visual data navigation and data mining features, such as charting, statistical analysis, histograms and scatterplots
- ▶ Detailed report generation, including web-based HTML documentation

## SAE Main Console

The main console of SAE (see Figure 2) provides designers with a high-altitude view of the current design's variables, analyses and outputs and allows them to focus on the design, not on the details of simulator syntax. Features that increase designer productivity include an “edit-in-place” capability allowing users to work directly with the values in the main console. Specific dialogs can also be used for setup and detailed control of the entries in the console.

The analyses section of the main console shows the various simulations that will be conducted. The environment helps a designer be more productive by hiding the details of simulation syntax in favor of easy-to-use, simulator-specific dialogs.

Another key part of the environment is the outputs section, which collects and manages the volumes of data that can be produced by complex analog/mixed-signal (AMS) simulations. Each line in the outputs section is a measurement that can be chosen from a schematic or text view cross-probe or constructed with the Results Analyzer or Calculator. After simulation, scalar data results will be automatically displayed in the table while vector data will automatically be displayed in the optional Custom WaveView viewer where they can be subjected to further analysis.

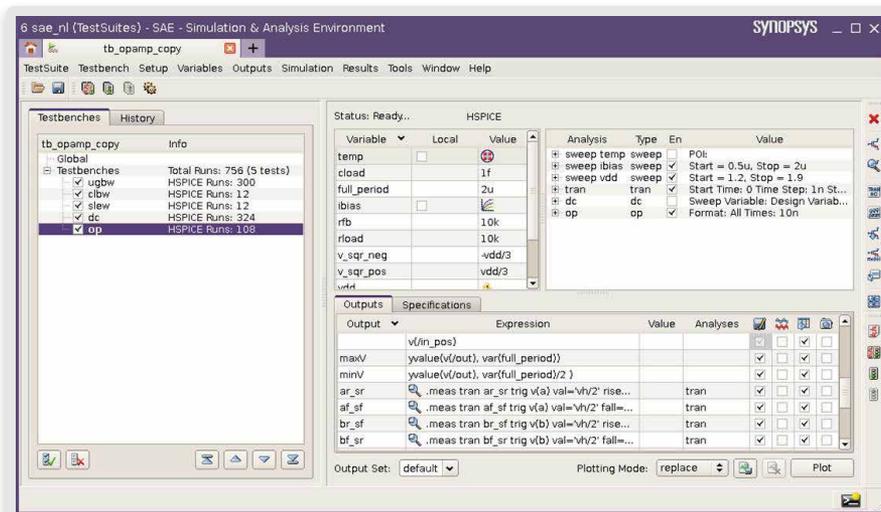


Figure 2. SAE main console

## Unique Netlist-based Flow

One of the unique features of the SAE is the netlist-based flow for direct import of SPICE, Verilog and DSPF netlists. This capability enables faster simulation setup and enables verification of pure text-based circuit testbenches in a GUI environment.

When a netlist is imported into SAE, the imported netlist text populates the various sections in the SAE GUI (see Figure 3). All portions of the netlist, such as parameters, probes, analysis and outputs, get automatically populated and the environment is ready for simulation without any additional setup steps required. A cell-based view selector (equivalent of hierarchy editor) is also included for mixed-signal verification.

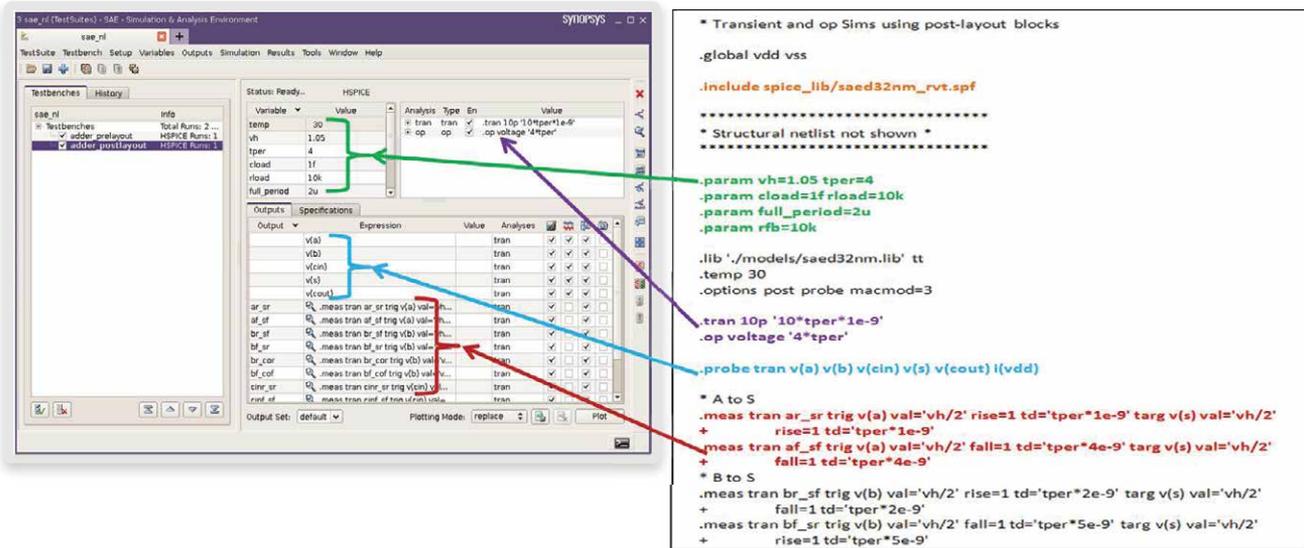


Figure 3. Netlist-based flow example

## Intuitive Simulation Setup

SAE provides a streamlined simulation setup with its intuitive, easy-to-use environment. It is trivial to import netlists of the same or different formats for creation of single or multiple tests. The re-import feature and incremental saving/loading of setup enables quick reuse of the existing simulation setup. Direct support for HSPICE **.measure** statements and additional assistance through Measurement Assist GUI in Calculator helps designers create complex expressions and apply them to ideal or extracted designs without change. When possible, simulator settings are retained when switching simulators, thereby allowing designers to perform a variety of simulations on the same testbench.

The SAE interface is developed using Tcl scripting language, which makes it easily customizable to a design team's requirements. An imported netlist or an interactively created SAE session can also be converted to a Tcl-based regression script, which can then be run in batch mode to save time on interactive runs and improve throughput. A powerful language-sensitive text editor offers several unique features, such as hierarchy traversal from text to schematic and vice-versa, back-annotation to text views and output probing from text view. The text editor supports multiple languages, such as Verilog, SystemVerilog and SPICE, and provides a syntax-checking feature for all supported languages. This feature helps designers quickly write and simulate text views for mixed-signal verification.

## Scalable Regression Environment

SAE is built for large-scale multi-dimensional verification with multi-testbench support across different designs, analysis and simulators. The multi-testbench interface (shown in Figure 2) is easy to use and more intuitive than existing solutions. Previous run histories are available in multi-testbench mode, making it easier to perform multiple runs with design parameter changes and compare results for target design specifications.

The environment provides a unified mechanism for parametric sweeps, corners and Monte Carlo analyses that simplify the setup, launch and recovery of the thousands of individual simulations required to understand the behavior of a design. Displayed in the analyses section of the main console, the Parametric Analyses dialog adds nested sweep commands as needed and supports both native and data-driven sweeps.

The Corners dialog allows the user to set up sets of parameter values and model libraries and organize them into distinct sections prior to simulation. The Corners tool can launch, recover and summarize the results of simulations for a thorough understanding of the effect of process corners, temperatures or other variables in the design.

The Monte Carlo capability helps reduce the volume of simulations by providing statistical analyses across process variability. The Monte Carlo capability is also tightly integrated with HSPICE's variability analysis capability to maximize throughput and improve accuracy.

SAE is designed to take maximized advantage of compute farm resources and simulator licenses. Shipped with native support for Platform Computing™ LSF and Sun Microsystems® Sun Grid Engine grid management products, SAE also supports remote grid job distribution for optimal use of compute resources. The hierarchical job monitor allows users to instantly track progress for any number of runs and configurations. Seamless integration with remote job management provides visibility of run status with visual indication and error text view for failed runs for quick detection of failure (see Figure 3). Additionally, SAE provides an open application programming interface (API), allowing easy integration of proprietary grid management software.

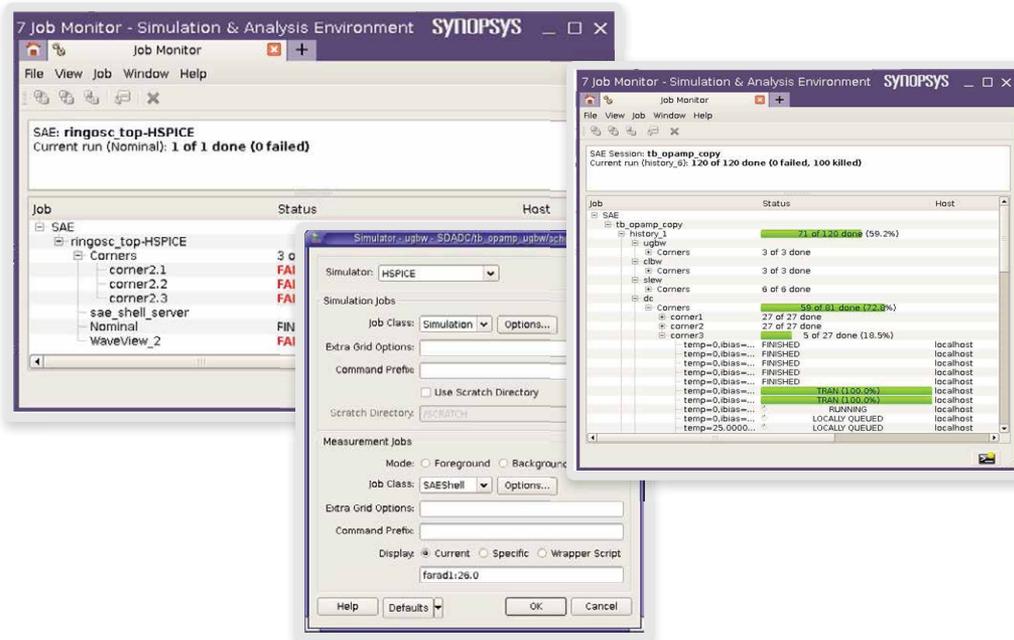


Figure 4. Hierarchical job monitor with job distribution setup dialog

## Superior Debugging Capabilities

Following a simulation, scalar results are displayed in the Results Viewer and vector results are displayed in the optional Custom WaveView waveform viewer. Results viewer provides a summarized list of output results across all testbenches as well as detailed results for individual testbenches. There are also visual indicators for measures that pass, fail or fall within the specified margin (see Figure 5).

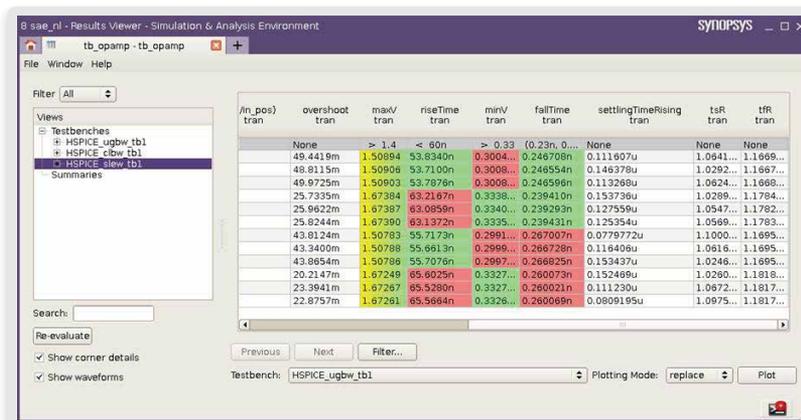


Figure 5. Results viewer with results summary and detailed results for all testbenches

Advanced visual data navigation with several charts utilities helps make data mining and debugging of multi-dimensional verification much faster. Depending on the type of analysis performed, results can be displayed in scatter plots, histograms or multi-axis charts with additional tabulated statistical results for Monte Carlo analysis (see Figure 6). Any point identified as a problem on a chart can be cross-probed and displayed in the results browser and variables assistant for further investigation of the failed point. These unique features significantly improve productivity when running thousands of simulations and sorting through massive amounts of simulation data.

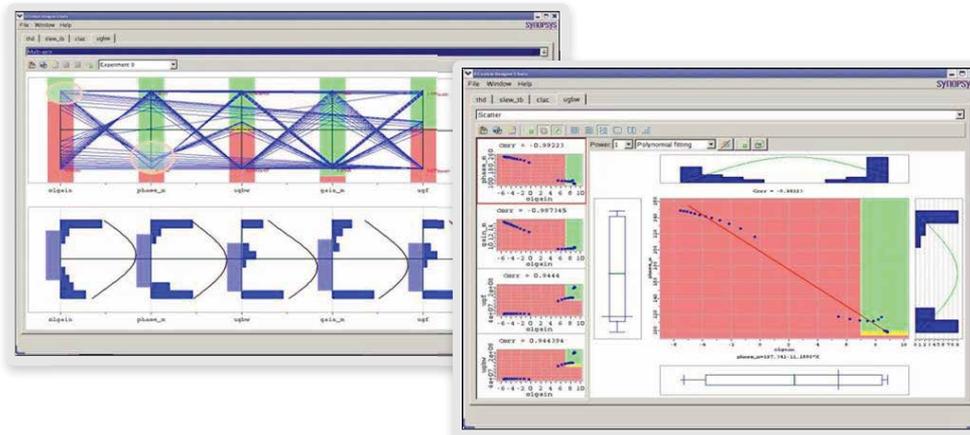


Figure 6. Data mining with multi-axis charts and scatter plots

Once all the simulation and verification is complete, designers can write out a web-based HTML report capturing the complete simulation setup, specifications and results including variables/corners setup for all testbenches and saved waveform images (see Figure 7). Reporting features a hyperlinked table of contents for quick access and a summary section for quick review.

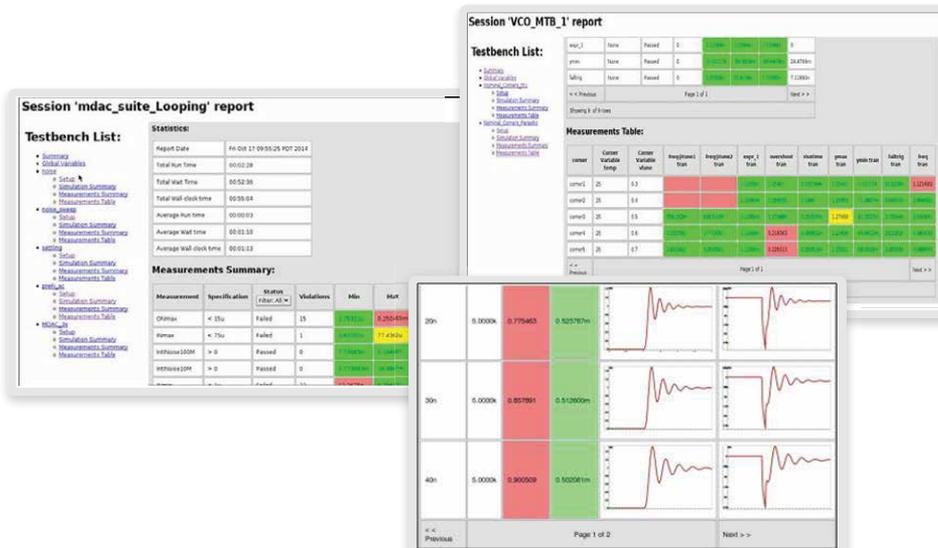


Figure 7. HTML report with testbench setup, results and waveform images

## Platform Support

- ▶ X86 for 32- and 64-bit
- ▶ Red Hat Enterprise Linux version 4 and 5 (AS, ES, WS)
- ▶ SUSE Linux 10 and 11 (AS, ES, WS)