

# CustomSim

## High-performance, high-capacity FastSPICE simulation

## Overview

The CustomSim™ FastSPICE simulator delivers superior verification performance and capacity for all classes of design, including custom digital, memory and analog/mixed-signal circuits. The comprehensive offering includes advanced analysis options for native circuit checking, power, signal and MOS reliability analysis and mixed-signal simulation. CustomSim, in combination with the CustomExplorer™ Ultra advanced regression and analysis environment, provides a complete mixed-signal verification solution that boosts productivity.

Designer productivity is negatively impacted by the overwhelming number of simulations that need to be run. Not only is the number of simulations increasing, but the size of circuits, combined with extracted post-layout parasitic, is far exceeding the capacity of traditional simulation solutions. Synopsys' CustomSim FastSPICE simulator is built on best-in-class technologies that deliver increased productivity and designer confidence to address today's AMS verification challenges.

## Increased Productivity

- Designers can use a single simulator for verifying all design types and performing advanced post-layout analysis
- Highest-performance, highest-capacity, SPICE-accurate solution allows designers to run more simulations, faster
- Native design rule checking avoids wasted simulation time by flagging rule violations when they occur
- Runs simulations not previously possible, for example, full-chip post-layout functional verification with CustomSim and VCS® mixed-signal simulation
- Reuse testbenches and measurements from pre-layout simulations for post-layout verification with back-annotation
- Simplifies usability through a common set of inputs, outputs and device models integrated into the CustomExplorer Ultra verification environment

Circuit Types	MOS Count	CustomSim	Other Simulator	Speed-up
Full-chip USB interface	13.2M	9.9 hours	48 hours	4.8X
Serial SRAM	13.4M	1.5 hours	4.5 hours	3X
Post-layout clock mesh	11.6M	10.5 hours	>2 days	>4X

Table 1: CustomSim simulates large designs in hours instead of days

## Increased Confidence

- Built on a common set of HSPICE™ device models endorsed as the gold standard by foundries worldwide
- Native design rule checking finds errors that previously could not be detected by simulation or required long transient simulations
- Accurately verifies that power and signal nets comply to stringent nanometer electromigration rules
- Analyzes power nets for excess IR-drop
- Determines device lifetime limitations before tapeout by running full-chip MOS reliability analysis

## Next-generation Circuit Simulation Technology

CustomSim's breakthrough patented technologies deliver superior performance and capacity while maintaining SPICE accuracy. Built-in simulation intelligence enables CustomSim to automatically recognize devices, topologies and hierarchies and employ the most efficient techniques to accurately simulate any design type. True multi-rate engine technology with intelligent partitioning allows CustomSim to quickly react to changes in circuit behavior, thereby delivering the highest performance simulation time with SPICE accuracy. Revolutionary techniques for array and RC optimization ensure that accuracy is retained while delivering the highest-capacity circuit simulation solution. A compiled Verilog-A solver ensures high-speed execution of complex analog behavioral models.

## Golden HSPICE Device Models

CustomSim is built on top of a common HSPICE device model library, guaranteeing device model correlation between CustomSim and HSPICE. The common HSPICE device model library simplifies foundry support by using a single golden library for advanced device model updates. CustomSim supports advanced nanometer foundry models developed with the HSPICE customizable C-model interface.

## Native Circuit Checking

Designer productivity is negatively impacted by manually having to verify that electrical design rules are not violated. CustomSim provides a comprehensive set of static and dynamic native circuit checks to rapidly identify electrical rule violations and power management failures. With this technology, designers can easily identify violations such as missing level-shifters, incorrect VDD hook-up, floating gates, excess leakage paths and excursions from the device safe operating area, to name a few. CustomSim supports a rich set of diagnostic commands that enable extensive power and timing analysis.

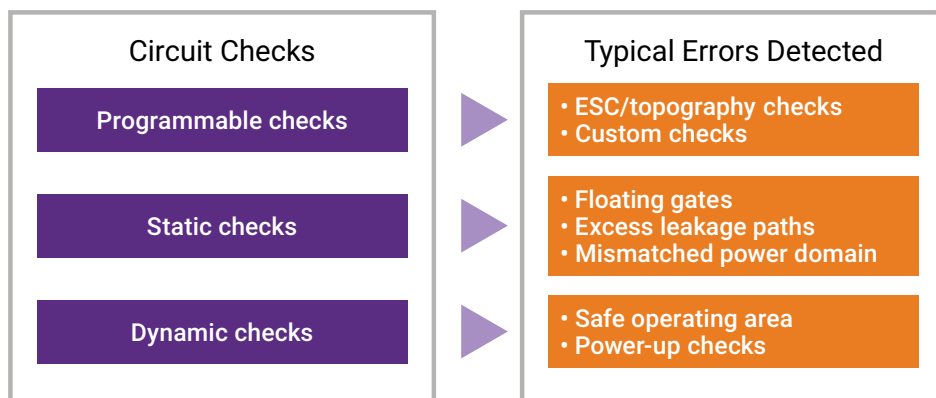


Figure 1: CustomSim native circuit checks enable ERC and low power verification

## Static Power and Signal Net Resistance Check

Utilizing CustomSim's high-capacity engine, designers can run a full-chip static analysis of all power and signal nets to identify any high-resistance paths for power and signal nets and uncover any errors in power bus network design and signal net routing.

## Power Net Reliability Analysis

CustomSim employs a unique coupled flow for EM/IR-drop analysis. Taking advantage of the superior capacity, it is possible to run detailed current simulations of blocks, including post-layout parasitic data in the power network and core circuitry. This then delivers high-accuracy EM/IR-drop analysis and avoids wasted area and power through overdesign. The solution fully supports nanometer length-dependent rules. Custom Compiler™ provides an extensive reliability analysis visualization environment allowing designers to debug reliability issues within the layout environment.

## Signal Net Reliability Analysis

Shrinking geometries have dictated the need for EM/IR-drop analysis of signal nets. CustomSim utilizes dynamic current density analysis for this purpose. Bidirectional current flow is correctly considered, including calculation of the RMS currents required for monitoring Joule heating within the design. Custom Compiler provides an extensive reliability analysis visualization environment that allows designers to debug reliability issues within the layout environment.

## MOS Reliability Analysis

Fragile nanometer transistors are stressed by high field strengths in the device channel due to high temperature and high-frequency switching activity over extended periods of time. These stress effects lead to device ‘aging’, resulting in performance degradation and designs that fail to meet specification during their expected operating life.

CustomSim allows users to add aging effects to industry-standard BSIM3 and BSIM4 models. In addition to the built-in HCI reliability model equation, CustomSim provides a user reliability interface (URI) that permits users to define custom equations for modeling HCI and other stress effects, such as negative-bias temperature instability (NBTI) in PMOS devices. CustomSim enables users to measure performance degradation over time by comparing the results of pre-stress and post-stress simulation results.

## Mixed-signal Simulation

CustomSim is tightly integrated to Synopsys’ VCS digital simulator through a direct-kernel integration. This mixed-signal solution delivers the highest throughput by breaking through the analog performance bottleneck with the highest-performance, SPICE-accurate circuit simulation technology. A flexible usage model allows for any mixture of abstraction level and design hierarchy with full language support for Verilog, VHDL, Verilog-AMS and SPICE. Post-layout data is supported through DSPF, SPF and SDF formats.

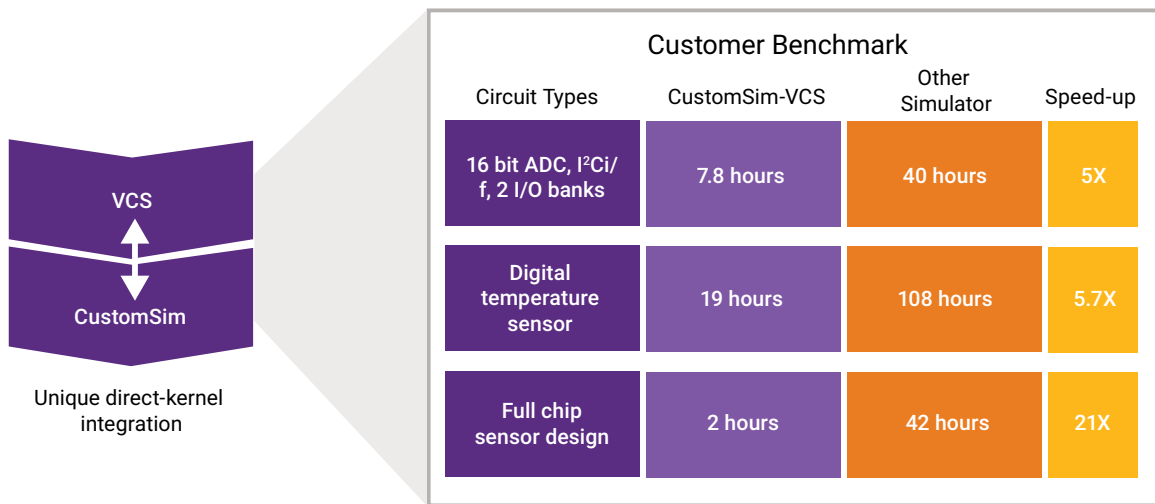


Figure 2: Throughput improvements using CustomSim mixed-signal simulation

CustomSim with VCS is integrated with Synopsys’ CustomExplorer Ultra advanced regression and analysis environment to streamline mixed-signal verification and boost productivity. CustomSim supports third-party digital simulators through an industry standard VPI integration.

## Inputs Supported

- HSPICE, Spectre and Eldo
- Common HSPICE device models
- Spectre and Eldo models
- Verilog-A analog behavioral modeling
- SPF, DPF and SPEF for post-layout parasitic data
- VCD and VEC stimulus input formats
- TCL scripting

## Outputs Supported

- WDF, WDB, FSDB and many more waveform database formats

## Platforms Supported

- RedHat RHEL 6.6, 32- and 64-bit
- SUSE SLES 12, 32- and 64-bit

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