SYNOPSYS®
Predictable Success

Automotive Electronics Reliability Flow
Improving Electronics Quality for Automotive Systems

Overview

Today's automobiles and trucks include more electronics features and functions than at any time in history. While many of these are necessary for increased comfort, convenience, and safety, they must also be designed vs. stringent quality requirements. Designers must manage a number of key problems including:

‣ *Increasingly complex HW/SW design complexity*
‣ *Harsh operating conditions*
‣ *Increasingly demanding market needs*

Synopsys offers leading products for the implementation, system-level validation, and verification of high reliability systems, subsystems, and ICs.

Complexity vs. Reliability vs. Cost

The automobile has evolved from merely a vehicle for simple transport to a rolling electro-mechanical laboratory, filled with sophisticated electronics that must work in concert with complex mechanical components. These electronics serve to increase the levels of comfort, performance, and safety of vehicles, making them more attractive and practical for today's consumer.

However, it is necessary to balance this with the realities of the automotive world. No matter how "whiz-bang" the features of a new design promise to be, they must "just work" despite the internal complexities and harsh external conditions. Excessive recalls and warranty-related work can easily sap profits from OEMS and their supply chain partners alike.

On the other hand, and perhaps surprisingly, over-design of components and systems can lead to problems, as well. If the massive number of vehicle sub-components is designed with excessive performance margins, the final product can be too expensive to manufacture.
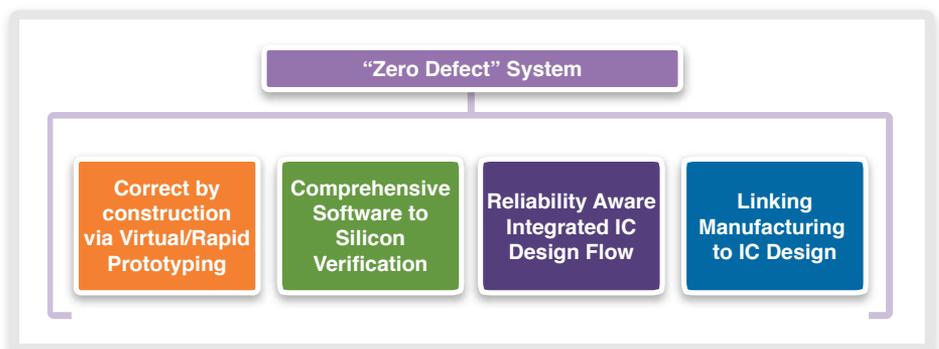

"Zero Defect" System

| Correct by construction via Virtual/Rapid Prototyping | Comprehensive Software to Silicon Verification | Reliability Aware Integrated IC Design Flow | Linking Manufacturing to IC Design |

Figure 1: Synopsys Automotive Flow supports Zero Defect Design

Building Reliability from Idea to Implementation

In order to address the triple threat of features, cost and reliability, a broad based view of incorporating reliability into all phases of design offers the best path to successful implementation and manufacture of automotive electronics. Whether it is called "Six Sigma Design" or "Zero-defect" design, Synopsys has a wide range of technology to help engineers implement software, design and manufacture ICs, and optimize system performance to meet the challenging demands of the automotive industry.

The Synopsys Automotive Electronics Flow

Key Areas for Improving Reliability

Synopsys offers widely adopted solutions that address the four key elements of designing and building highly reliable automotive electronics.

- Virtual and FPGA-based Prototyping To Ensure 'Correct By Construction' Systems
- Comprehensive Software-to-Silicon Verification
- Reliability –Aware IC Design
- Linking Manufacturing To Design

Each of these addresses the significant IC, component and system-level issues that can lead to degraded end product reliability.

Correct by Construction via Rapid Prototyping

At the outset, any complex design must be formulated, prototyped, analyzed and verified at the system level. This design, analysis and debug must take into account several important considerations:

- Hardware/Software Complexity: Because of the immense (and growing) amount of code needed to run today's automobiles, reliability is gained by ensuring that the software and hardware mesh seamlessly.

- Tolerance Stackup: Even if individual components are designed and manufactured to meet their unique tolerance profiles, they may still fail when assembled in a subsystem. If too many components are at the outer edge of their tolerances, component interactions may be compromised, leading to system failure. On the other hand, overdesigning to ensure reliability can increase costs and time to market.

- Mechatronic Interactions: Today's automobile depends on complex interactions across a wide variety of subsystems: electrical, mechanical, hydraulic, software, etc. Designers must create virtual prototypes of the system, including the wire harness, to reduce the number of design iterations and hardware prototypes.

- Harsh Operating Environment: Automotive systems must be able to function under difficult operating conditions: extremes in temperature, humidity and vibration, as well as the unique operating behavior of a wide range of drivers.

As a result of years of customer interaction, and research and development, Synopsys has developed and assembled the tools and flows to handle the challenges of correct-by-construction system design.

Hardware Software Complexity

To enable engineers to handle the challenges of hardware/software complexity, Synopsys enables early software development and more productive test with the Virtualizer™ tool set, and Synplify® tool and HAPS® systems for FPGA and ASIC prototyping.

Synopsys' Virtualizer provides an integrated SystemC development environment for assembling virtual prototypes using transaction-level models (TLMs) developed by Synopsys and obtained from third party sources.

Virtualizer improves overall design productivity by enabling concurrent hardware and software development through virtual prototypes.

Synopsys' System Studio is a high performance, model-based algorithm design and analysis tool, which combines unmatched simulation performance with high modeling efficiency plus the industry's best integration into the chip implementation design and verification flows.

The Synplify Pro FPGA synthesis software is the industry standard for producing high-performing, cost-effective FPGA designs. It performs optimization at a high level, and can synthesize RTL into popular FPGA devices. It provides superior optimization across the FPGA, optimal performance, and support of very large designs.

The Synopsys FPGA-Based Prototyping Solution offers a complete suite of tightly integrated, easy to use products for FPGA-based prototyping, including HAPS systems and boards, interface and memory boards, and implementation and debug software. The HAPS systems dramatically accelerate functional verification of ASIC, ASSP and SoC designs and is ideal for design and verification teams who leverage FPGA-based prototypes to improve their time to market and avoid costly device re-spins.

Tolerance Stackup

Synopsys' Saber® Simulator is ideal for analyzing interactions and tolerance stackup in mixed-signal, mixed-domain Mechatronic systems and power electronics. Saber's highly acclaimed modeling, simulation tools give designers the capabilities to simulate, analyze and verify interactions between multiple physical domains (electrical, magnetic, mechanical, thermal, hydraulic, etc.). Saber's statistical analysis capabilities predict how

component tolerance variations affect system performance. With its advanced analysis and modeling capabilities – waveform analyzer, comprehensive model libraries, and multi-language model creation tools – designers can perform optimization on virtual prototypes of any system.

System Interactions and Harsh Operating Environment

Saber also enables comprehensive system design and verification using parametric, sensitivity, stress, and worst case analyses. Parametric analysis fine-tunes key parameters in a design. Sensitivity analysis determines which parameters most affect system performance, while stress analysis evaluates the degree and effects of component stress in a system during operation.

Comprehensive Software-to-Silicon Verification

After system-level design and analysis, the next step toward achieving maximum performance and reliability involves comprehensive software-to-silicon verification. To ensure success in this phase of automotive design development, the engineers must take three important factors into account:

▶ Mechatronic Interactions:
At this verification stage, unexpected component and system behavior must be analyzed in a real-life operating environment. Verification must also account for multi-domain system behavior, using a comprehensive model library.

▶ Maximum Functional Coverage:
The verification environment must also account for functional failure due to unanticipated operating modes. It must follow a methodology that achieves maximum coverage and allows visibility into the verification process.

▶ Component Aging and Analog/Mixed-Signal (AMS) Verification:
A comprehensive verification flow must also consider IC failures over time, especially in the harsh automotive environment. AMS verification must span the block, chip and board levels, with jitter, noise and signal integrity analysis. This stage of verification should also encompass electromigration, power grid and IR drop issues.

System Interactions

To model, analyze and verify mechatronic interactions, Synopsys' Saber enables multiple analyses across multiple domains. It also allows engineers to optimize for harsh operating environments, accounting for temperature and EMC/EMI. Saber accelerates the work flow by providing the industry's largest single-source model library with 30,000+ parts spanning multiple engineering domains.

Maximum Functional Coverage

To ensure system reliability, functional verification must offer maximum test coverage with high visibility into the verification environment. Synopsys' VCS® simulator enables both directed and constrained random tests with a scoreboard of overall verification progress. VCS' unified coverage reports present a clear map of assertion, design and testbench coverage.

Component Aging and AMS Verification

To fully simulate and analyze component aging and AMS effects at the block, IC and PCB levels, Synopsys offers its HSPICE® and FastSPICE solutions. HSPICE is the industry's "gold standard" for accurate circuit simulation and offers foundry-certified MOS device models with state-of-the-art simulation and analysis algorithms. With over 25 years of successful tapeouts, HSPICE

simulates analog designs, RF design, custom digital design, standard cell design, memory design and characterization. It also features silicon-to-package-to-board-to-backplane analysis and simulation.

Synopsys CustomSim simulator provides fast and accurate transistor-level analysis with full chip capacity. Its capabilities include prediction of component aging, parasitics, and temperature effects as well as post-layout power grid, voltage and EM analyses.

Reliability Aware IC Implementation

The Implementation flow for automotive IC requires a high degree of attention to three major sources of potential failures:

▶ Electromigration (EM):
In the close confines of an automobile, tight wire harnesses, IC proximity, and dense PCB layout and routing can cause a range of electromigration challenges. Identifying and fixing voltage-drop and electromigration issues must be done early in the flow, to avoid costly iterations later.

▶ Electrostatic Discharge (ESD):
ESD is a major threat for IC reliability. Accurate device simulation can identify and investigate ESD-relevant effects and the internal behavior of the device under ESD stress conditions, which are not generally accessible by measurement. In particular, ESD analysis can be successfully used to study 3D effects arising from device layout.

▶ Poor Signal Integrity:
On-chip Signal integrity issues, such as excessive noise or crosstalk, can result in low yield and sub-optimal functionality in the field. This can result in costly recalls, warranty returns, and lost revenue.

Electromigration

Synopsys' PrimeRail uses embedded analysis and repair guidance technology to enable designers to easily perform power network verification throughout physical implementation. By identifying and fixing voltage-drop and electromigration issues early in the flow, designers can eliminate costly iterations late in the design process.

ESD and Signal Integrity

In order to address ESD and signal integrity issues, Synopsys' Galaxy™ Implementation Platform offers an array of powerful design and implementation tools. The IC Compiler, Hercules™, StarRC, TetraMAX® ATPG, PrimeTime® and PrimeRail solutions, enable engineers to take an IC design through to completion with high performance, quality and reliability.

A key component of the Synopsys' Galaxy platform is IC Compiler, the powerful IC synthesis and implementation solution. Its Zroute technology incorporates state-of-the-art routing features, such as native support of soft rules, multiple via insertion and wire spreading/widening, to enable litho-friendly routing and avoid manufacturing problems. By simultaneously considering the impact of manufacturing rules, as well as timing and other design goals, Zroute delivers high QoR and improved manufacturability.

Taken together, the wide range of tools and technologies integrated into the Galaxy Implementation System flow enables engineers to overcome the unique challenges in automotive IC implementation.

Linking Manufacturing to Design

Though design for manufacturing (DFM) is a concern for almost all electronic products and components, it's especially critical in automotive applications. Not taking manufacturing into consideration from the outset of a design will result in low yield, increased manufacturing costs and lost revenue.

The three major components of DFM for automotive applications are:

▸ Device level effects: Electrostatic effects upon transistors and interconnect are a major consideration in increasing the reliability of automotive IC designs.

▸ Interconnect modeling: On-chip Interconnect stress, exacerbated by the thermal and electromagnetic environment common in a motor vehicle, can pose a significant threat to the long term reliability of automotive IC and systems.

▸ Weak manufacturing-to-design link: Incomplete device models and the lack of a cohesive DFM flow can result in degraded medium- to long-term IC reliability and low yield, both of which can cause severe consequences.

Device Level Effects

These effects can include ESD, aging effects and self heating. Device simulation tools explore the electrical characteristics of semiconductor devices, as a response to external electrical, thermal or other boundary conditions imposed on the structure. The input device structure typically comes from process simulation steps using tools like Synopsys' Sentaurus™ Process or Taurus TSUPREM-4™, or through process emulation with tools like Sentaurus Structure Editor.

Interconnect Modeling

Raphael™, Synopsys' 2D and 3D RLC extraction tool, pinpoints potentially harmful on-chip parasitic elements. As a reference field solver, Raphael provides the most accurate parasitic models in the industry, and can analyze complex on-chip interconnect structures and the influence of process variations. It also generates accurate capacitance rules for layout parameter extraction (LPE) tools and can create 3D structures from GDS-II and technology files.

Manufacturing-to-Design Link

To address manufacturing yield issues caused by poor communication with design parameters, Synopsys' Yield Explorer brings yield relevant data from diverse sources such as the physical design flow, wafer manufacturing, and wafer and chip level testing into a single data bank. With the widest possible range of data at their disposal, engineers can achieve unsurpassed clarity in root cause analysis when faced with systematic yield limiters. Yield Explorer achieves this with an order of magnitude advantage in analysis speed in the most complex designs.

A Proven DFM Flow

Synopsys TCAD/DFM solution is used by 19 of 20 of the top semiconductor companies worldwide. The solution is supported by a strong R&D program, and provides faster time to yield, better quality of results and lowered risk as the design goes from inception to manufacture.
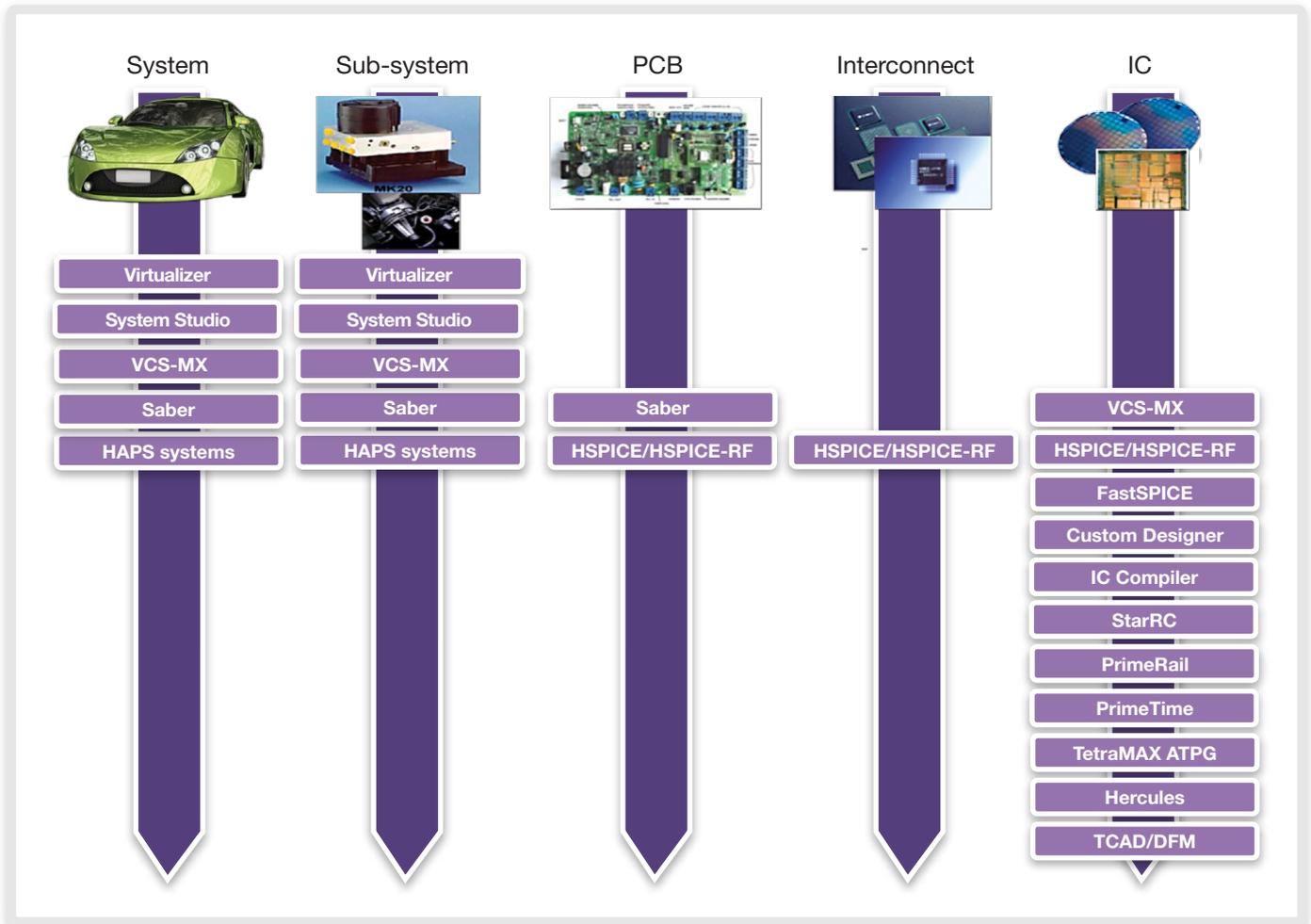
System	Sub-system	PCB	Interconnect	IC
Virtualizer	Virtualizer			
System Studio	System Studio			
VCS-MX	VCS-MX			VCS-MX
Saber	Saber	Saber		HSPICE/HSPICE-RF
HAPS systems	HAPS systems	HSPICE/HSPICE-RF	HSPICE/HSPICE-RF	FastSPICE
				Custom Designer
				IC Compiler
				StarRC
				PrimeRail
				PrimeTime
				TetraMAX ATPG
				Hercules
				TCAD/DFM

Figure 2: Synopsys Portfolio for Automotive Electronics Reliability

The Most Complete Solution for Complex Automotive Design

No longer a simple machine to get passengers from destination to destination, the modern automobile brings together an almost unimaginable collection of mechanical components, electronic control systems, wiring harnesses interfaces and software. For this complex machine to function properly, all components must work seamlessly to produce a reliable, cost-effective drivetrain coupled with other elements for safety, comfort and efficiency. The challenge lies in building, analyzing, debugging and manufacturing these separate components, so that when they are assembled and shipped, a reliable vehicle is ready for the road.

Synopsys' broad range of design, verification, implementation and manufacturing solutions is the culmination of years of design success. A proven, seamless flow allows automotive engineers to concentrate on innovative design and value added features, with the assurance that Synopsys' advanced technology can help the them solve their toughest design challenges and ensure predictable success.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.