A Quick Guide to Synopsys University Program Resources

Courseware, SolvNetPlus & Synopsys Learning Center

University Program, Synopsys Taiwan

June 2022

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Contents

- Membership Benefit
- Teaching Resources
  - courseware, generic libraries, PDKs
- Knowledge Base
  - SolvNetPlus
  - Synopsys Learning Center

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Membership Benefits

Teaching Resources 教學資源

IC Design and EDA Curriculum:

- Full Semester Courses – ***80+ courses*** for Bachelor and Master programs
- Workshops/Lectures - ***30 courses***
- Short Lectures/Labs - ***28 courses***

Teaching Support:

- ***32/28nm*** & ***90nm*** Generic Libraries and iPDK's
- Generic Memory Compiler

Knowledge Base 知識庫

Access Synopsys knowledge base:

- **Document –** contains product release note, installation guide, user guide & reference manual
- **Search –** provides an advanced search engine to retrieve information from various sources, such as documentation, articles, training, and so on.
- **Training –** Access ***Synopsys Learning Center*** for free self-paced training resources. The approved academic users are entitled to the **"Elite"** subscription model. Find more details here.

*Requires SolvNetPlus account to access above-mentioned resources.

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Teaching Resources

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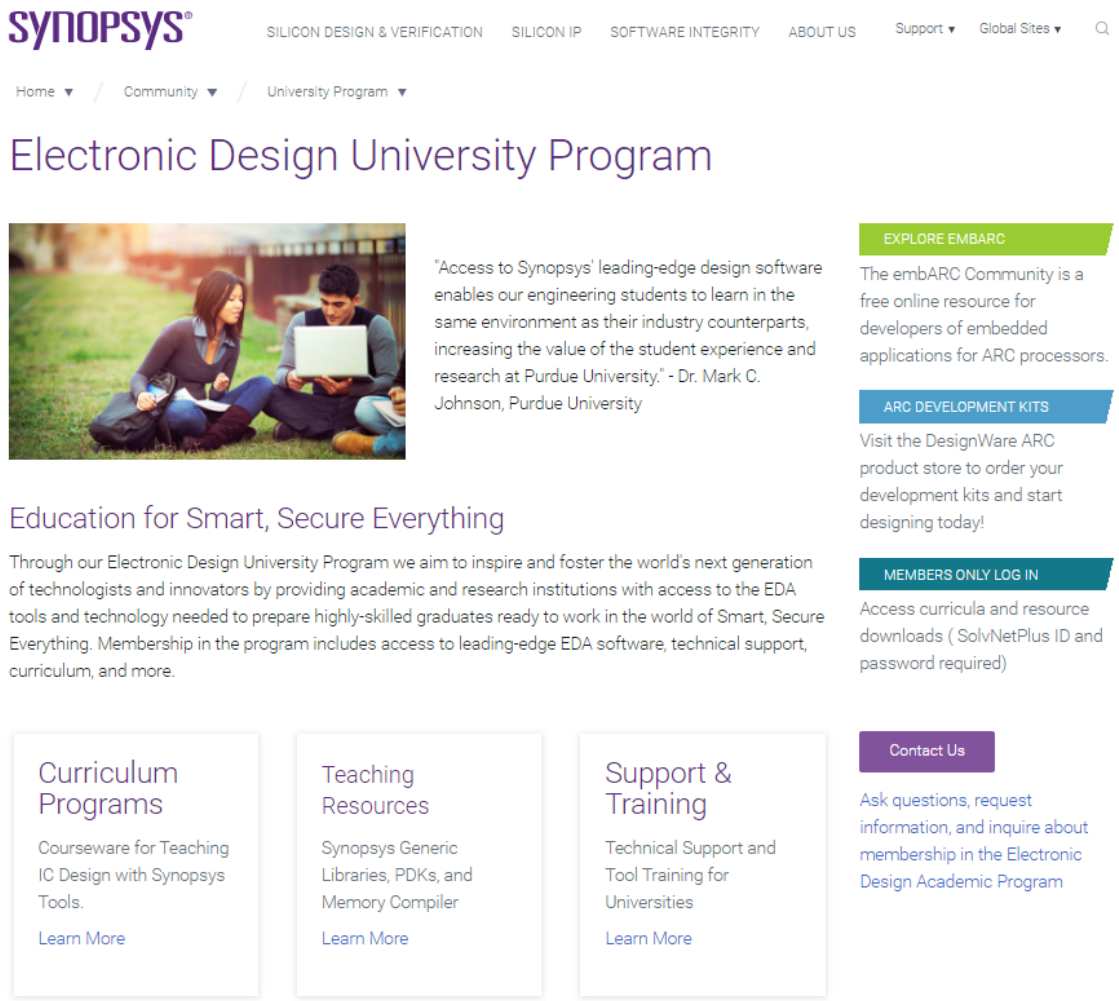
☞ Access through:
www.synopsys.com/community/university-program.html



Teaching Resources

IC Design and EDA Curriculum

IC Design Courses

Bachelor

- Analog and Mixed-Signal IC Physical Design
- Analog Integrated Circuits
- Computer Architecture and Engineering
- Digital Integrated Circuits
- IC Design Flow
- IC Design Introduction
- IC Testing
- IC Synthesis and Optimization
- Introduction to Microelectronic Circuits
- IC Synthesis and Optimization
- Introduction to Semiconductor Devices
- Linear Algebra
- Logic Design
- Microprocessor Systems
- Numerical Methods
- Scripting Languages for Beginners
- Static Timing Analysis
- Synthesis and Optimization of Digital Integrated Circuits
- Technical Writing

Master

- Analog Modeling with Verilog-A
- ARC Processor-Based Embedded Programming
- Complex Functions
- Crosstalk and Noise
- Design for Test
- Design of Embedded Systems
- Design of Special I/O's
- Digital Signal Processing
- EDA Tools
- FPGA Prototyping
- IC Design for Thermal Issues
- IO Design
- Low Power Design
- Low Power Design with Synopsys 32/28nm Generic Library
- Mixed-Signal IC Design
- Modeling and Optimization of IC Interconnects
- Rad-hard IC Design
- RF IC Design
- Synopsys EDA Tool Flow for Front-End Digital IC Design
- Synopsys EDA Tool Flow for Back-End Digital IC Design
- Thermal and Electro-Thermal Simulation: Achievements and Trends

Short Lectures and Workshops

Short Lectures

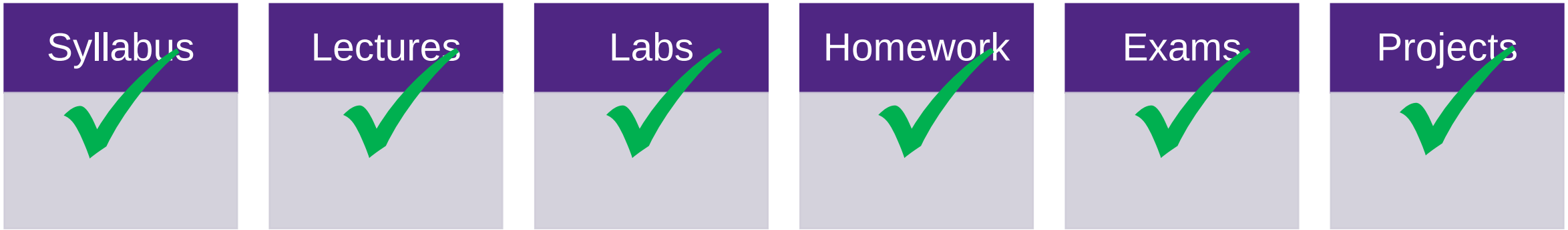
- Basic Perl Programming
- Characterization with SiliconSmart
- Circuit Simulation Transient Analysis
- Compiler Optimization and Code Generation
- Computer Networks
- Digital Design with Verilog
- Digital System Design and Simulation with VHDL
- Embedded Systems Design
- How to Create an Interoperable PDK
- IC Fabrication
- IC Simulation Theory
- Introduction to RF Communication
- Introduction to Verilog HDL
- Low Power Design w/Synopsys 32/28nm Generic Library
- Low Power Methodology Manual for 32/28nm
- Operational Research
- Optimization Methods
- Physical Verification Russet Development
- Power-Performance Optimization of Digital Circuits
- Process Variation Aware Design
- RF Circuits
- Scripting Languages
- Sequential Elements
- Signal and Power Integrity
- Statistical Techniques for Timing Analysis
- Subthreshold Design and Implementation
- Synthesizing OpenSPARC with 32/28nm EDK
- Techniques for Circuit Simulation
- User Interface Design
- Verification Methodology for Low Power

Workshops

- Advanced Design of Digital Circuits for Specific Applications
- ASIC Design Flow Tutorial Based on Synopsys 32/28nm Library
- ASIC Design Flow Tutorial Based on Synopsys 90nm Library
- Chip Design
- Computer Arithmetic Applied to High-Performance Cryptography
- Design for Testability
- Full Custom IC Design Flow with Synopsys Custom Tools
- Project Management
- Software Methodology Module for Custom Designer
- Synopsys Design Flow Tutorial
- Synopsys IC Design Flow Based on 90nm Generic Library
- SystemVerilog Verification Tutorial
- TCAD Course
- TCAD for VLSI Design
- TCAD Quick Start Guide
- TCAD Short Course
- Universal Verification Methodology

Full Semester Courses

- Topics cover all aspects of IC/SoC design
- Courseware for Bachelor and Master level programs
- Full-semester courses contain ~15 weeks of material and include the following components



Teaching Resources

Teaching Support (Generic Libraries, PDKs, Generic Memory Compiler)

Generic Libraries (EDK)

- 32/28nm and 90nm

- Enables students to master advanced design methods using the latest Synopsys EDA tools
- Includes:

Digital Standard Cell Library	I/O Cell Library	I/O Special Cell Library	Embedded Memories
Phase Locked Loop	Low Power Memories	Reference Designs	

- Used by Synopsys for:

Curricula Development	Customer Education	Global Technical Services	Application Consultants
To support development of laboratory works and course projects.	To train customers with Leon3 and ORCA processors' design.	To train internal staff and customers on Synopsys tools and low power flows.	To develop and test sample designs and Reference Methodology scripts.

Interoperable Process Design Kits (iPDKs)

- 32/28nm and 90nm

- Enables students to master AMS/Custom design with the Synopsys custom implementation tool suite
- Includes:

Technology Files	Parasitic Extraction Files	Symbol Library and Python PCells	Embedded Memories
Physical Verification Files	HSPICE Models	Callback Scripts	Setup Files

Curricula Development	Customer Education	Global Technical Services	Application Consultants
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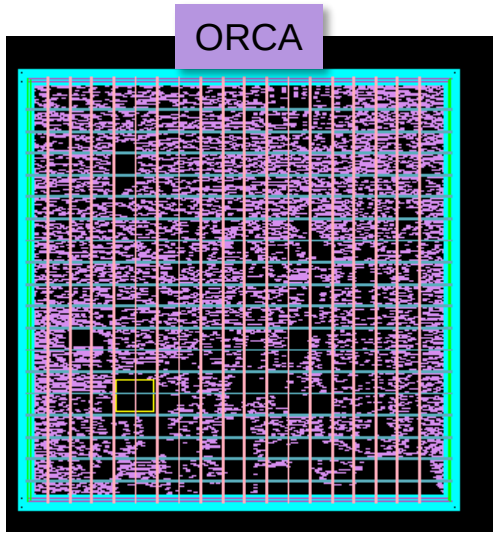
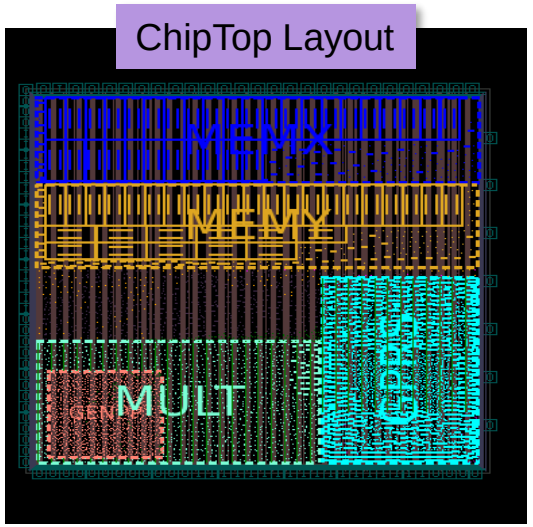
Reference Designs Supported by Synopsys EDKs

- **DesignWare® ARC 600 Academic Core** - 32-bit RISC processor core optimized for embedded applications and DSP tasks
- **ARM® Cortex® - M0 DesignStart™ Processor** - Entry-level configuration of ARM Cortex-M0 microprocessor[1]
- **OpenSPARC T1** - 64-bit multicore processor[2]
- **LEON3** - 32-bit embedded processor[2]
- Sample Processor Designs - included in EDK
  - ORCA for timing analysis
  - ChipTop for low power design

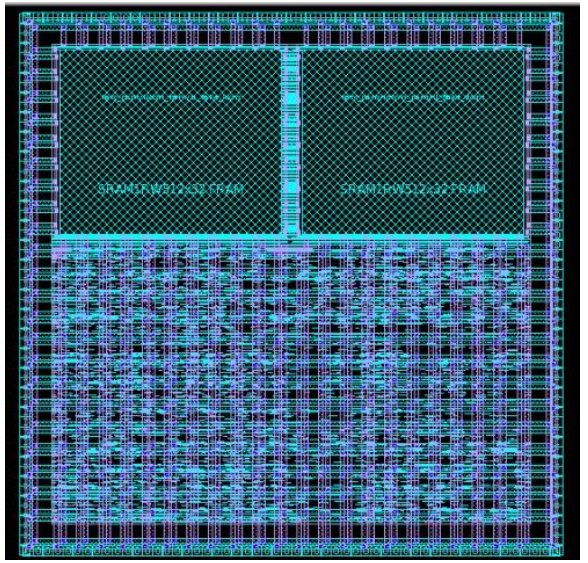




1. *Available through ARM DesignStart for Processor IP portal*
2. *Available via GNU General Public License*

DesignWare ARC 600 Processor Design

- Synthesis scripts optimized for 32/28nm EDK that can be used to easily redesign the academic version of the ARC 600 processor
- Synopsys curriculum for the ARC 600
  - IC Synthesis Based on DesignWare ARC 600 Core, includes:
    - Lecture slides
      - Covers ARC 600 details and EDA tool use
    - Laboratory works
      - Step-by-step guide of the ARC 600 design process

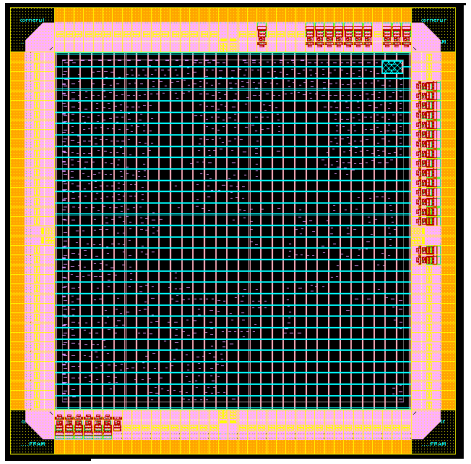


Apply in Members Only for access to the DesignWare ARC 600 Academic Core:
https://www.synopsys.com/apps/protected/university/members.html

ARM Cortex-M0 DesignStart Processor Design

- Complete Synthesizable Solution
  - Pre-configured Verilog netlist derived from commercial Cortex-M0 processor
  - Simple testbench
  - Example test code
- Scripts to implement the ARM Cortex-M0 DesignStart design using Synopsys 32/28nm EDK and EDA tools
- Synopsys curriculum for the ARM Cortex-M0
  - IC Synthesis Based on ARM Cortex-M0 DesignStart Processor

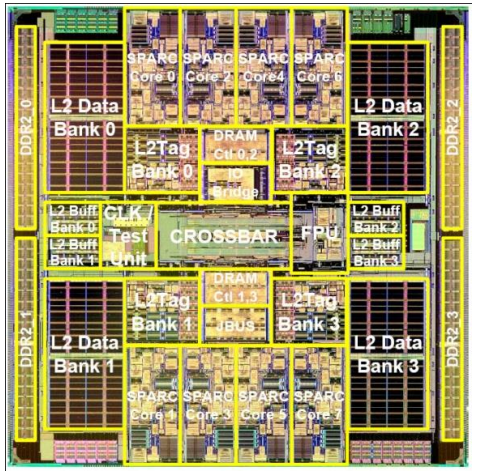
Download from ARM DesignStart for Processor IP portal:
http://arm.com/products/processors/designstart-processor-ip

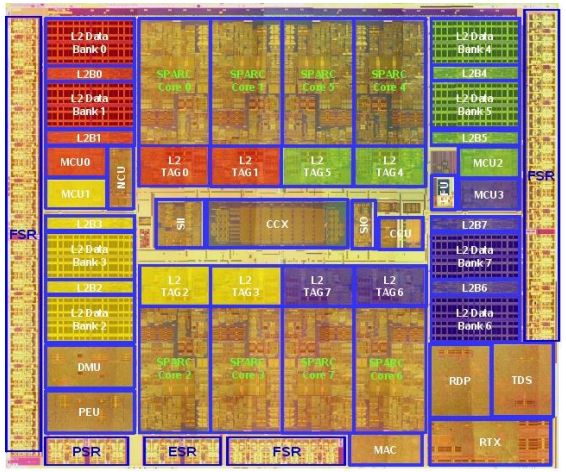


OpenSPARC Processor Design

- Scripts to enable OpenSPARC design using Synopsys 32/28nm EDK and Design Compiler
- Implemented low power design techniques
- Synopsys curriculum for OpenSPARC
  - Computer Architecture
  - Includes:
    - Physical design scripts for IC Compiler
    - Scripts to enable small block reuse for educational purposes
    - Various lab projects based on small blocks

Download OpenSPARC:
http://www.opensparc.net





Synopsys Generic Memory Compiler

- Configurable software that automatically generates static RAM circuits of different types and sizes with all required deliverables
- Generate custom memory instances for educational ICs
- Designed for use with Synopsys EDKs and EDA tools
- Optimized for the Synopsys Digital Design Flow
- Supports multiple technologies (90nm, 32/28nm, etc.)

User interface

- Command line
- GUI

Supported memory types

- 1 port SRAM
- 2 port SRAM
- 1 port Low Power SRAM
- 2 port Low Power SRAM

*"Using the Synopsys Generic Memory Compiler in our complex processor for DSP application was a **great time-saving tool**. It helped the students generate the SRAM they wanted in a snap, saving them critical time to concentrate on the rest of the complex design."*

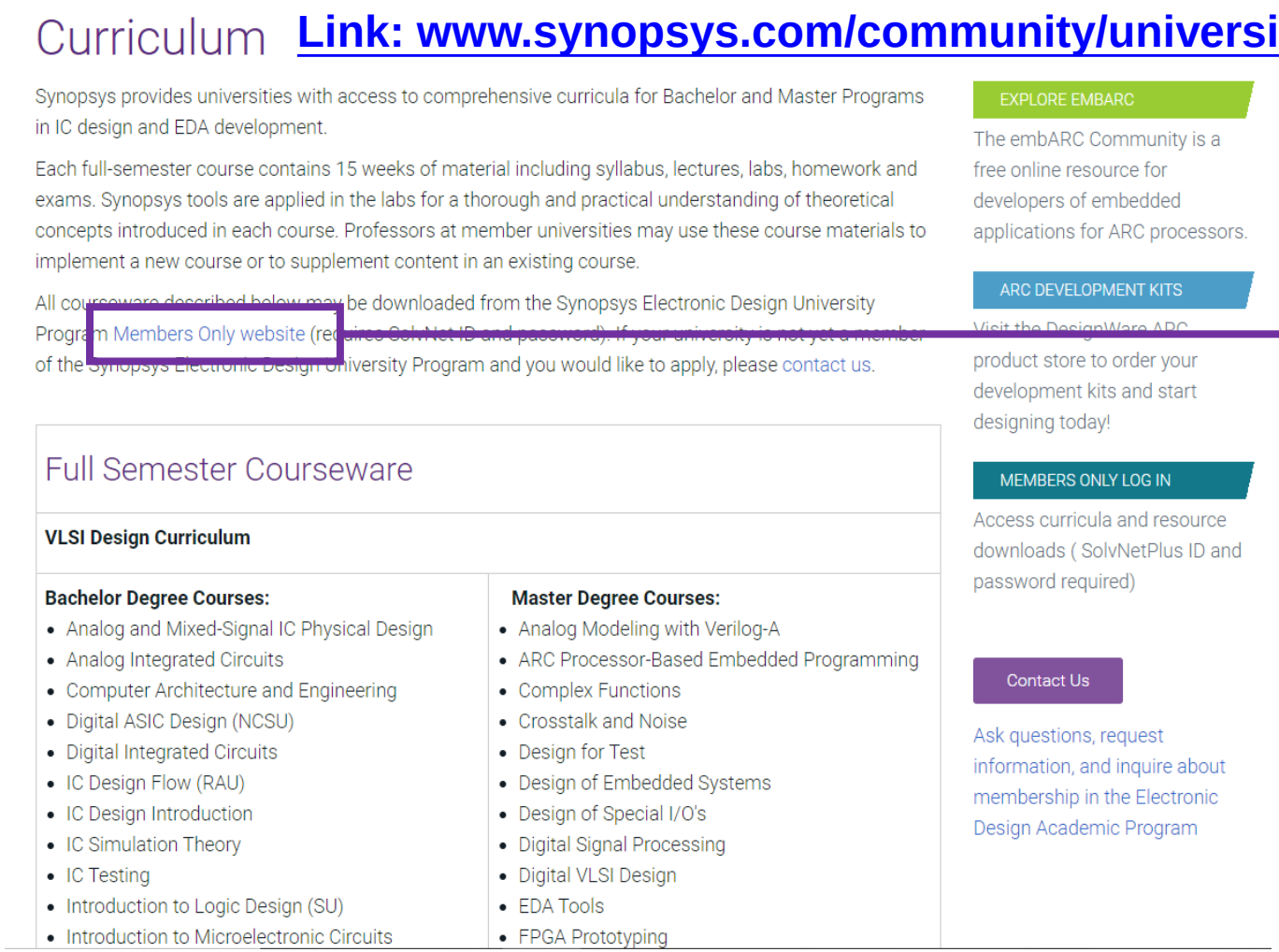
Dr. Maged Ghoneima, American University in Cairo

Get started w/ Teaching Resources

Link: www.synopsys.com/community/university-program.html

01 Go to Electronic University Program website

Select the Teaching Resources that you need, then click on “ Members Only website”.



Curriculum

Link: www.synopsys.com/community/university-program.html

Synopsys provides universities with access to comprehensive curricula for Bachelor and Master Programs in IC design and EDA development.

Each full-semester course contains 15 weeks of material including syllabus, lectures, labs, homework and exams. Synopsys tools are applied in the labs for a thorough and practical understanding of theoretical concepts introduced in each course. Professors at member universities may use these course materials to implement a new course or to supplement content in an existing course.

All courseware described below may be downloaded from the Synopsys Electronic Design University Program Members Only website (requires SolvNet ID and password). If your university is not yet a member of the Synopsys Electronic Design University Program and you would like to apply, please contact us.

Full Semester Courseware

VLSI Design Curriculum

Bachelor Degree Courses:

- Analog and Mixed-Signal IC Physical Design
- Analog Integrated Circuits
- Computer Architecture and Engineering
- Digital ASIC Design (NCSU)
- Digital Integrated Circuits
- IC Design Flow (RAU)
- IC Design Introduction
- IC Simulation Theory
- IC Testing
- Introduction to Logic Design (SU)
- Introduction to Microelectronic Circuits

Master Degree Courses:

- Analog Modeling with Verilog-A
- ARC Processor-Based Embedded Programming
- Complex Functions
- Crosstalk and Noise
- Design for Test
- Design of Embedded Systems
- Design of Special I/O's
- Digital Signal Processing
- Digital VLSI Design
- EDA Tools
- FPGA Prototyping

EXPLORE EMBARC

The embARC Community is a free online resource for developers of embedded applications for ARC processors.

ARC DEVELOPMENT KITS

Visit the DesignWare ARC product store to order your development kits and start designing today!

MEMBERS ONLY LOG IN

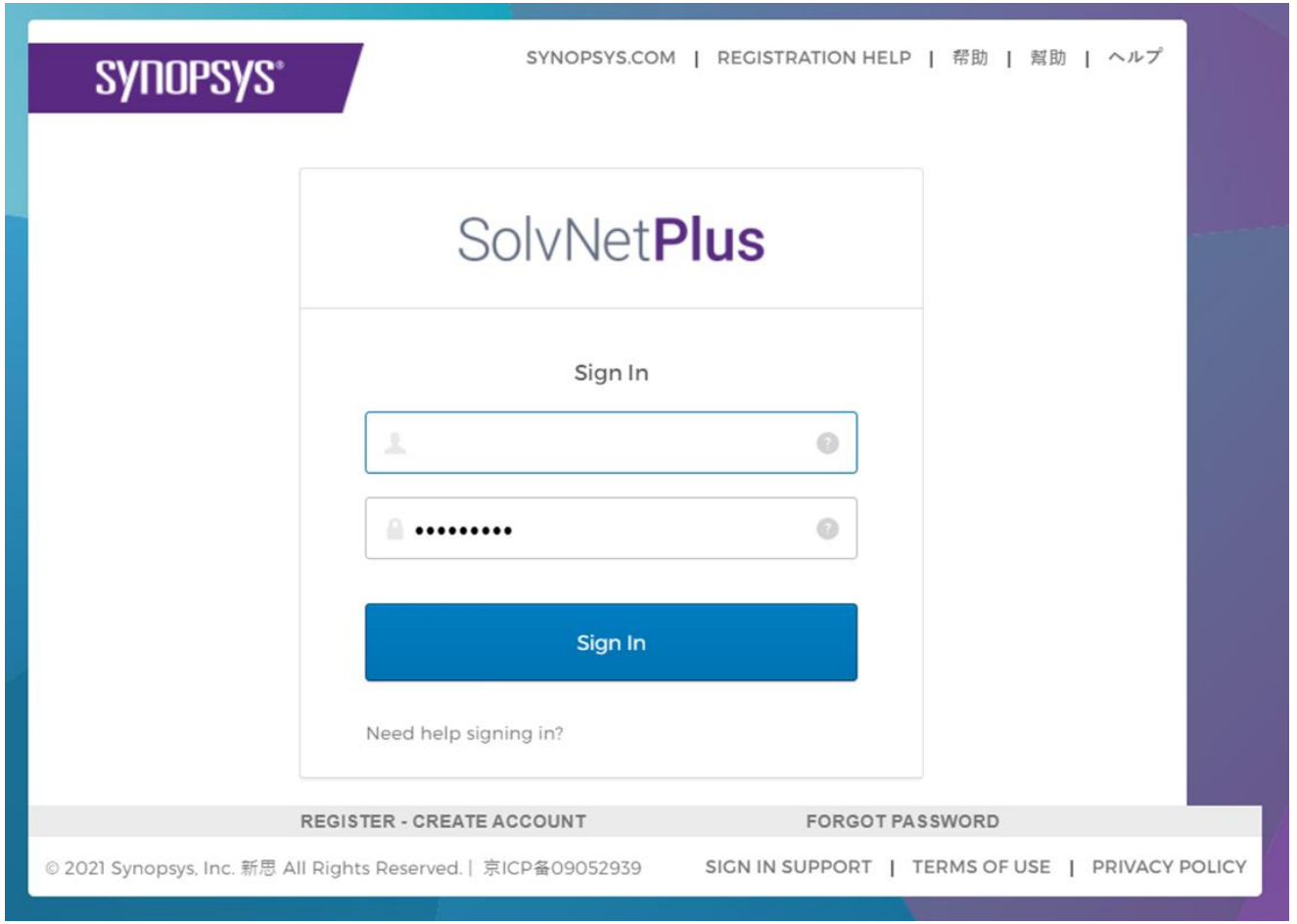
Access curricula and resource downloads (SolvNetPlus ID and password required)

Contact Us

Ask questions, request information, and inquire about membership in the Electronic Design Academic Program

- Requires a SolvNetPlus account to sign in.
- Please contact *Synopsys University Program – Taiwan (chunhsu@synopsys.com)* for membership enquiry.

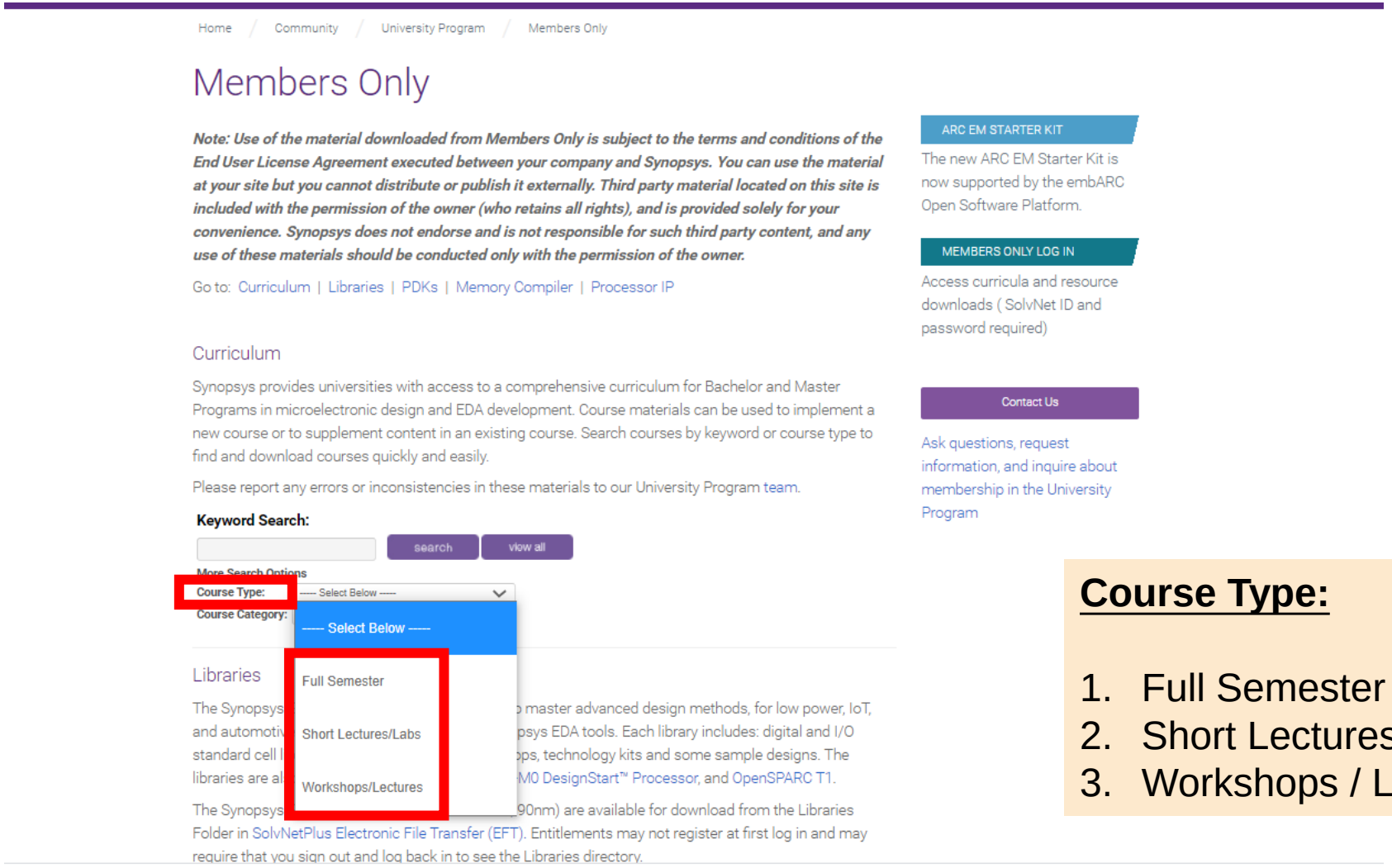
02 Log-in with Synopsys SolvNetPlus credential



https://www.synopsys.com/apps/protected/university/members.html

03 Insert course name in the search engine

Search by “Course Type”



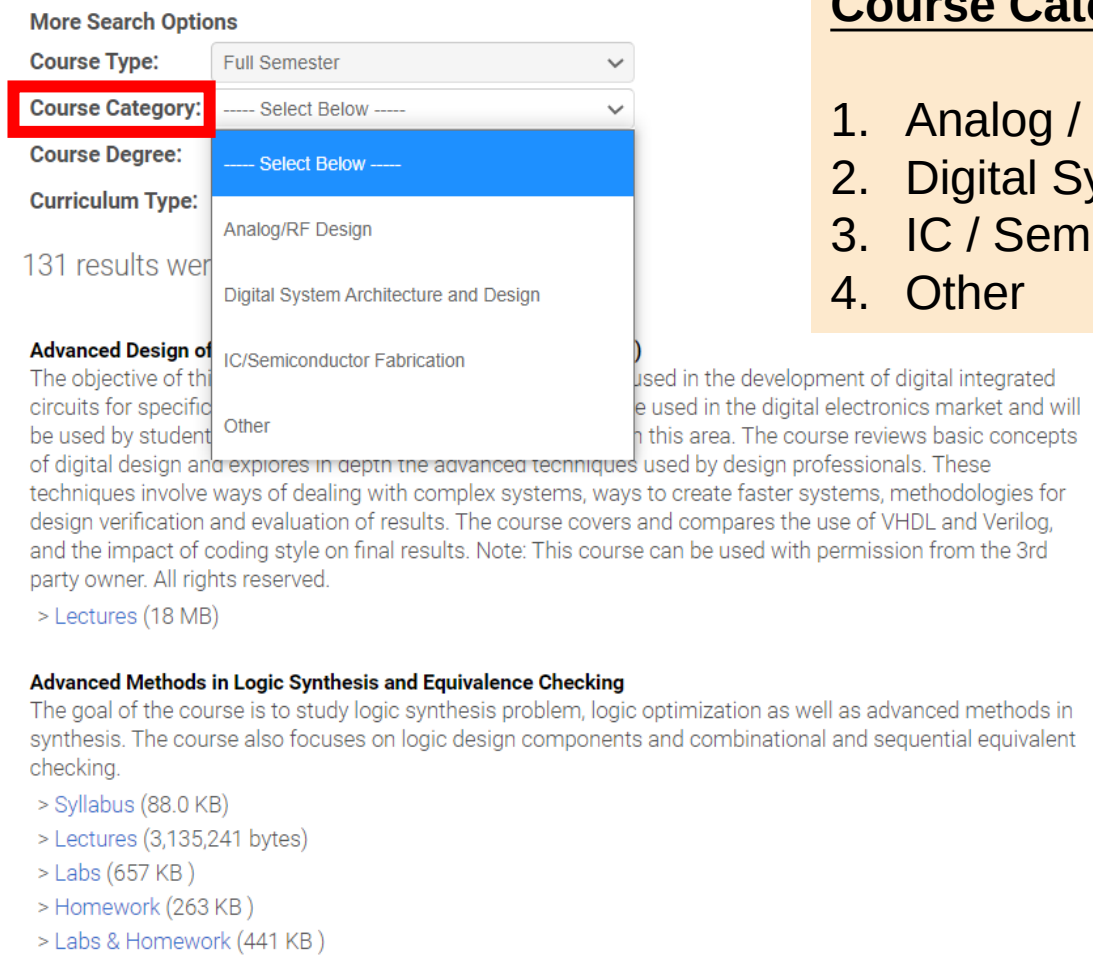
Course Type:

1. Full Semester
2. Short Lectures / Labs
3. Workshops / Lecturers

03 Insert course name in the search engine (cont.)

Search by “Course Category”

Example : Full Semester



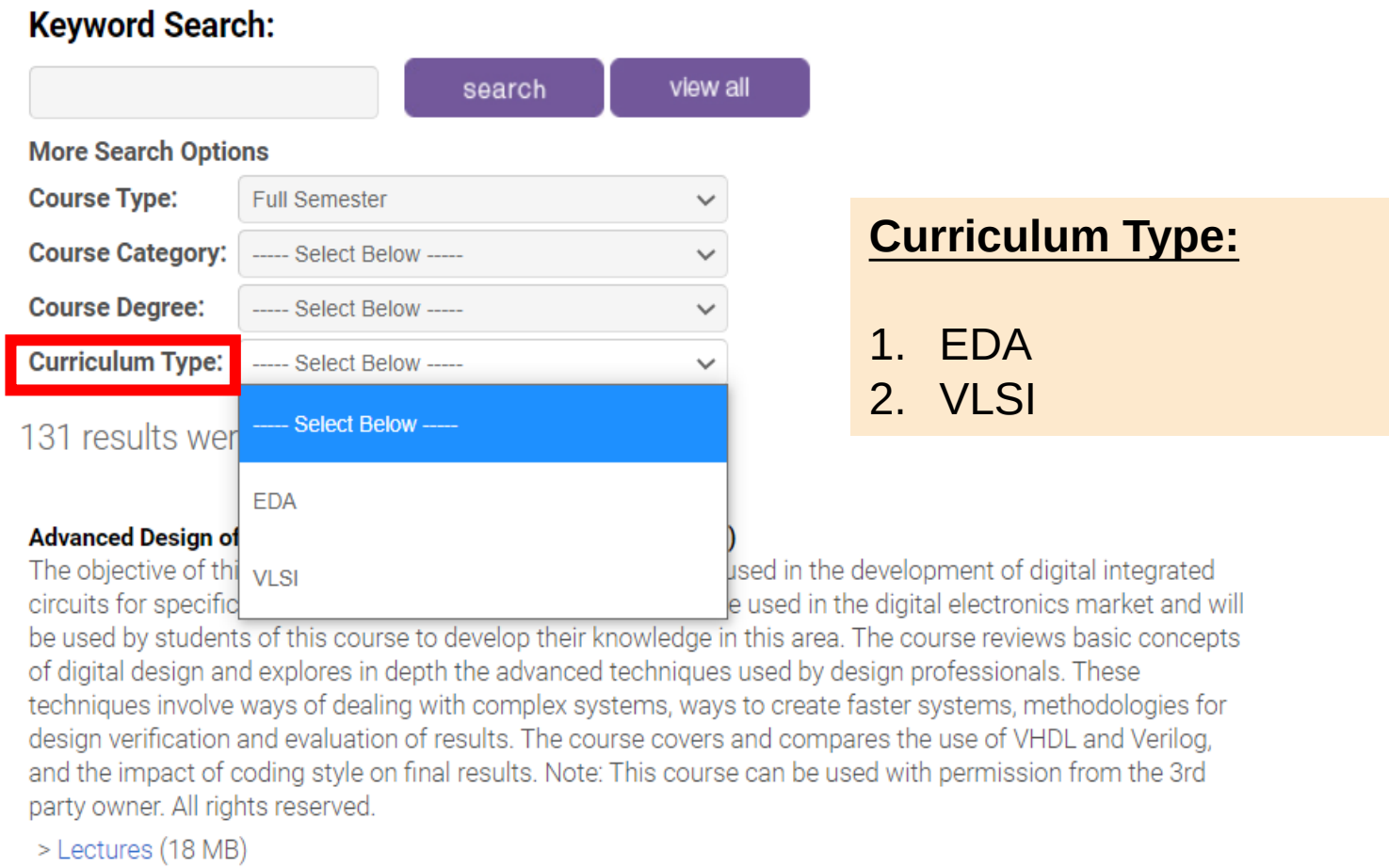
Course Category:

1. Analog / RF Design
2. Digital System Architecture and Design
3. IC / Semiconductor Fabrication
4. Other

03 Insert course name in the search engine (cont.)

Search by “Curriculum Type”

Example : Full Semester



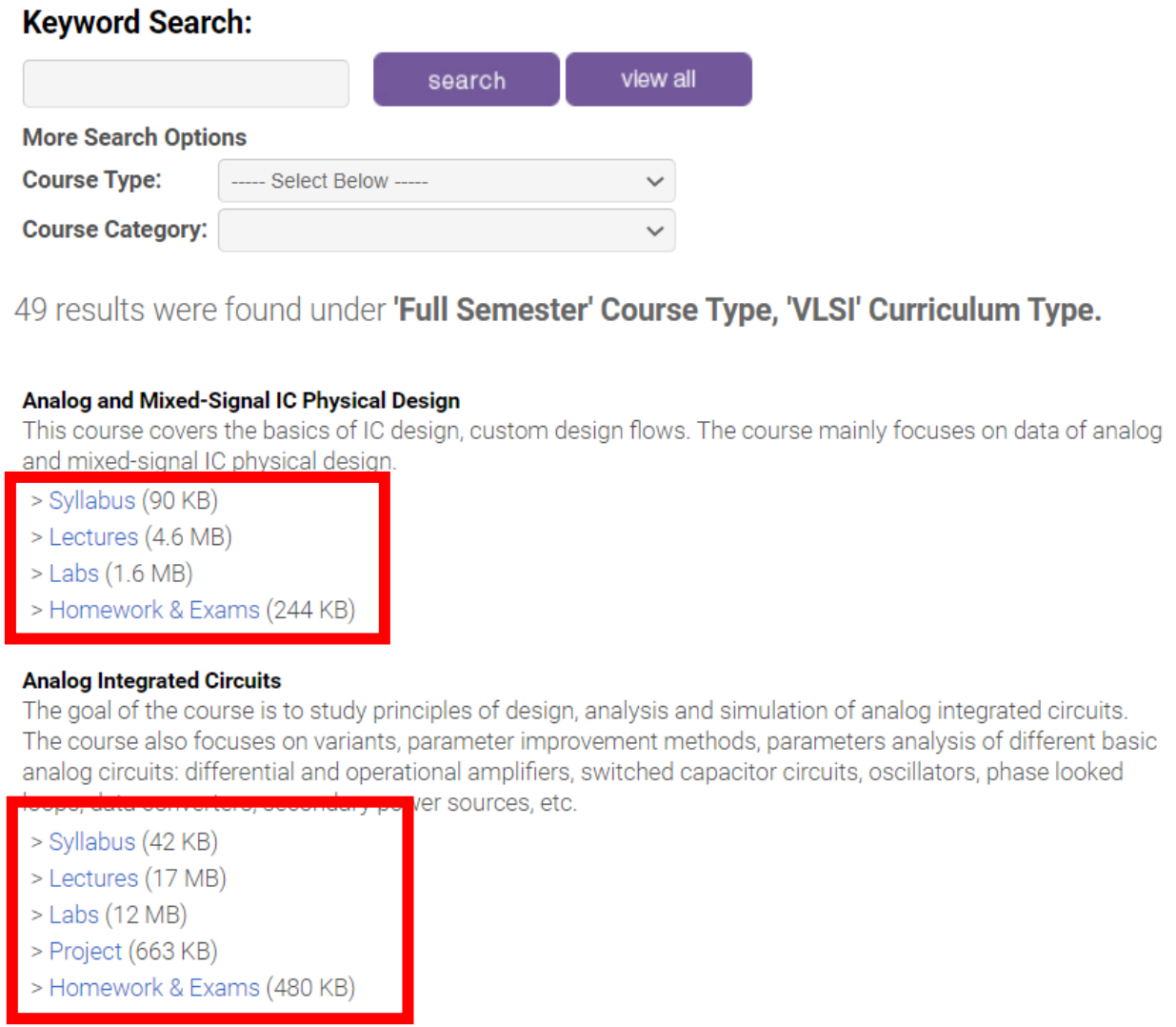
Curriculum Type:

1. EDA
2. VLSI

04 Access to the courseware

Start to download course syllabus, lecturer slides, labs or exams

Example : Full Semester



Course Contents:

1. Syllabus
2. Lectures
3. Labs
4. Project
5. Homework & Exams

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☞ **Access through:**
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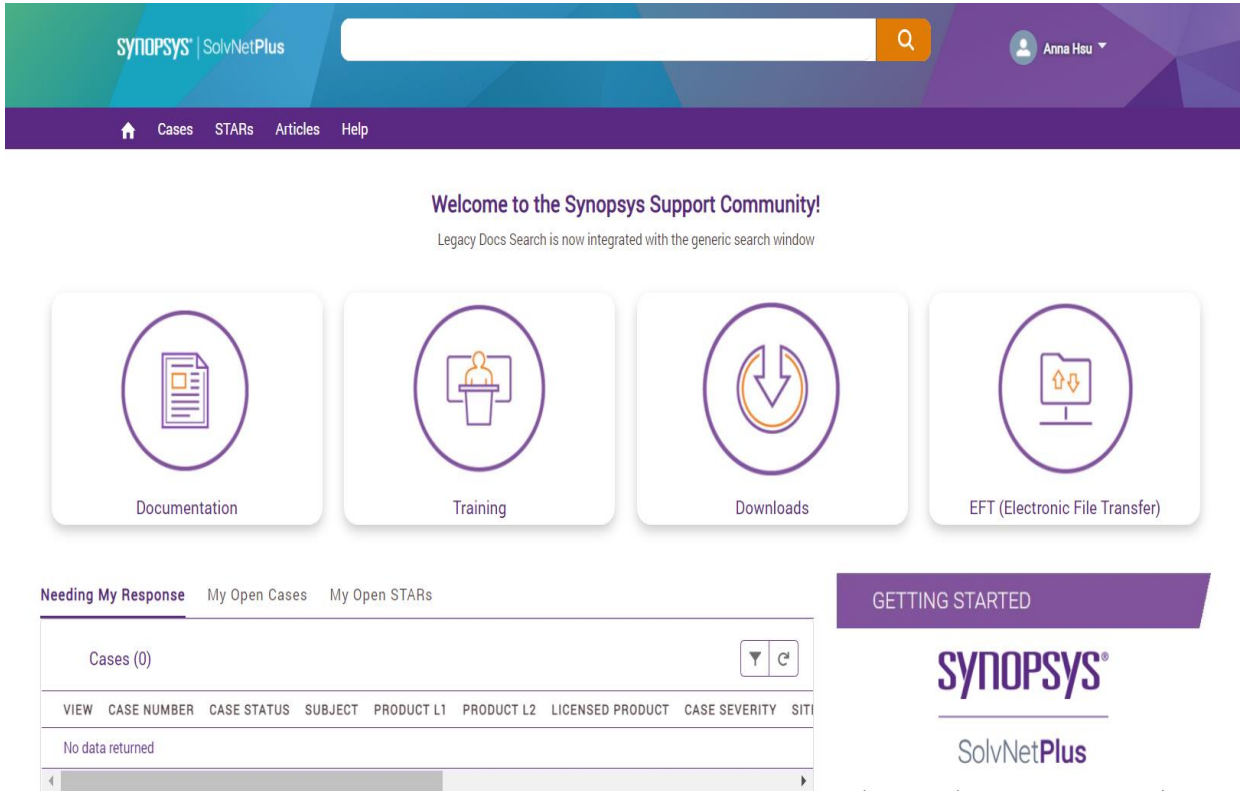
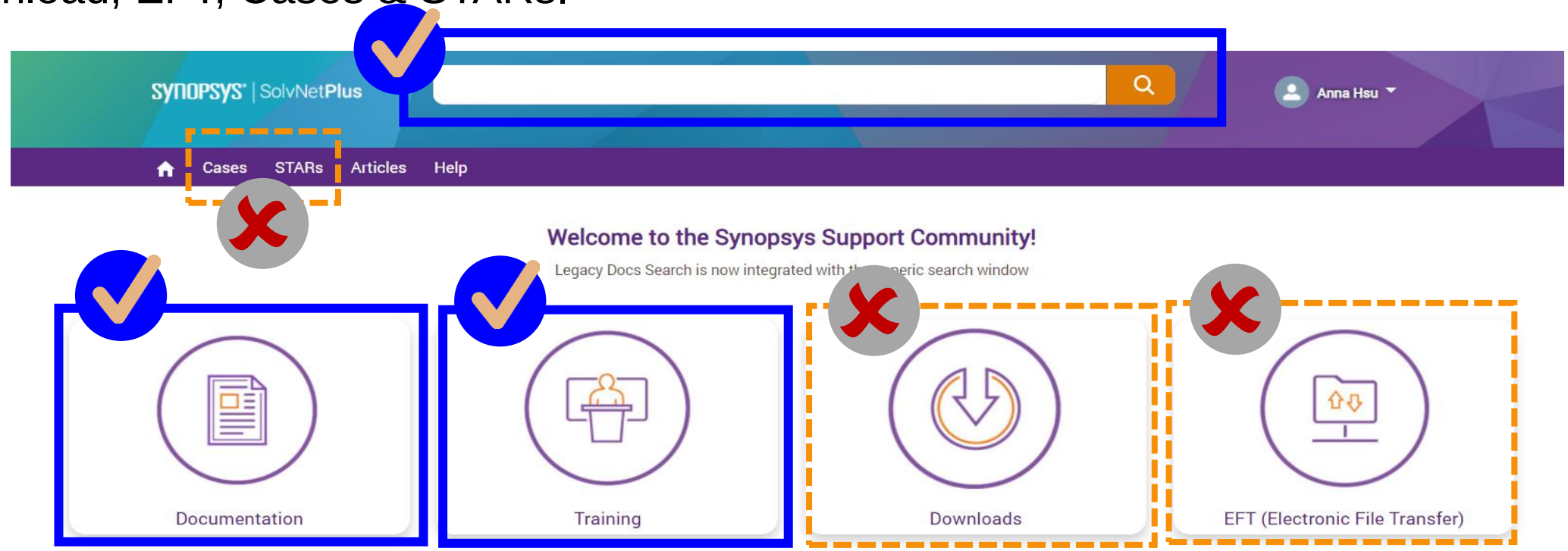


Get Oriented with SolvNetPlus

University users can access Documentation, Training & Search ; but CANNOT access Download, EFT, Cases & STARs.



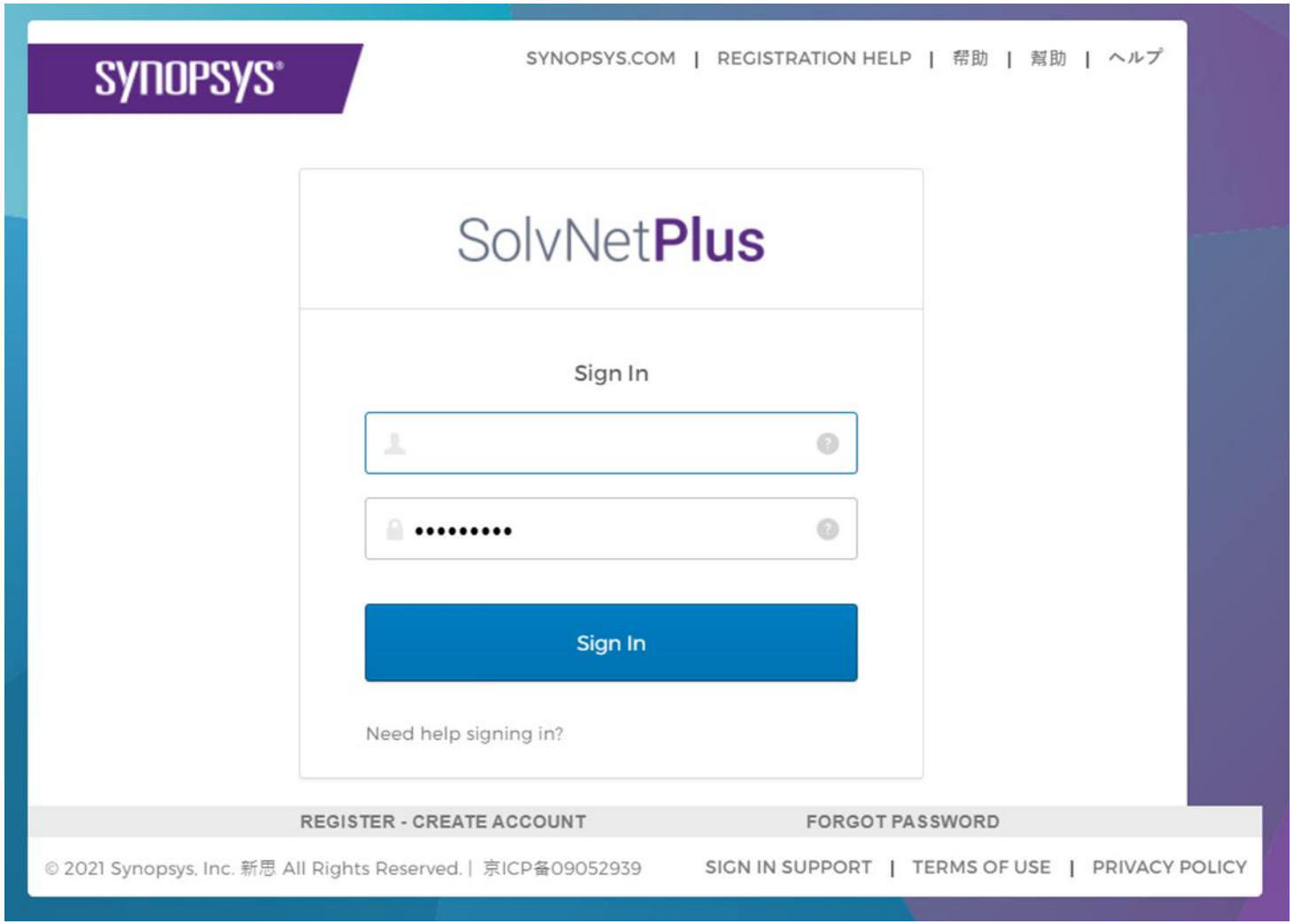
Knowledge Base

SolvNetPlus (Documentation & Search)

Get started w/ SolvNetPlus

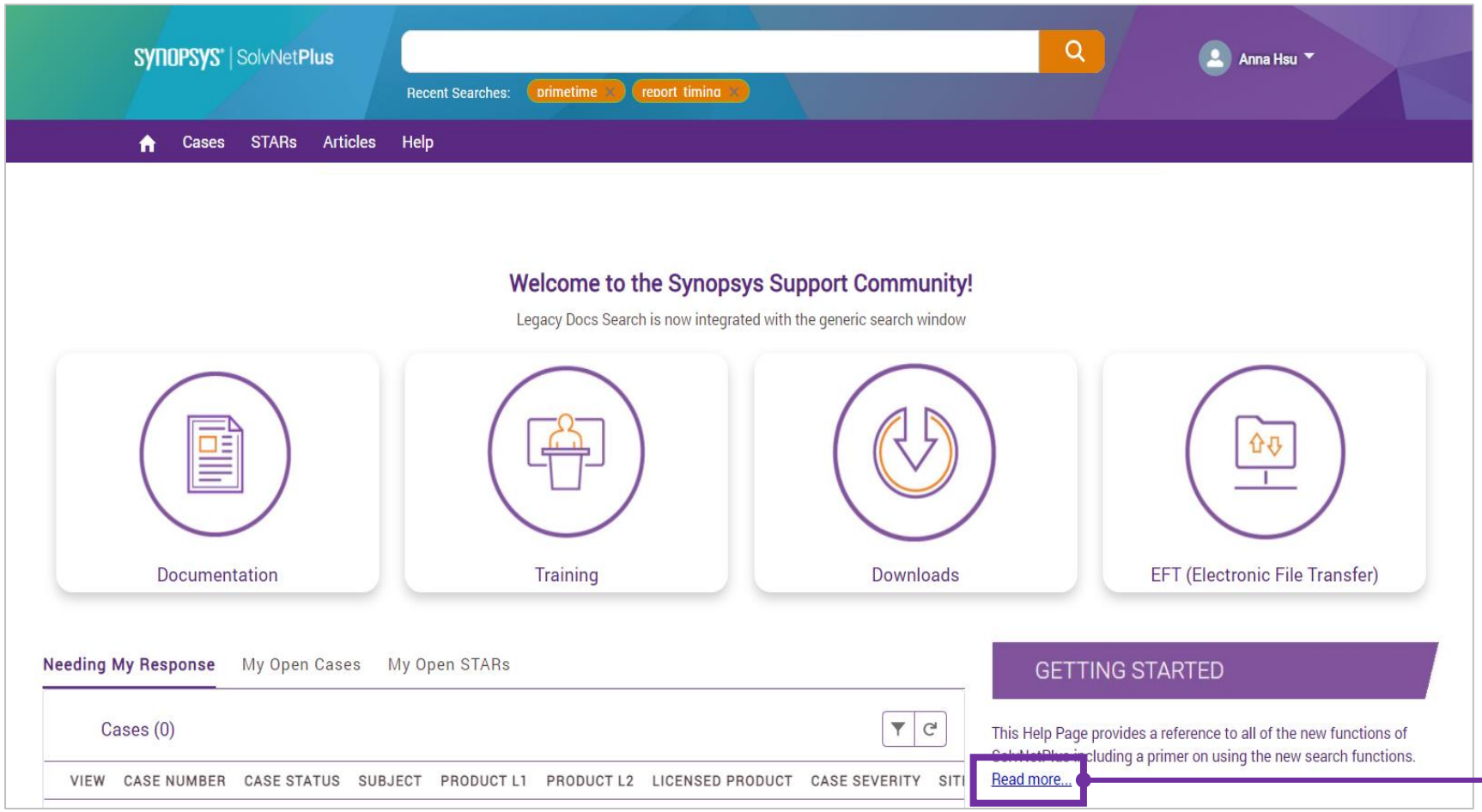
https://solvnetplus.synopsys.com/

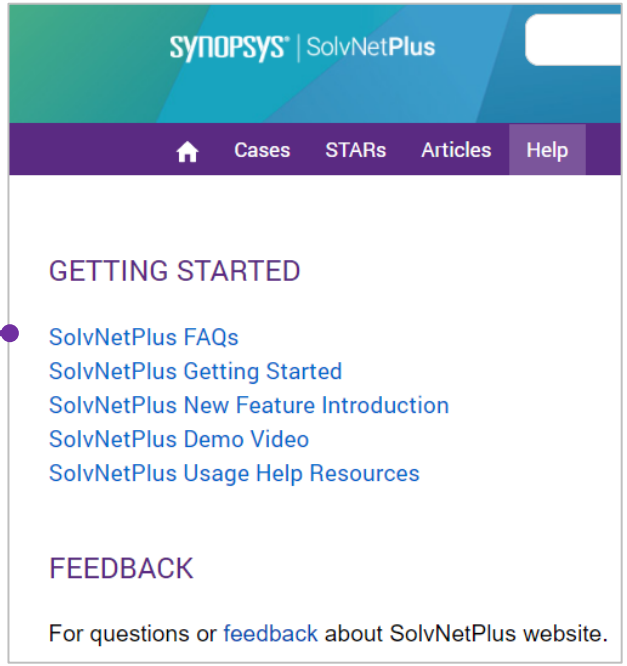
01 Log-in with Synopsys SolvNetPlus credential



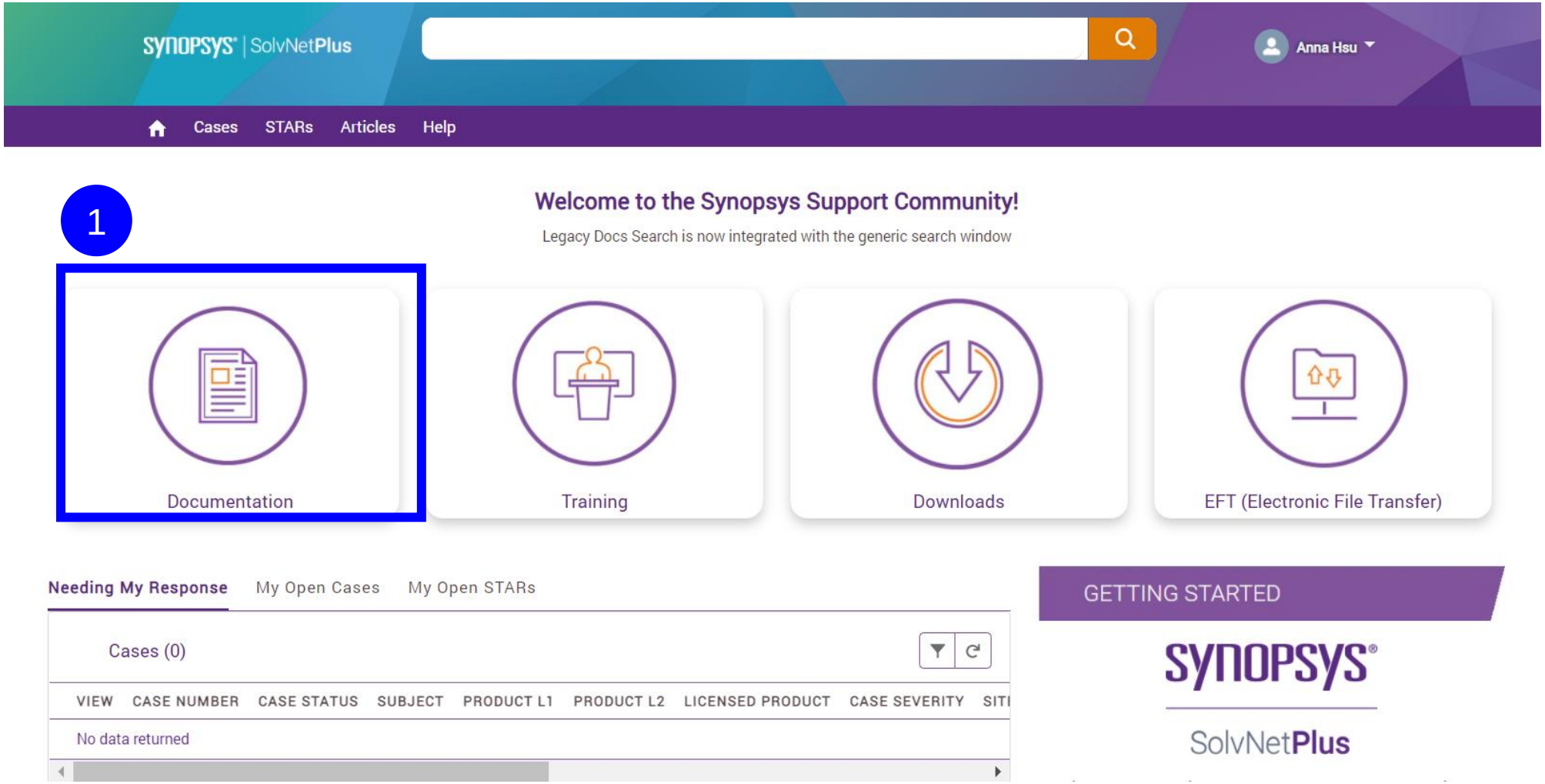
https://solvnet.synopsys.com/

02 Read “ GETTING STARTED” before use



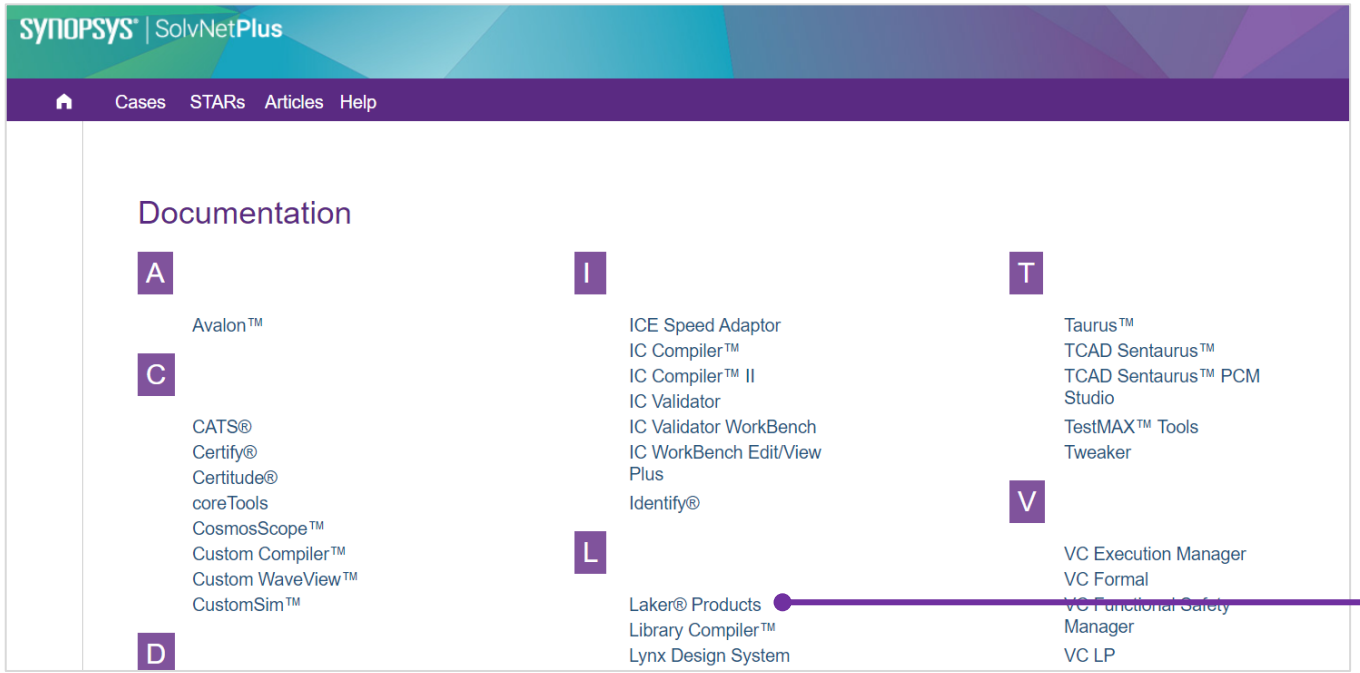


03 Click on “Documentation”



04 Search by product name to get tool documents

You can download release notes, installation guides & user guides and reference manuals from this section



Example : Laker

Laker

Laker3, L-2018.06, June 2018

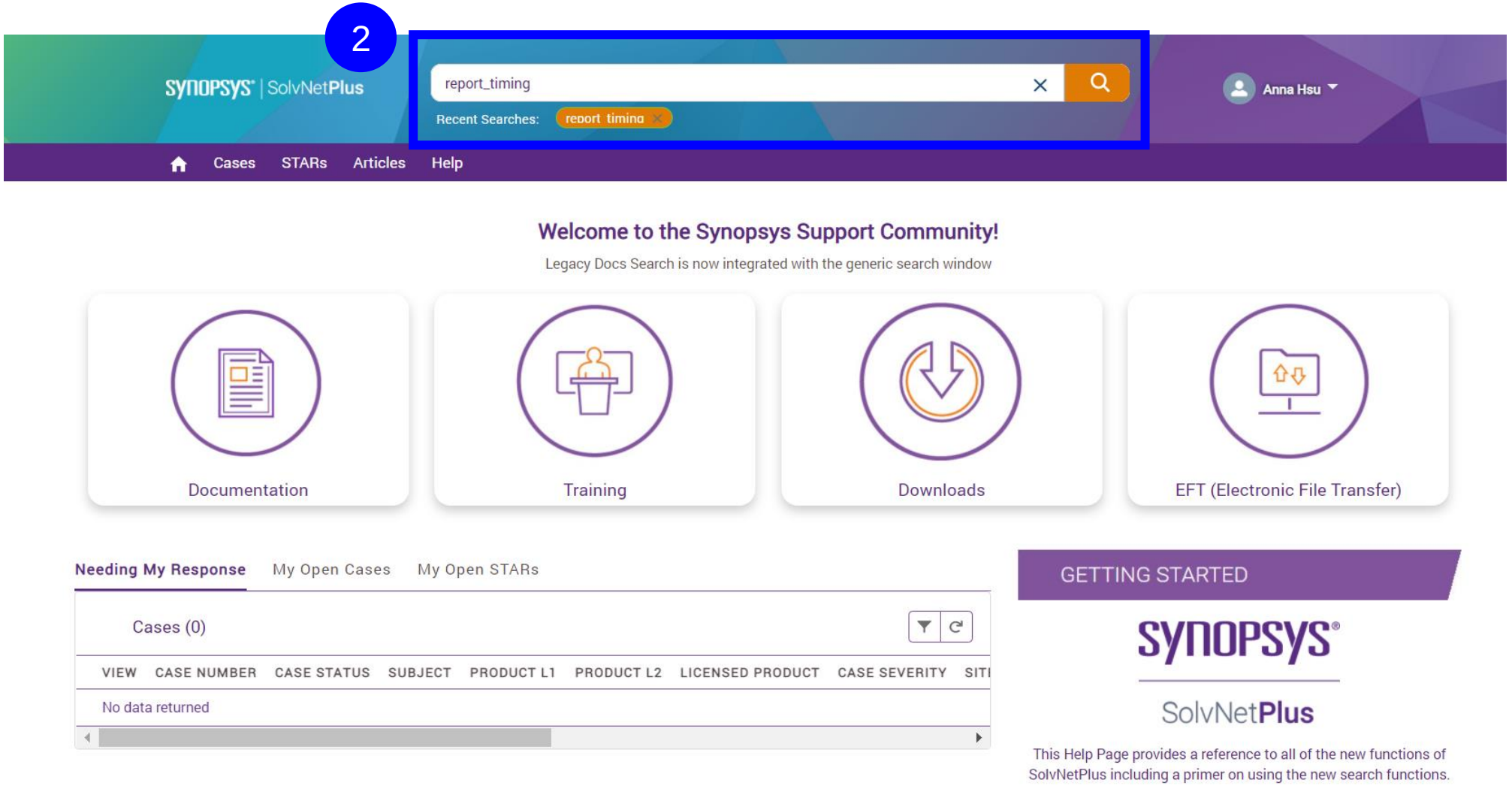
- Laker3 Installation Guide
- Laker3 Quick Start Guide for Laker3 User Interface, K-2015.06, June 2015
- Laker3 Command Reference Manual, K-2015.06, June 2015
- Laker3 Tcl Reference Manual, K-2015.06, June 2015
- Laker3 Bind Key Summary
- Laker3 Menu Summary
- Laker DRD Tcl Command Reference, K-2015.06, June 2015
- Laker CDPR LEF/DEF Tutorial, 2013.02, February 2013
- Laker CDPR Data Preparation and SDL Tutorial, 2013.02, February 2013
- Laker3 Release Notes Version, L-2018.06-SP1 (January 2019)

Laker, 2020.03, March 2020

- Laker User Guide and Tutorial, 2015.03
- Laker Command Reference, 2015.12
- Laker Tcl Reference, 2015.12
- Laker Bind Key Summary, 2015.12
- Laker Command Index, 2015.12

05 Look for information in the “Search” bar

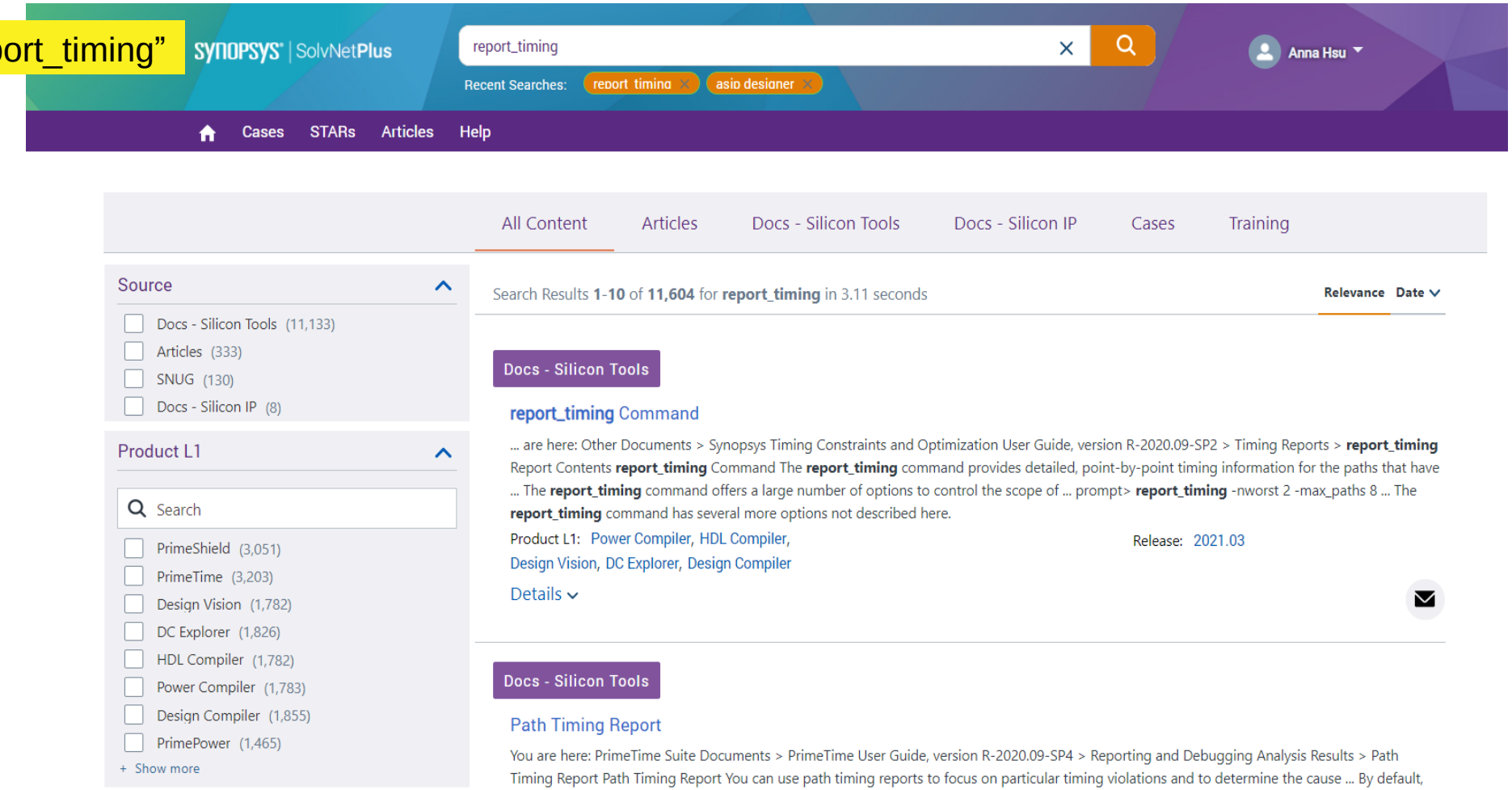
You can use search to retrieve information from various sources



06 Choose needed info from the displayed search results

The information will be displayed from various sources, such as documentation, articles, training, YouTube, and so on (but *NOT* in cases & STARs)

Example : insert “report_timing”

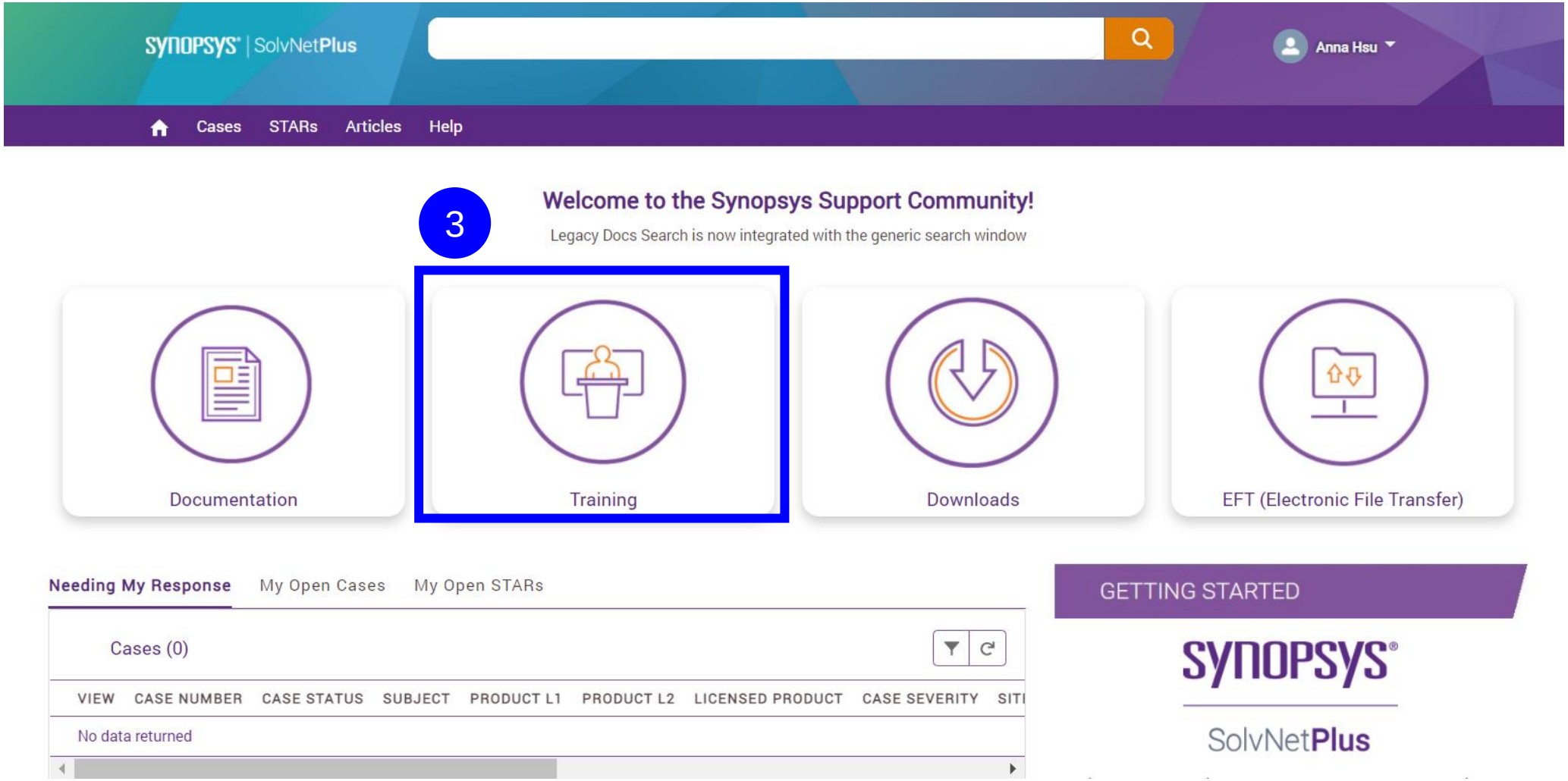


Knowledge Base

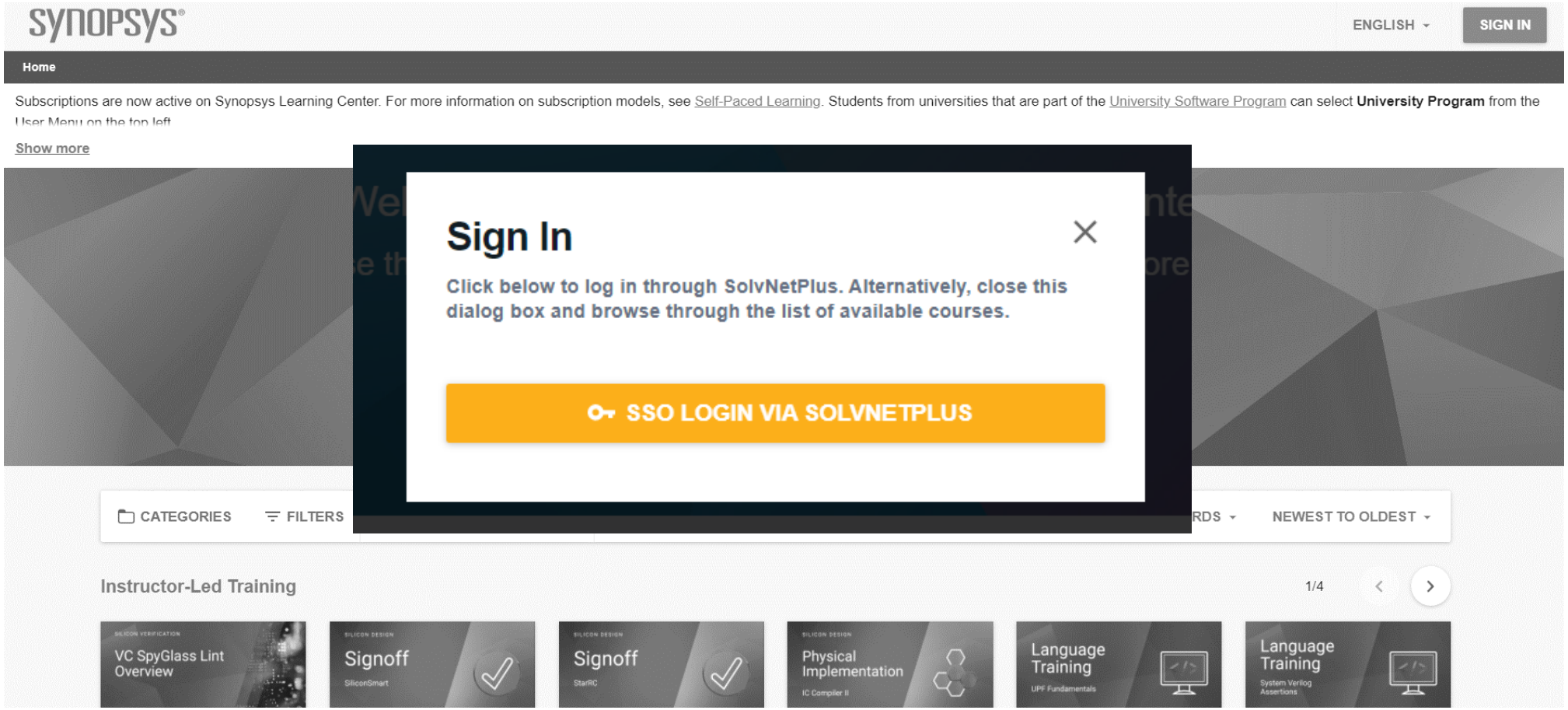
Synopsys Learning Center (Self-paced Learning)

1. Access via SolvNetPlus (https://solvnet.synopsys.com/)
2. Access via Synopsys Learning Center (https://www.synopsys.com/support/training/self-paced.html)

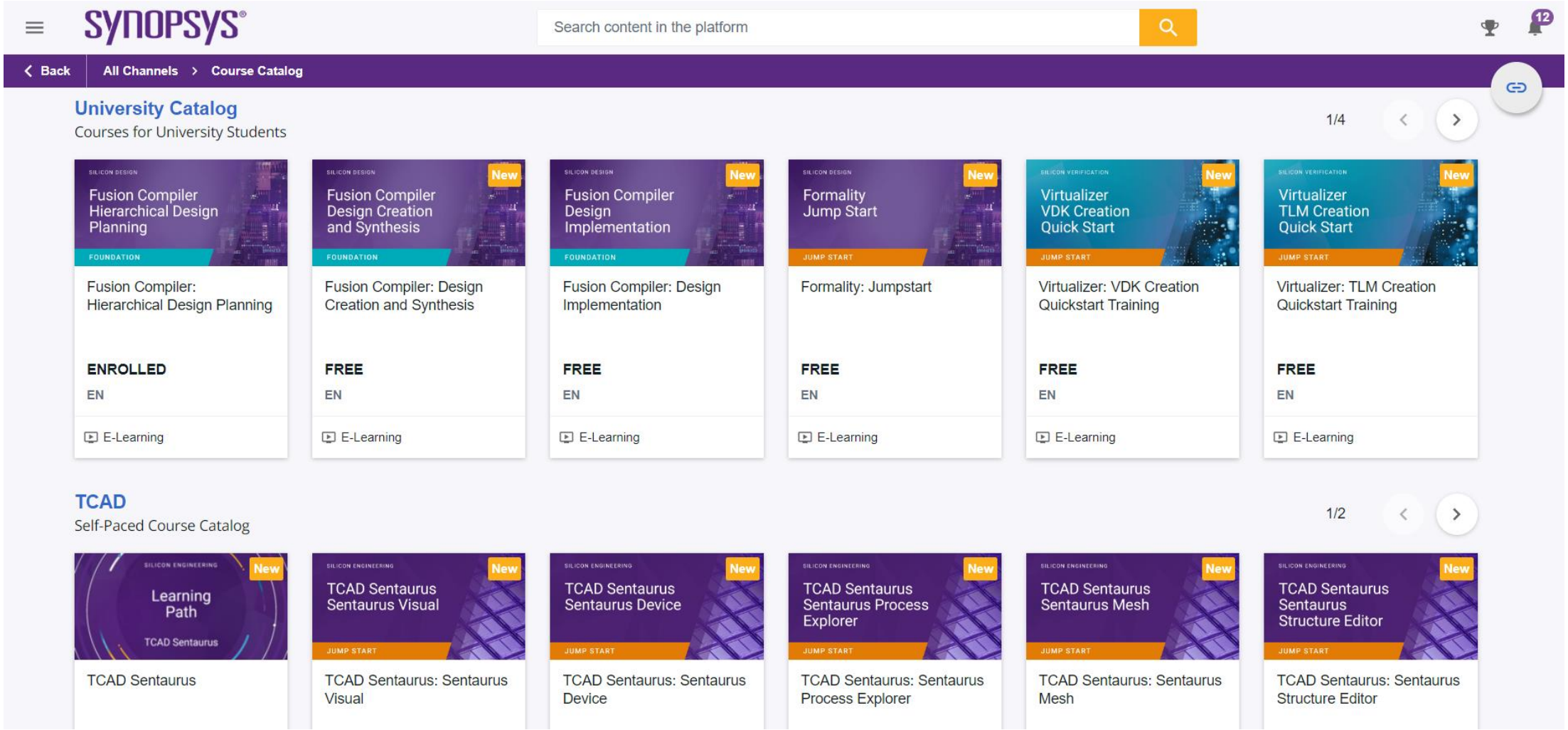
01 Login SolvNetPlus and click “Training”



02 SSO Login via SolvNetPlus

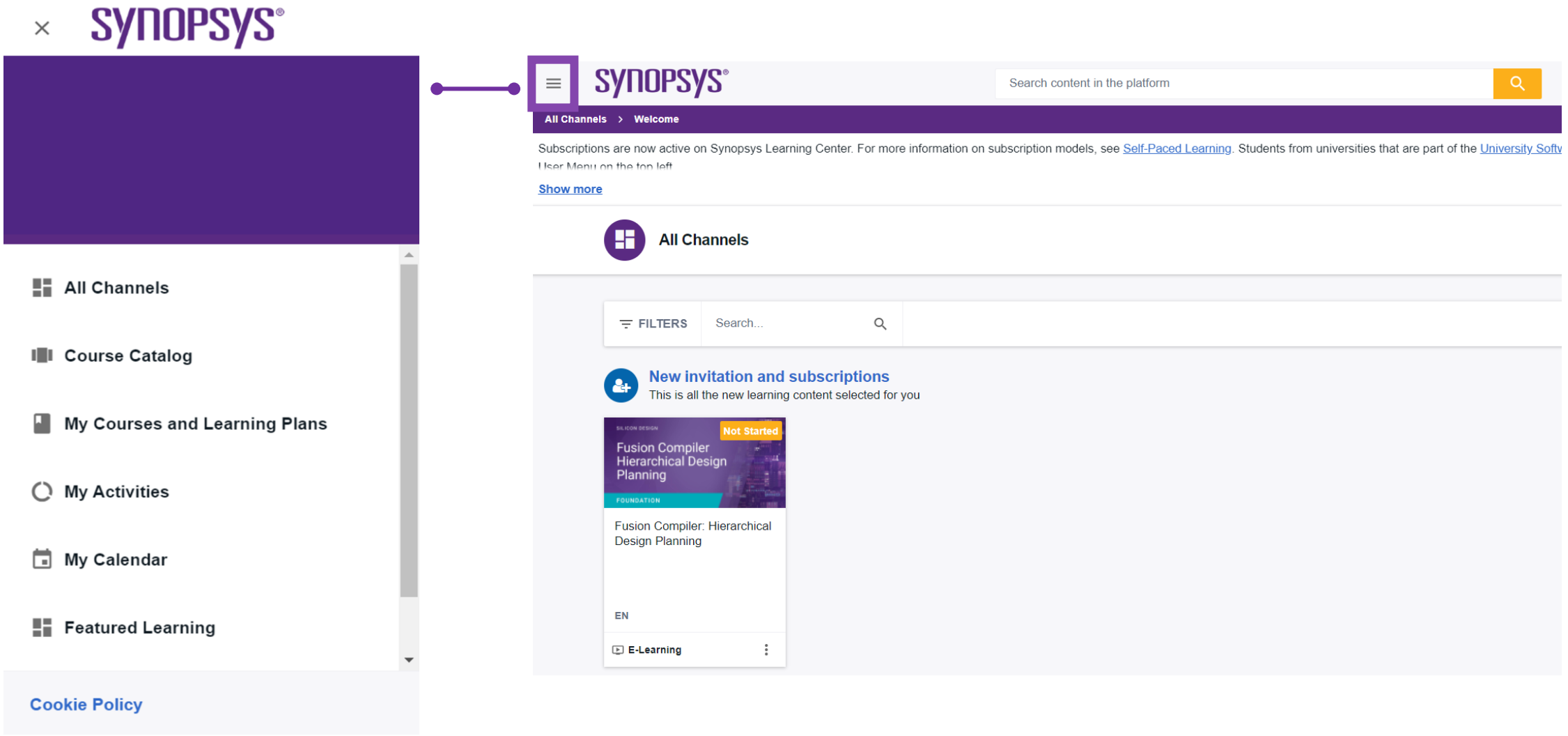


02 Access Synopsys Learning Center

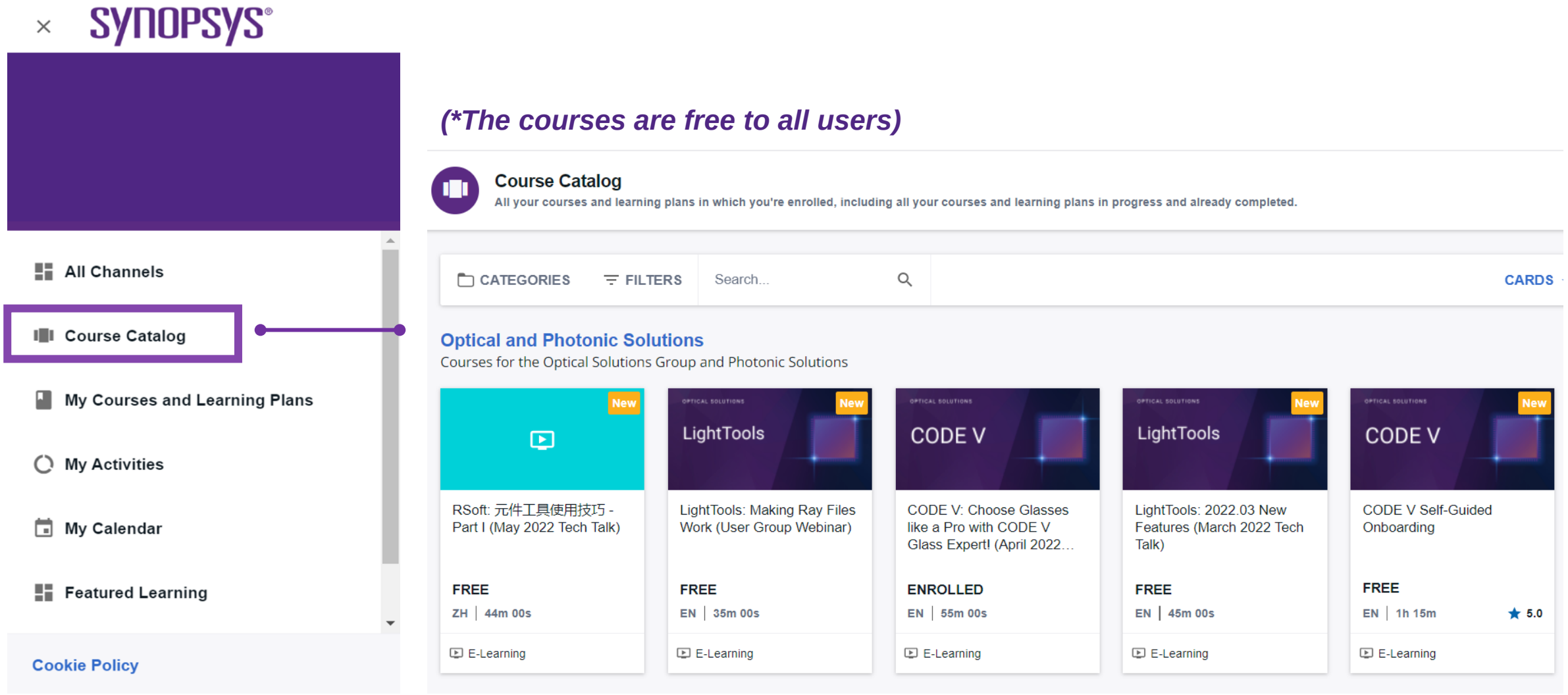


✓ You can also directly access through: https://training.synopsys.com/

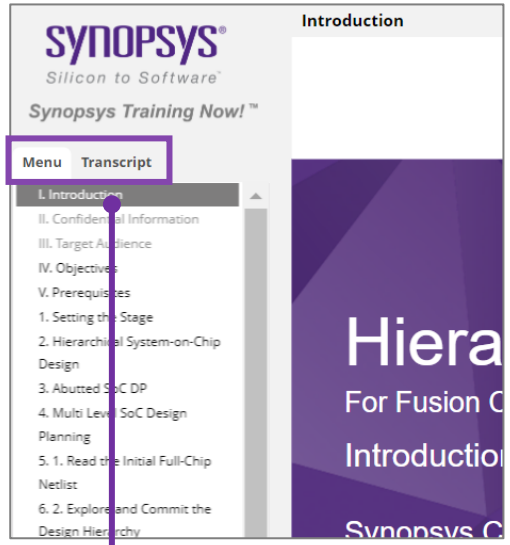
03 Click on “三”



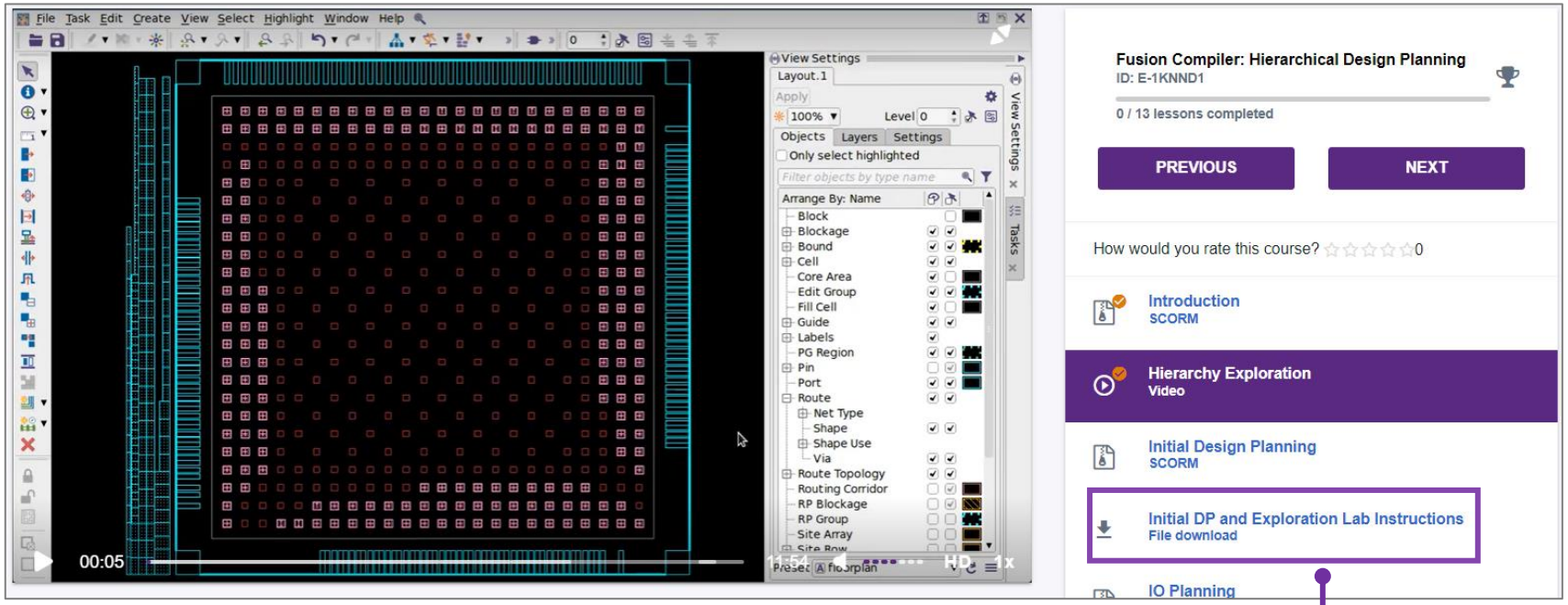
04 Click on “Course Catalog”



05 The Interface of Courses



Menu and transcript are provided.



Downloadable files/instructions

Scroll down to see course description, including abstract, objectives, audience profile, etc.

Course Description

ABSTRACT

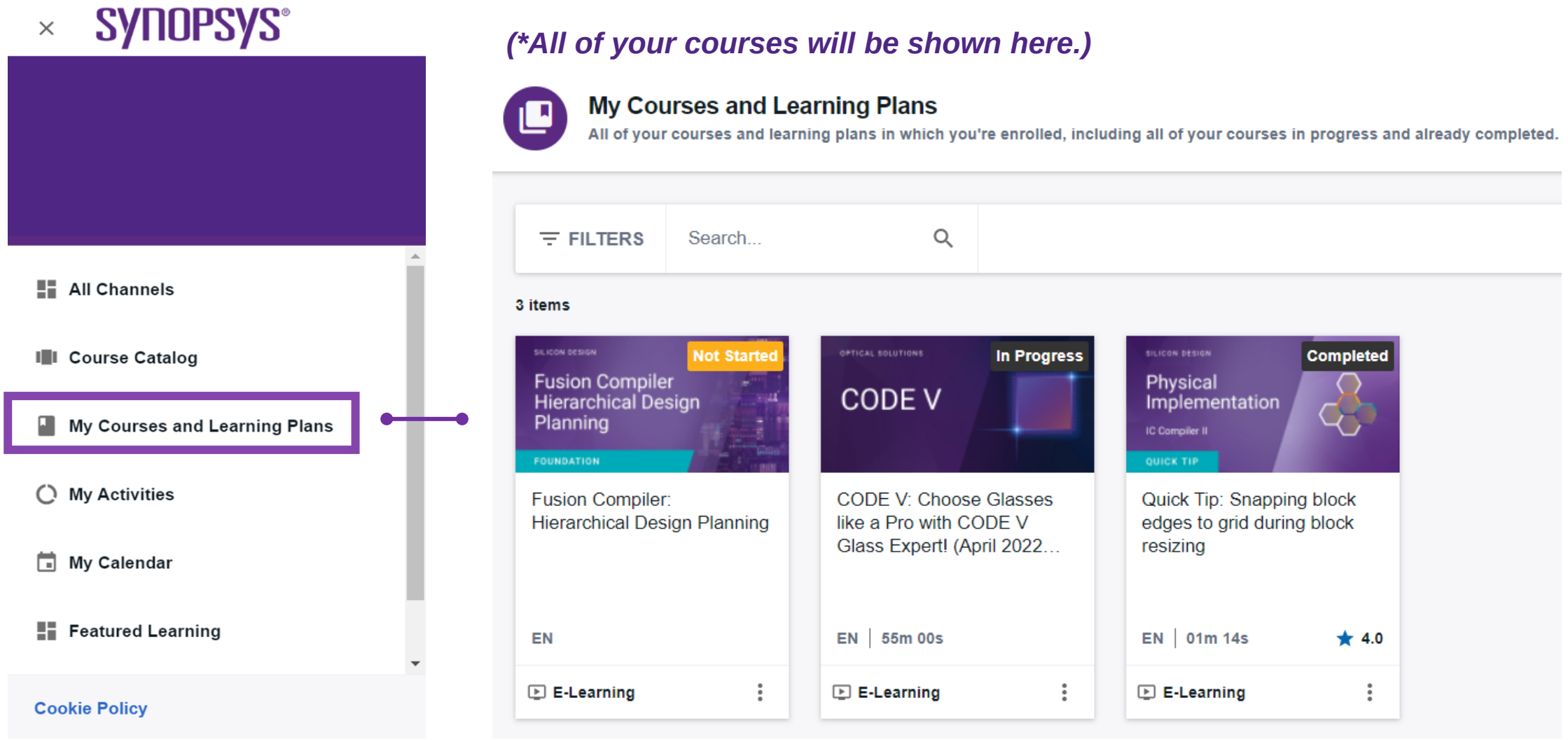
In this hands-on course, you will use Fusion Compiler or IC Compiler II to create chip and block-level floorplans using a hierarchical (top-down) design planning approach. The focus is on multi-voltage (UPF) system-on-a-chip (SoC) designs with multiple levels of physical hierarchy, which can contain a mix of multiply-instantiated blocks (MIBs), black boxes, and partial netlists.

OBJECTIVES

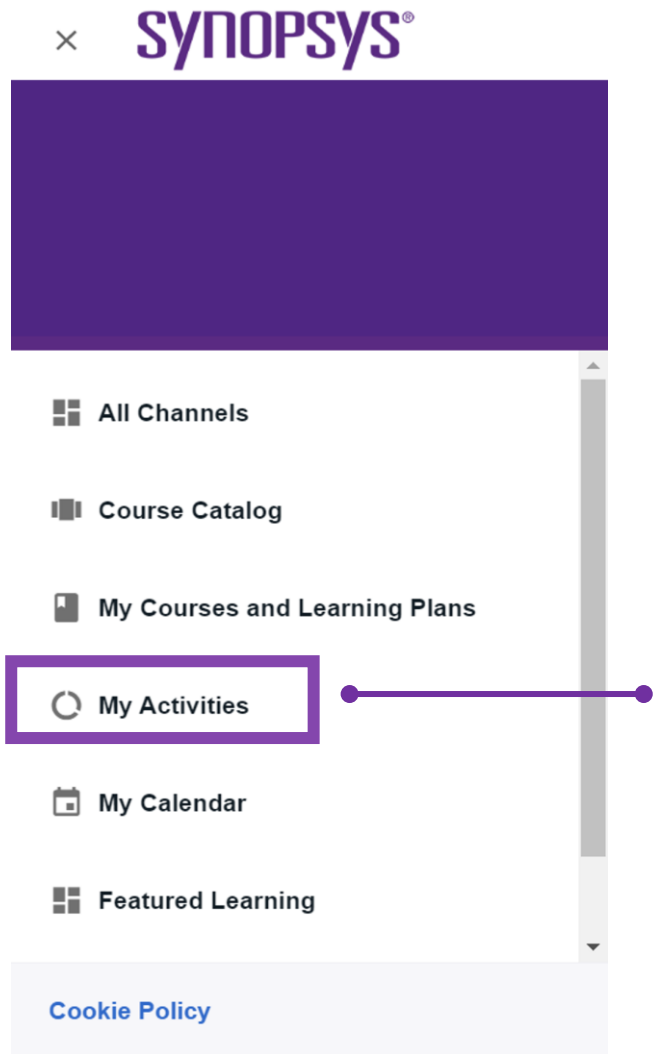
At the end of this course you should be able to:

- Create an NDM design library
- Read the Verilog outlines
- Initialize the chip-level floorplan
- Place the flip-chip bumps
- Place the Signal IO drivers/pads
- Explore the physical design hierarchy

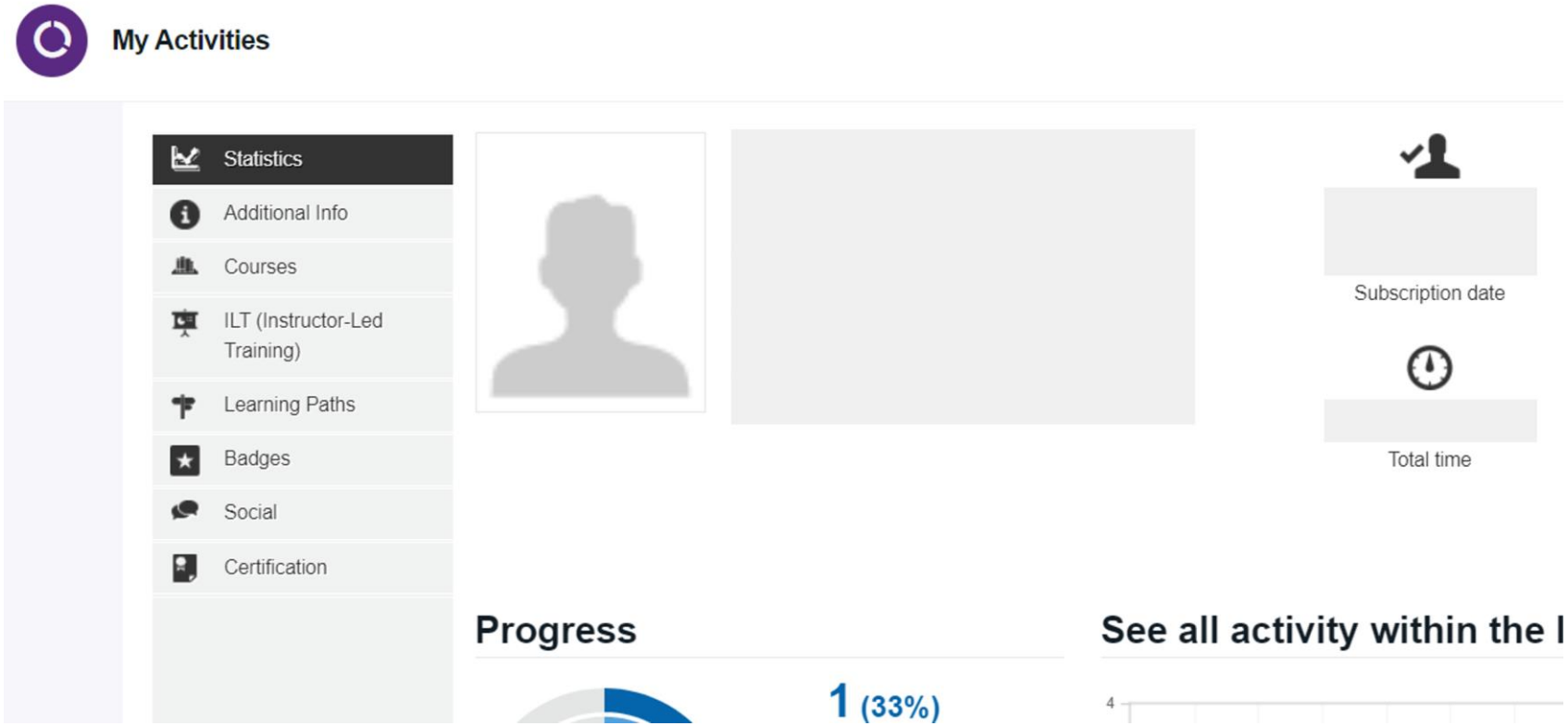
06 Click on “My Courses and Learning Plan”



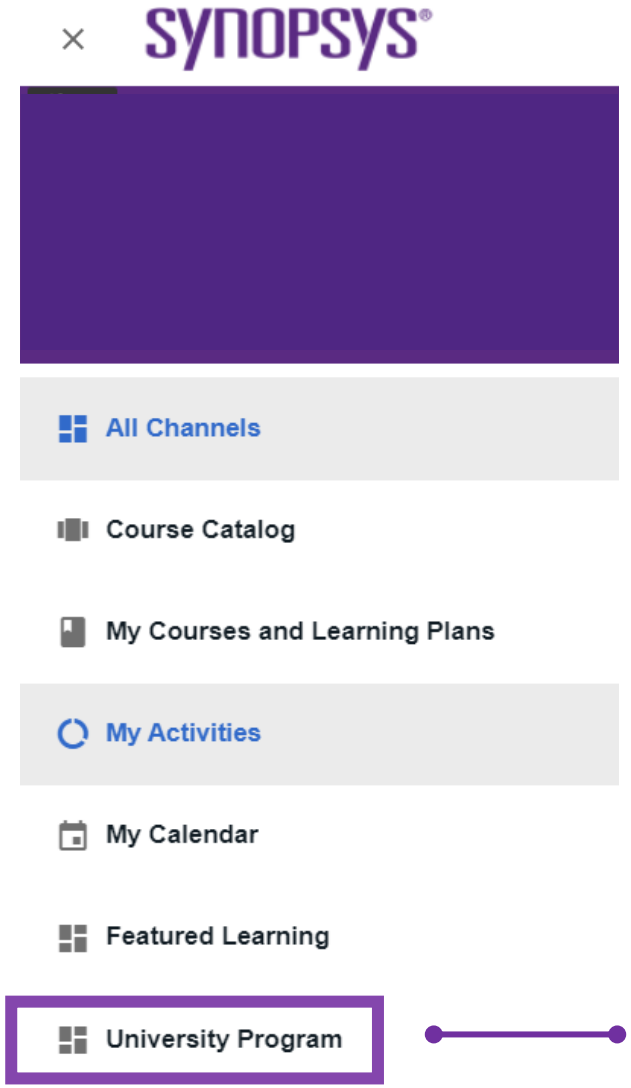
07 Click on “My Activities”



(*Your information, performance, badges, certification, etc. will be shown here.)

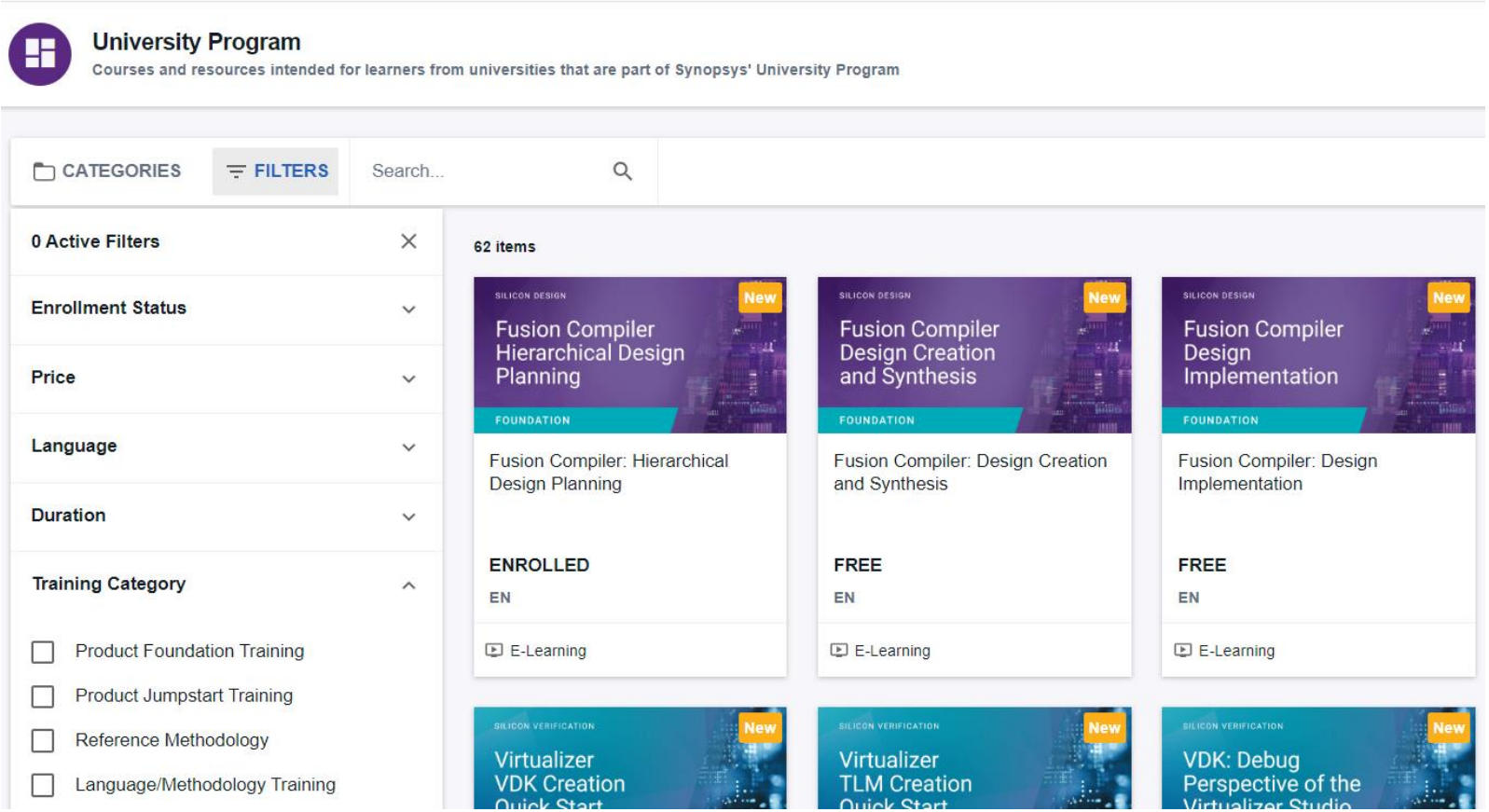


08 Click on “University Program”



Academic users approved by Synopsys University Program (TW) are entitled to the “Elite” subscription model.

More details for the subscription model (Link).



09 Synopsys Learning Paths

Custom Compiler Learning Path **Analog Designer**

Course 1	Course 2	Course 3	Course 4	Course 5
CC: Foundation I	CC: Schematic Entry	PrimeWave Jumpstart	PrimeWave & PrimeSIM SPICE Analog Tutorial	CC: Reliability
Custom Compiler Overview	Capturing Schematics	Testbench Setup	OP, DC, Tran Analysis	PrimeSim ResCheck Analysis
Library Manager	Using Advanced Editing features	Parametric Analysis	Loop Stability Analysis	PrimeSim EMIR Reliability Analysis
Data I/0	Generating Symbols	Corner Analysis	Noise Analysis	In-Design EM Aware Layout Implementation
Technology	Schematic Entry	Monte Carlo Analysis	Transient Analysis	In-Design Capacitance Reporting
Design Review Assistant	Advanced Schematic Editing	Dynamic Device Checks	Transient Noise Analysis	In-Design Resistance Checking and Reporting
Unified Constraint Management	Symbol Creation		S-parameter Analysis	Partial Layout Extraction (needs CC Elite license)
	Design Hierarchy		SOA	Layout Dependent Effects
	Working with Text Views		Transient + Monte Carlo Analysis	Voltage Dependent Rule Check
	Parameterized Connections		MOSRA	
	Schematic Overlays			
	Using Estimated Parasitic			

Legend
- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge

IC Compiler II Learning Path

Course 1	Course 2	
ICCII: Jumpstart	ICCII: Block Level Implementation	
Introduction	GUI Usage (lab)	Signoff
Design/Timing Setup	Objects, Attributes, Application Options	
NDMs/CLIBS	Floorplanning	
Floorplan	Placement	
Placement & Optimization	NDM Cell Libraries	
Clock Tree Synthesis	Design Setup	
Routing	Timing Setup	
Top Level Synthesis	Setting up CTS	
Design Implementation	Running CTS (CCD+classic flow)	
	Routing	
	Routing DRC	
	Via Ladder	
	Post-route Optimization	
	Top Level Implementation	

Learning Paths are available on Synopsys Learning Center.
-> Explore more Synopsys Learning Paths (Link)

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Silicon to Software™

Thank You

Synopsys University Program
(chunhsu@synopsys.com)