

A Quick Guide to Synopsys University Program Resources

Courseware, SolvNetPlus & Synopsys Learning Center

University Program, Synopsys Taiwan
June 2022



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Contents

- Membership Benefit
- Teaching Resources
 - courseware, generic libraries, PDKs
- Knowledge Base
 - SolvNetPlus
 - Synopsys Learning Center

Contents

- **Membership Benefit**
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Membership Benefits



IC Design and EDA Curriculum:

- Full Semester Courses – **80+ courses** for Bachelor and Master programs
- Workshops/Lectures - **30 courses**
- Short Lectures/Labs - **28 courses**

Teaching Support:

- **32/28nm & 90nm** Generic Libraries and iPDK's
- Generic Memory Compiler



Access Synopsys knowledge base:

- **Document** – contains product release note, installation guide, user guide & reference manual
- **Search** – provides an advanced search engine to retrieve information from various sources, such as documentation, articles, training, and so on.
- **Training** – Access **Synopsys Learning Center** for free self-paced training resources. The approved academic users are entitled to the **“Elite”** subscription model. Find more details [here](#).

*Requires SolvNetPlus account to access above-mentioned resources.

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Teaching Resources



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- Generic Memory Compiler

👉 Access through:

www.synopsys.com/community/university-program.html

SYNOPSYS®

SILICON DESIGN & VERIFICATION

SILICON IP

SOFTWARE INTEGRITY

ABOUT US

Support ▼

Global Sites ▼

Q

Home ▼

Community ▼

University Program ▼

Electronic Design University Program



"Access to Synopsys' leading-edge design software enables our engineering students to learn in the same environment as their industry counterparts, increasing the value of the student experience and research at Purdue University." - Dr. Mark C. Johnson, Purdue University

Education for Smart, Secure Everything

Through our Electronic Design University Program we aim to inspire and foster the world's next generation of technologists and innovators by providing academic and research institutions with access to the EDA tools and technology needed to prepare highly-skilled graduates ready to work in the world of Smart, Secure Everything. Membership in the program includes access to leading-edge EDA software, technical support, curriculum, and more.

EXPLORE EMBARC

The embARC Community is a free online resource for developers of embedded applications for ARC processors.

ARC DEVELOPMENT KITS

Visit the DesignWare ARC product store to order your development kits and start designing today!

MEMBERS ONLY LOG IN

Access curricula and resource downloads (SolvNetPlus ID and password required)

Contact Us

Ask questions, request information, and inquire about membership in the Electronic Design Academic Program

Curriculum Programs

Courseware for Teaching IC Design with Synopsys Tools.

[Learn More](#)

Teaching Resources

Synopsys Generic Libraries, PDKs, and Memory Compiler

[Learn More](#)

Support & Training

Technical Support and Tool Training for Universities

[Learn More](#)

Teaching Resources

IC Design and EDA Curriculum



IC Design Courses

Bachelor

- Analog and Mixed-Signal IC Physical Design
- Analog Integrated Circuits
- Computer Architecture and Engineering
- Digital Integrated Circuits
- IC Design Flow
- IC Design Introduction
- IC Testing
- IC Synthesis and Optimization
- Introduction to Microelectronic Circuits
- IC Synthesis and Optimization
- Introduction to Semiconductor Devices
- Linear Algebra
- Logic Design
- Microprocessor Systems
- Numerical Methods
- Scripting Languages for Beginners
- Static Timing Analysis
- Synthesis and Optimization of Digital Integrated Circuits
- Technical Writing

Master

- Analog Modeling with Verilog-A
- ARC Processor-Based Embedded Programming
- Complex Functions
- Crosstalk and Noise
- Design for Test
- Design of Embedded Systems
- Design of Special I/O's
- Digital Signal Processing
- EDA Tools
- FPGA Prototyping
- IC Design for Thermal Issues
- IO Design
- Low Power Design
- Low Power Design with Synopsys 32/28nm Generic Library
- Mixed-Signal IC Design
- Modeling and Optimization of IC Interconnects
- Rad-hard IC Design
- RF IC Design
- Synopsys EDA Tool Flow for Front-End Digital IC Design
- Synopsys EDA Tool Flow for Back-End Digital IC Design
- Thermal and Electro-Thermal Simulation: Achievements and Trends

Short Lectures and Workshops

Short Lectures

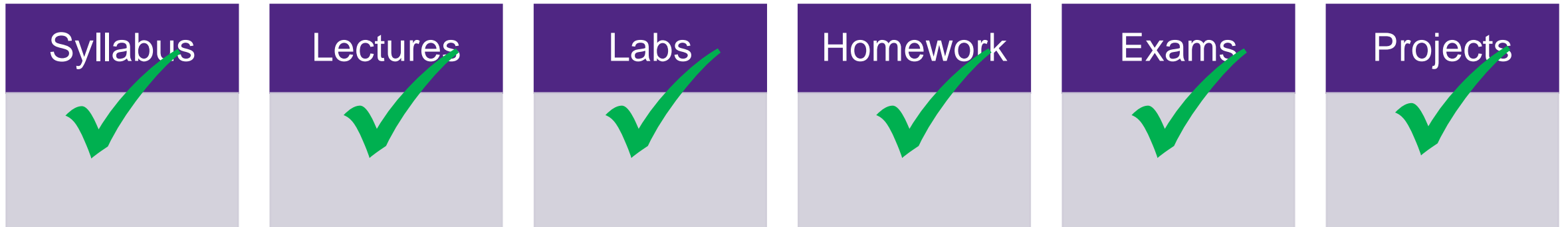
- Basic Perl Programming
- Characterization with SiliconSmart
- Circuit Simulation Transient Analysis
- Compiler Optimization and Code Generation
- Computer Networks
- Digital Design with Verilog
- Digital System Design and Simulation with VHDL
- Embedded Systems Design
- How to Create an Interoperable PDK
- IC Fabrication
- IC Simulation Theory
- Introduction to RF Communication
- Introduction to Verilog HDL
- Low Power Design w/Synopsys 32/28nm Generic Library
- Low Power Methodology Manual for 32/28nm
- Operational Research
- Optimization Methods
- Physical Verification Russet Development
- Power-Performance Optimization of Digital Circuits
- Process Variation Aware Design
- RF Circuits
- Scripting Languages
- Sequential Elements
- Signal and Power Integrity
- Statistical Techniques for Timing Analysis
- Subthreshold Design and Implementation
- Synthesizing OpenSPARC with 32/28nm EDK
- Techniques for Circuit Simulation
- User Interface Design
- Verification Methodology for Low Power

Workshops

- Advanced Design of Digital Circuits for Specific Applications
- ASIC Design Flow Tutorial Based on Synopsys 32/28nm Library
- ASIC Design Flow Tutorial Based on Synopsys 90nm Library
- Chip Design
- Computer Arithmetic Applied to High-Performance Cryptography
- Design for Testability
- Full Custom IC Design Flow with Synopsys Custom Tools
- Project Management
- Software Methodology Module for Custom Designer
- Synopsys Design Flow Tutorial
- Synopsys IC Design Flow Based on 90nm Generic Library
- SystemVerilog Verification Tutorial
- TCAD Course
- TCAD for VLSI Design
- TCAD Quick Start Guide
- TCAD Short Course
- Universal Verification Methodology

Full Semester Courses

- Topics cover all aspects of IC/SoC design
- Courseware for Bachelor and Master level programs
- Full-semester courses contain ~15 weeks of material and include the following components



Teaching Resources

Teaching Support (Generic Libraries, PDKs, Generic Memory Compiler)



Generic Libraries (EDK)

- 32/28nm and 90nm
- Enables students to master advanced design methods using the latest Synopsys EDA tools
- Includes:

Digital Standard Cell
Library

I/O Cell Library

I/O Special Cell
Library

Embedded Memories

Phase Locked Loop

Low Power Memories

Reference Designs

- Used by Synopsys for:

Curricula Development

To support development of laboratory works and course projects.

Customer Education

To train customers with Leon3 and ORCA processors' design.

Global Technical Services

To train internal staff and customers on Synopsys tools and low power flows.

Application Consultants

To develop and test sample designs and Reference Methodology scripts.

Interoperable Process Design Kits (iPDKs)

- 32/28nm and 90nm
- Enables students to master AMS/Custom design with the Synopsys custom implementation tool suite
- Includes:

Technology Files

Parasitic Extraction
Files

Symbol Library and
Python PCells

Embedded Memories

Physical Verification
Files

HSPICE Models

Callback Scripts

Setup Files

Curricula Development

To support development of laboratory works and course projects.

Customer Education

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Application Consultants

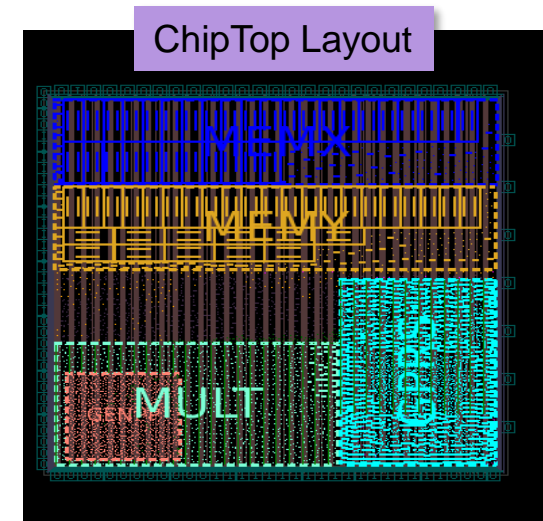
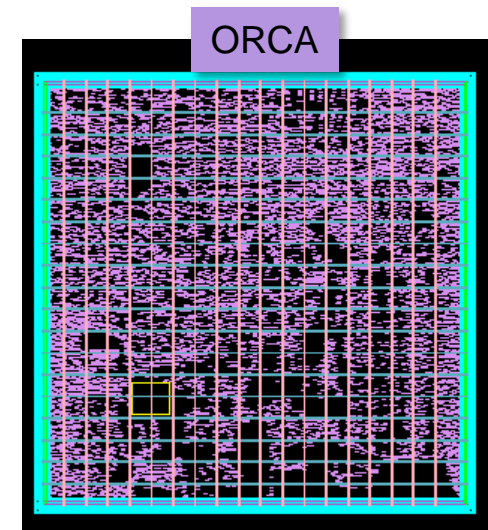
To develop and test sample designs and Reference Methodology scripts.

Reference Designs Supported by Synopsys EDKs

- **DesignWare® ARC 600 Academic Core** - 32-bit RISC processor core optimized for embedded applications and DSP tasks
- **ARM® Cortex® - M0 DesignStart™ Processor** - Entry-level configuration of ARM Cortex-M0 microprocessor¹
- **OpenSPARC T1** - 64-bit multicore processor²
- **LEON3** - 32-bit embedded processor²
- **Sample Processor Designs** - included in EDK
 - ORCA for timing analysis
 - ChipTop for low power design

1. Available through ARM DesignStart for Processor IP portal

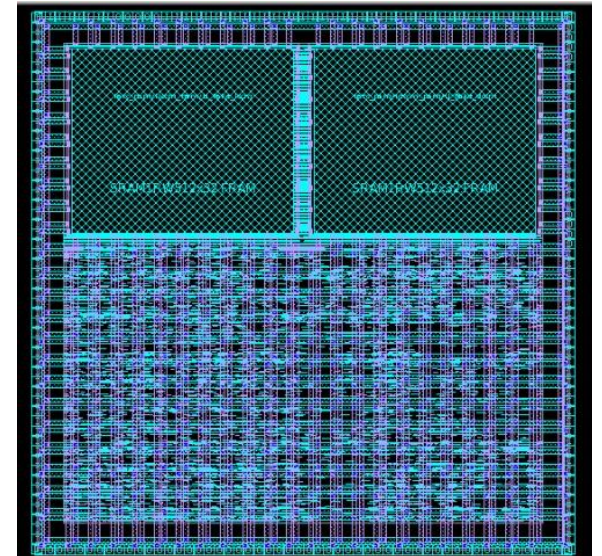
2. Available via GNU General Public License



DesignWare ARC 600 Processor Design

- Synthesis scripts optimized for 32/28nm EDK that can be used to easily redesign the academic version of the ARC 600 processor
- Synopsys curriculum for the ARC 600
 - IC Synthesis Based on DesignWare ARC 600 Core, includes:
 - Lecture slides
 - Covers ARC 600 details and EDA tool use
 - Laboratory works
 - Step-by-step guide of the ARC 600 design process

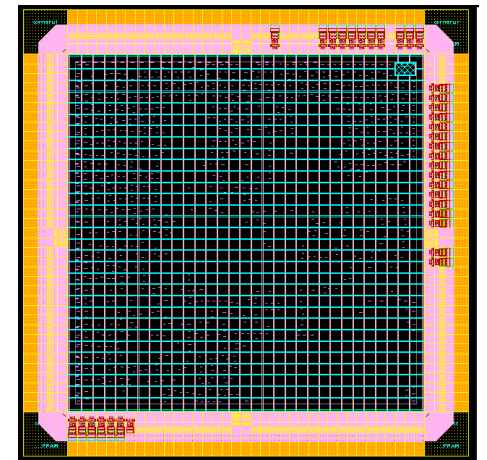
Apply in Members Only for access to the DesignWare ARC 600 Academic Core:
<https://www.synopsys.com/apps/protected/university/members.html>



ARM Cortex-M0 DesignStart Processor Design

- Complete Synthesizable Solution
 - Pre-configured Verilog netlist derived from commercial Cortex-M0 processor
 - Simple testbench
 - Example test code
- Scripts to implement the ARM Cortex-M0 DesignStart design using Synopsys 32/28nm EDK and EDA tools
- Synopsys curriculum for the ARM Cortex-M0
 - IC Synthesis Based on ARM Cortex-M0 DesignStart Processor

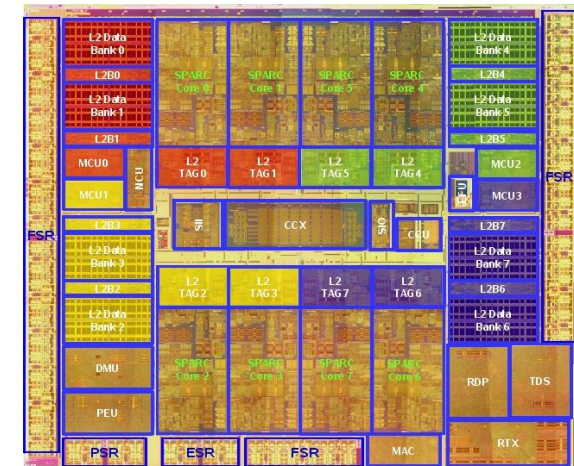
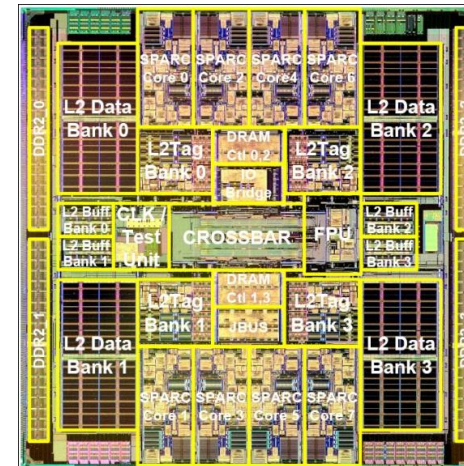
Download from ARM DesignStart for Processor IP portal:
<http://arm.com/products/processors/designstart-processor-ip>



OpenSPARC Processor Design

- Scripts to enable OpenSPARC design using Synopsys 32/28nm EDK and Design Compiler
- Implemented low power design techniques
- Synopsys curriculum for OpenSPARC
 - Computer Architecture
 - Includes:
 - Physical design scripts for IC Compiler
 - Scripts to enable small block reuse for educational purposes
 - Various lab projects based on small blocks

Download OpenSPARC:
<http://www.opensparc.net>



Synopsys Generic Memory Compiler

- Configurable software that automatically generates static RAM circuits of different types and sizes with all required deliverables
- Generate custom memory instances for educational ICs
- Designed for use with Synopsys EDKs and EDA tools
- Optimized for the Synopsys Digital Design Flow
- Supports multiple technologies (90nm, 32/28nm, etc.)

User interface

- Command line
- GUI

Supported memory types

- 1 port SRAM
- 2 port SRAM
- 1 port Low Power SRAM
- 2 port Low Power SRAM

*“Using the Synopsys Generic Memory Compiler in our complex processor for DSP application was a **great time-saving tool**. It helped the students generate the SRAM they wanted in a snap, saving them critical time to concentrate on the rest of the complex design.”*

Dr. Maged Ghoneima, American University in Cairo

Get started w/ Teaching Resources

[Link: www.synopsys.com/community/university-program.html](http://www.synopsys.com/community/university-program.html)

01 Go to Electronic University Program website

Select the Teaching Resources that you need, then click on “Members Only website”.

Curriculum [Link: www.synopsys.com/community/university-program.html](http://www.synopsys.com/community/university-program.html)

Synopsys provides universities with access to comprehensive curricula for Bachelor and Master Programs in IC design and EDA development.

Each full-semester course contains 15 weeks of material including syllabus, lectures, labs, homework and exams. Synopsys tools are applied in the labs for a thorough and practical understanding of theoretical concepts introduced in each course. Professors at member universities may use these course materials to implement a new course or to supplement content in an existing course.

All courseware described below may be downloaded from the Synopsys Electronic Design University Program **Members Only website** (requires SolvNet ID and password). If your university is not yet a member of the Synopsys Electronic Design University Program and you would like to apply, please [contact us](#).

Full Semester Courseware

VLSI Design Curriculum

Bachelor Degree Courses:

- Analog and Mixed-Signal IC Physical Design
- Analog Integrated Circuits
- Computer Architecture and Engineering
- Digital ASIC Design (NCSU)
- Digital Integrated Circuits
- IC Design Flow (RAU)
- IC Design Introduction
- IC Simulation Theory
- IC Testing
- Introduction to Logic Design (SU)
- Introduction to Microelectronic Circuits

Master Degree Courses:

- Analog Modeling with Verilog-A
- ARC Processor-Based Embedded Programming
- Complex Functions
- Crosstalk and Noise
- Design for Test
- Design of Embedded Systems
- Design of Special I/O's
- Digital Signal Processing
- Digital VLSI Design
- EDA Tools
- FPGA Prototyping

EXPLORE EMBARC

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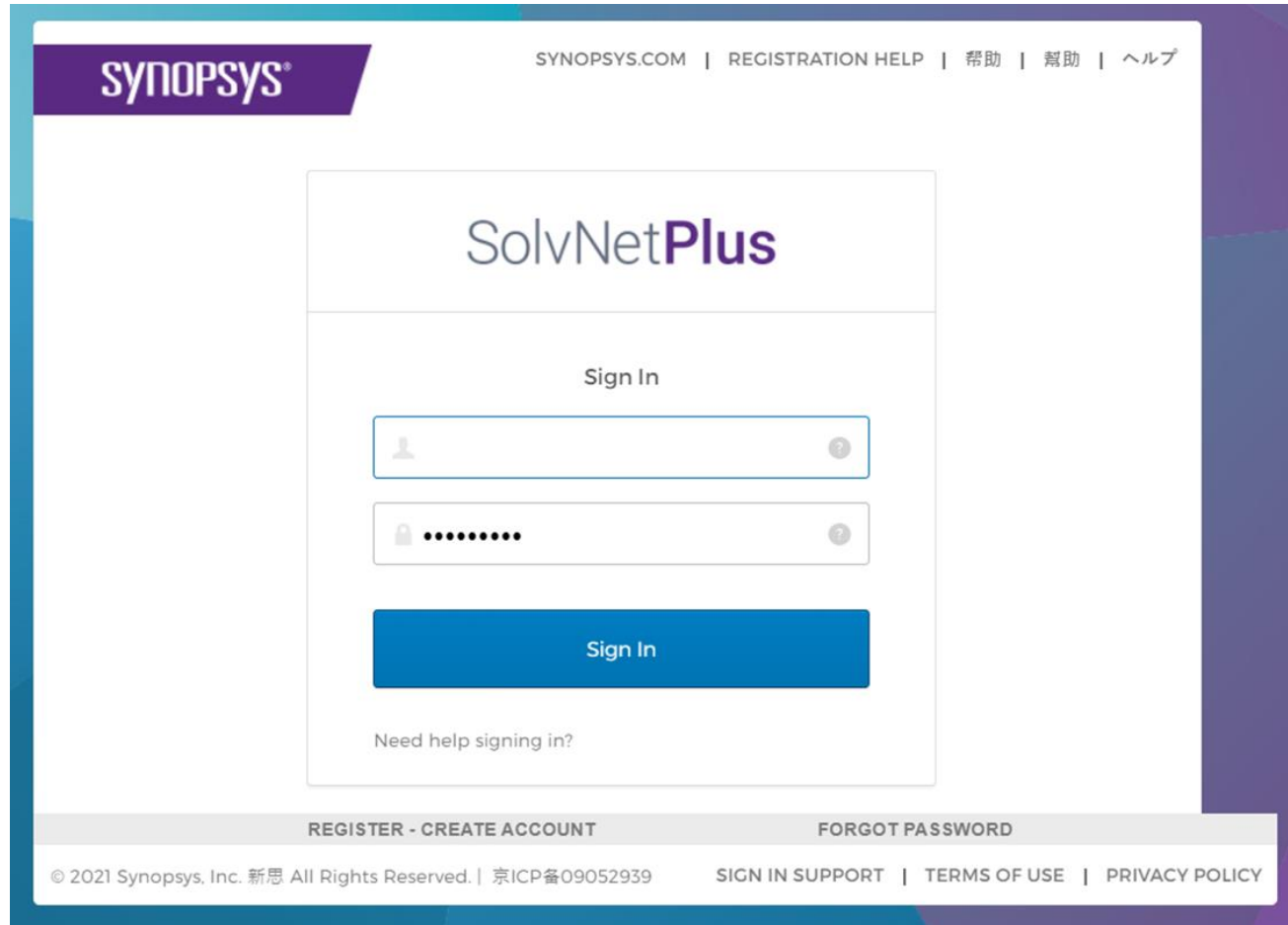
Access curricula and resource downloads (SolvNetPlus ID and password required)

Contact Us

Ask questions, request information, and inquire about membership in the Electronic Design Academic Program

- Requires a SolvNetPlus account to sign in.
- Please contact **Synopsys University Program – Taiwan** (chunhsu@synopsys.com) for membership enquiry.

02 Log-in with Synopsys SolvNetPlus credential



The screenshot shows the Synopsys SolvNetPlus login interface. At the top, the Synopsys logo is on the left, and navigation links for SYNOPSYS.COM, REGISTRATION HELP, and their Japanese equivalents are on the right. The main heading is 'SolvNetPlus'. Below it is a 'Sign In' section with two input fields: one for a username (indicated by a person icon) and one for a password (indicated by a lock icon and masked with dots). A blue 'Sign In' button is positioned below the fields. A link 'Need help signing in?' is located at the bottom of the sign-in box. At the bottom of the page, there are links for 'REGISTER - CREATE ACCOUNT' and 'FORGOT PASSWORD'. The footer contains copyright information for Synopsys, Inc. and links for 'SIGN IN SUPPORT', 'TERMS OF USE', and 'PRIVACY POLICY'.

<https://www.synopsys.com/apps/protected/university/members.html>

03 Insert course name in the search engine

Search by “Course Type”

[Home](#) / [Community](#) / [University Program](#) / [Members Only](#)

Members Only

Note: Use of the material downloaded from Members Only is subject to the terms and conditions of the End User License Agreement executed between your company and Synopsys. You can use the material at your site but you cannot distribute or publish it externally. Third party material located on this site is included with the permission of the owner (who retains all rights), and is provided solely for your convenience. Synopsys does not endorse and is not responsible for such third party content, and any use of these materials should be conducted only with the permission of the owner.

Go to: [Curriculum](#) | [Libraries](#) | [PDKs](#) | [Memory Compiler](#) | [Processor IP](#)

Curriculum

Synopsys provides universities with access to a comprehensive curriculum for Bachelor and Master Programs in microelectronic design and EDA development. Course materials can be used to implement a new course or to supplement content in an existing course. Search courses by keyword or course type to find and download courses quickly and easily.

Please report any errors or inconsistencies in these materials to our [University Program team](#).

Keyword Search:

More Search Options

Course Type:

Select Below

Course Category:

Select Below

Libraries

The Synopsys and automotive standard cell libraries are available for download from the Libraries Folder in [SolvNetPlus Electronic File Transfer \(EFT\)](#). Entitlements may not register at first log in and may require that you sign out and log back in to see the Libraries directory.

Full Semester

Short Lectures/Labs

Workshops/Lecturers

[ARC EM STARTER KIT](#)

The new ARC EM Starter Kit is now supported by the embARC Open Software Platform.

[MEMBERS ONLY LOG IN](#)

Access curricula and resource downloads (SolvNet ID and password required)

[Contact Us](#)

Ask questions, request information, and inquire about membership in the University Program

Course Type:

1. Full Semester
2. Short Lectures / Labs
3. Workshops / Lecturers

03 Insert course name in the search engine (cont.)

Search by “Course Category”

Example : Full Semester

More Search Options

Course Type: Full Semester

Course Category: ----- Select Below -----

Course Degree: ----- Select Below -----

Curriculum Type:

131 results were found

Advanced Design of Digital Integrated Circuits

The objective of this course is to study the design of digital integrated circuits for specific applications. The course covers the design of digital integrated circuits using VHDL and Verilog. The course also covers the design of digital integrated circuits using logic synthesis and logic optimization. The course is designed for students who are interested in the design of digital integrated circuits.

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of digital design and explores in depth the advanced techniques used by design professionals. These techniques involve ways of dealing with complex systems, ways to create faster systems, methodologies for design verification and evaluation of results. The course covers and compares the use of VHDL and Verilog, and the impact of coding style on final results. Note: This course can be used with permission from the 3rd party owner. All rights reserved.

> [Lectures](#) (18 MB)

Advanced Methods in Logic Synthesis and Equivalence Checking

The goal of the course is to study logic synthesis problem, logic optimization as well as advanced methods in synthesis. The course also focuses on logic design components and combinational and sequential equivalent checking.

> [Syllabus](#) (88.0 KB)

> [Lectures](#) (3,135,241 bytes)

> [Labs](#) (657 KB)

> [Homework](#) (263 KB)

> [Labs & Homework](#) (441 KB)

Course Category:

1. Analog / RF Design
2. Digital System Architecture and Design
3. IC / Semiconductor Fabrication
4. Other

03 Insert course name in the search engine (cont.)

Search by “Curriculum Type”

Example : Full Semester

Keyword Search:

search

view all

More Search Options

Course Type: Full Semester

Course Category: ----- Select Below -----

Course Degree: ----- Select Below -----

Curriculum Type: ----- Select Below -----

131 results were found

Advanced Design of

The objective of this course is to provide students with the knowledge and skills required to design and develop digital integrated circuits for specific applications.

be used by students of this course to develop their knowledge in this area. The course reviews basic concepts of digital design and explores in depth the advanced techniques used by design professionals. These techniques involve ways of dealing with complex systems, ways to create faster systems, methodologies for design verification and evaluation of results. The course covers and compares the use of VHDL and Verilog, and the impact of coding style on final results. Note: This course can be used with permission from the 3rd party owner. All rights reserved.

> [Lectures](#) (18 MB)

Curriculum Type:

1. EDA
2. VLSI

04 Access to the courseware

Start to download course syllabus, lecturer slides, labs or exams

Example : Full Semester

Keyword Search:

search

view all

More Search Options

Course Type:

Course Category:

49 results were found under 'Full Semester' Course Type, 'VLSI' Curriculum Type.

Analog and Mixed-Signal IC Physical Design

This course covers the basics of IC design, custom design flows. The course mainly focuses on data of analog and mixed-signal IC physical design.

- > [Syllabus](#) (90 KB)
- > [Lectures](#) (4.6 MB)
- > [Labs](#) (1.6 MB)
- > [Homework & Exams](#) (244 KB)

Analog Integrated Circuits

The goal of the course is to study principles of design, analysis and simulation of analog integrated circuits. The course also focuses on variants, parameter improvement methods, parameters analysis of different basic analog circuits: differential and operational amplifiers, switched capacitor circuits, oscillators, phase locked loops, data converters, secondary power sources, etc.

- > [Syllabus](#) (42 KB)
- > [Lectures](#) (17 MB)
- > [Labs](#) (12 MB)
- > [Project](#) (663 KB)
- > [Homework & Exams](#) (480 KB)

Course Contents:

1. Syllabus
2. Lectures
3. Labs
4. Project
5. Homework & Exams

Contents

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- Teaching Resources
 - courseware, generic libraries, PDKs
- **Knowledge Base**
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Knowledge Base

Knowledge
Base
知識庫



Access Synopsys knowledge base:

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👉 Access through:
<https://solvnetsynopsys.com/>



Welcome to the Synopsys Support Community!

Legacy Docs Search is now integrated with the generic search window



Needing My Response My Open Cases My Open STARS

Cases (0)							
VIEW	CASE NUMBER	CASE STATUS	SUBJECT	PRODUCT L1	PRODUCT L2	LICENSED PRODUCT	CASE SEVERITY
No data returned							

GETTING STARTED

SYNOPSYS
SolvNetPlus

Get Oriented with SolvNetPlus

University users can access Documentation, Training & Search ; but CANNOT access Download, EFT, Cases & STARs.

The screenshot shows the Synopsys SolvNetPlus interface. A blue box with a checkmark highlights the search bar. A red 'X' in a circle is placed over the 'Cases' and 'STARs' links in the navigation bar. Below the navigation bar, four tiles are shown: 'Documentation' (checkmark), 'Training' (checkmark), 'Downloads' (red X), and 'EFT (Electronic File Transfer)' (red X). At the bottom left, a table titled 'Cases (0)' is shown with columns: VIEW, CASE NUMBER, CASE STATUS, SUBJECT, PRODUCT L1, PRODUCT L2, LICENSED PRODUCT, CASE SEVERITY, and SITE. The table contains the text 'No data returned'. At the bottom right, the 'GETTING STARTED' section is visible with the Synopsys SolvNetPlus logo.

synopsys® | SolvNetPlus

Anna Hsu

Home Cases STARs Articles Help

Welcome to the Synopsys Support Community!
Legacy Docs Search is now integrated with the generic search window

Documentation

Training

Downloads

EFT (Electronic File Transfer)

Needing My Response My Open Cases My Open STARs

Cases (0)

VIEW	CASE NUMBER	CASE STATUS	SUBJECT	PRODUCT L1	PRODUCT L2	LICENSED PRODUCT	CASE SEVERITY	SITE
No data returned								

GETTING STARTED

synopsys®
SolvNetPlus

Knowledge Base

SolvNetPlus (Documentation & Search)

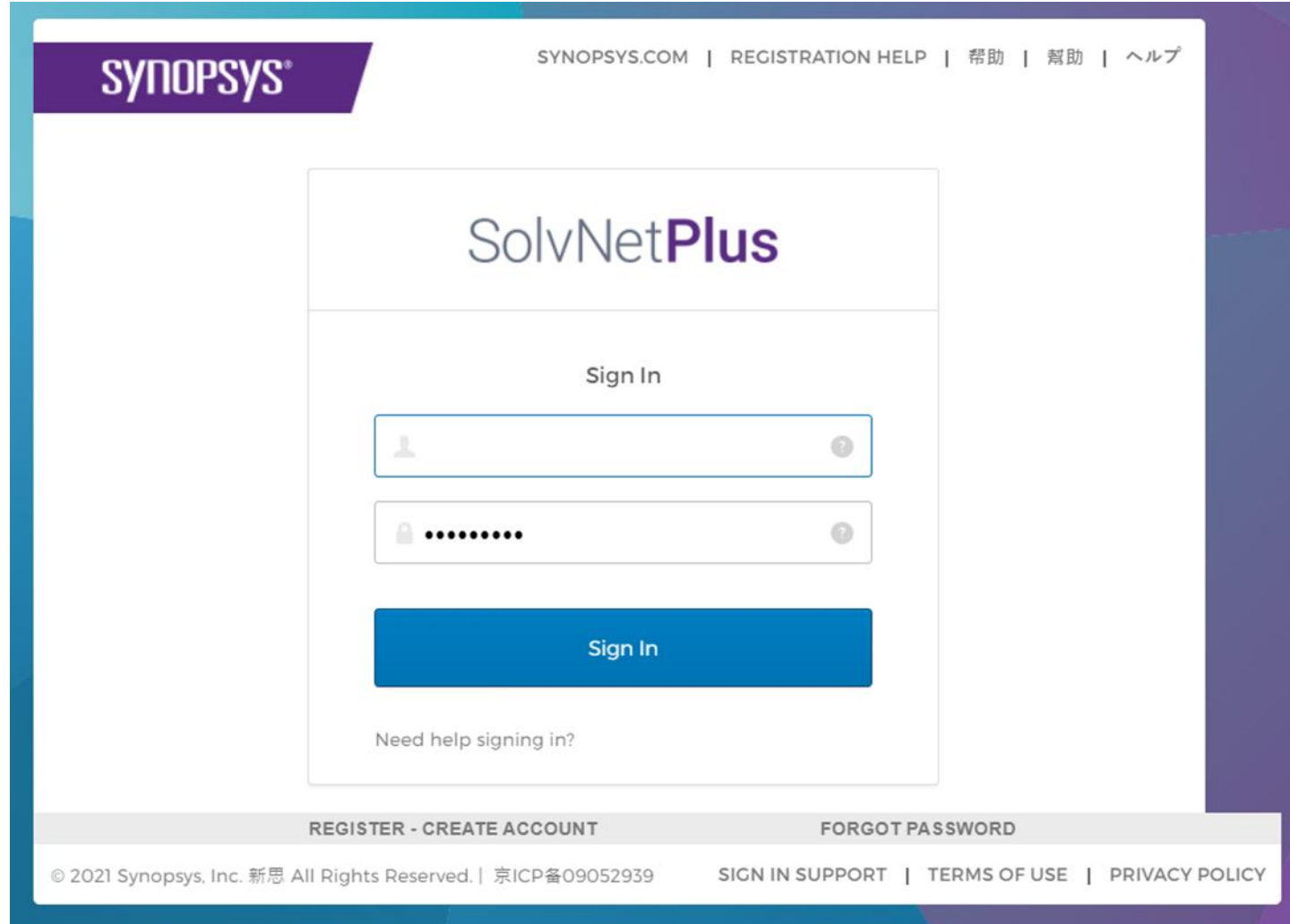


Get started w/ SolvNetPlus

<https://solvnetplus.synopsys.com/>



01 Log-in with Synopsys SolvNetPlus credential



The screenshot shows the Synopsys SolvNetPlus login interface. At the top, the Synopsys logo is on the left, and navigation links for SYNOPSYS.COM, REGISTRATION HELP, and help in Chinese and Japanese are on the right. The main content area features the SolvNetPlus logo, a 'Sign In' heading, and two input fields for username and password. Below the password field is a blue 'Sign In' button. A link for 'Need help signing in?' is positioned below the button. At the bottom of the main area, there are links for 'REGISTER - CREATE ACCOUNT' and 'FORGOT PASSWORD'. The footer contains copyright information for 2021 Synopsys, Inc., a Chinese ICP license number, and links for 'SIGN IN SUPPORT', 'TERMS OF USE', and 'PRIVACY POLICY'.

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SYNOPSYS.COM | REGISTRATION HELP | 帮助 | 帮助 | ヘルプ

SolvNetPlus

Sign In

Sign In

Need help signing in?

REGISTER - CREATE ACCOUNT

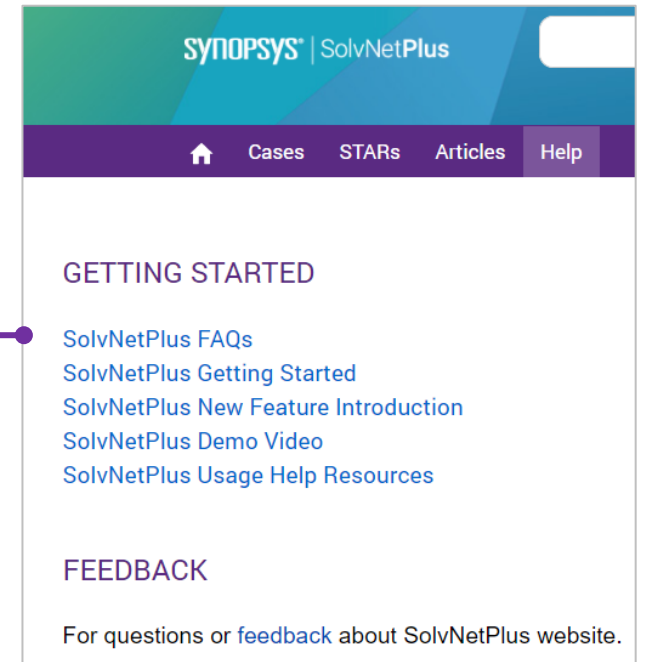
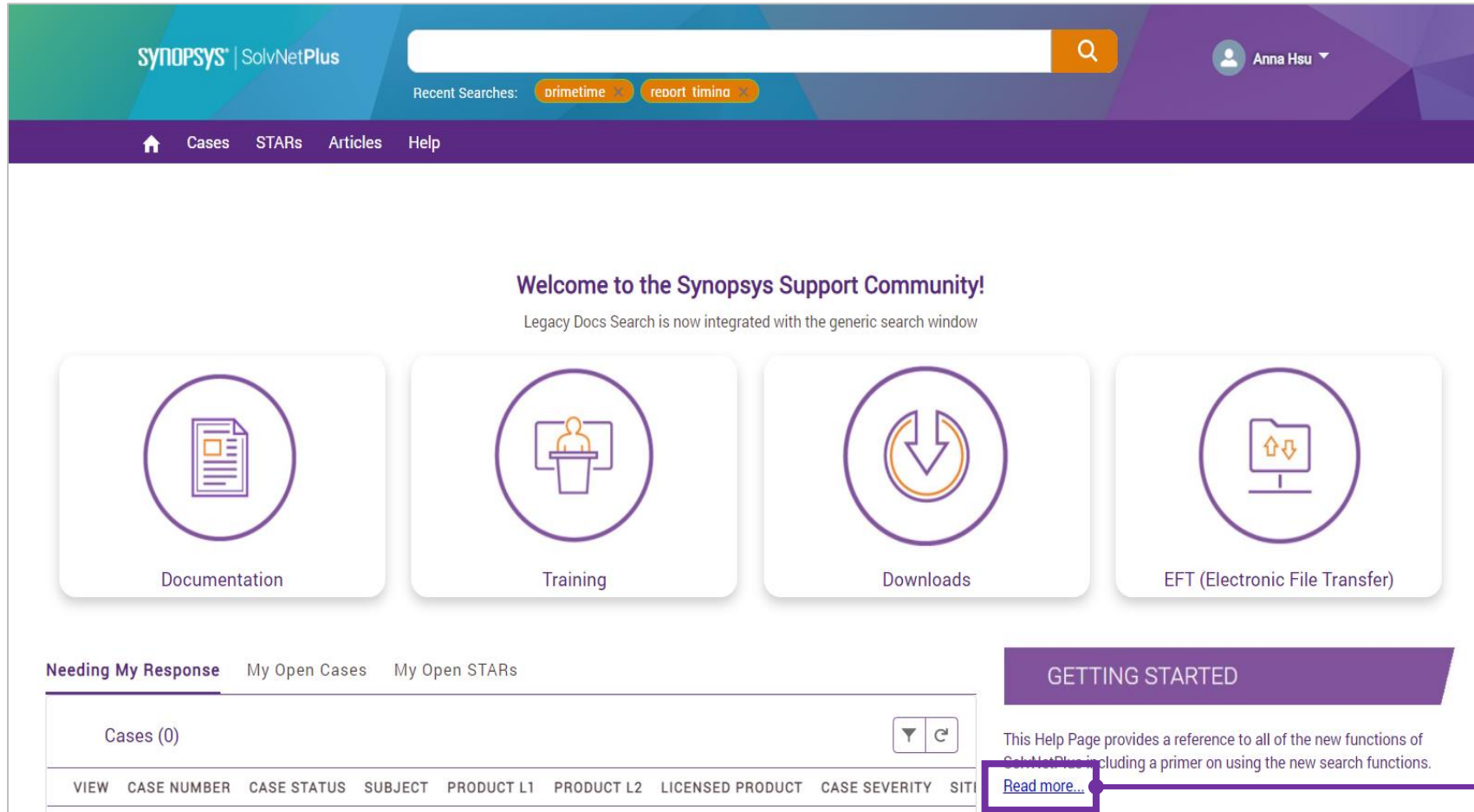
FORGOT PASSWORD

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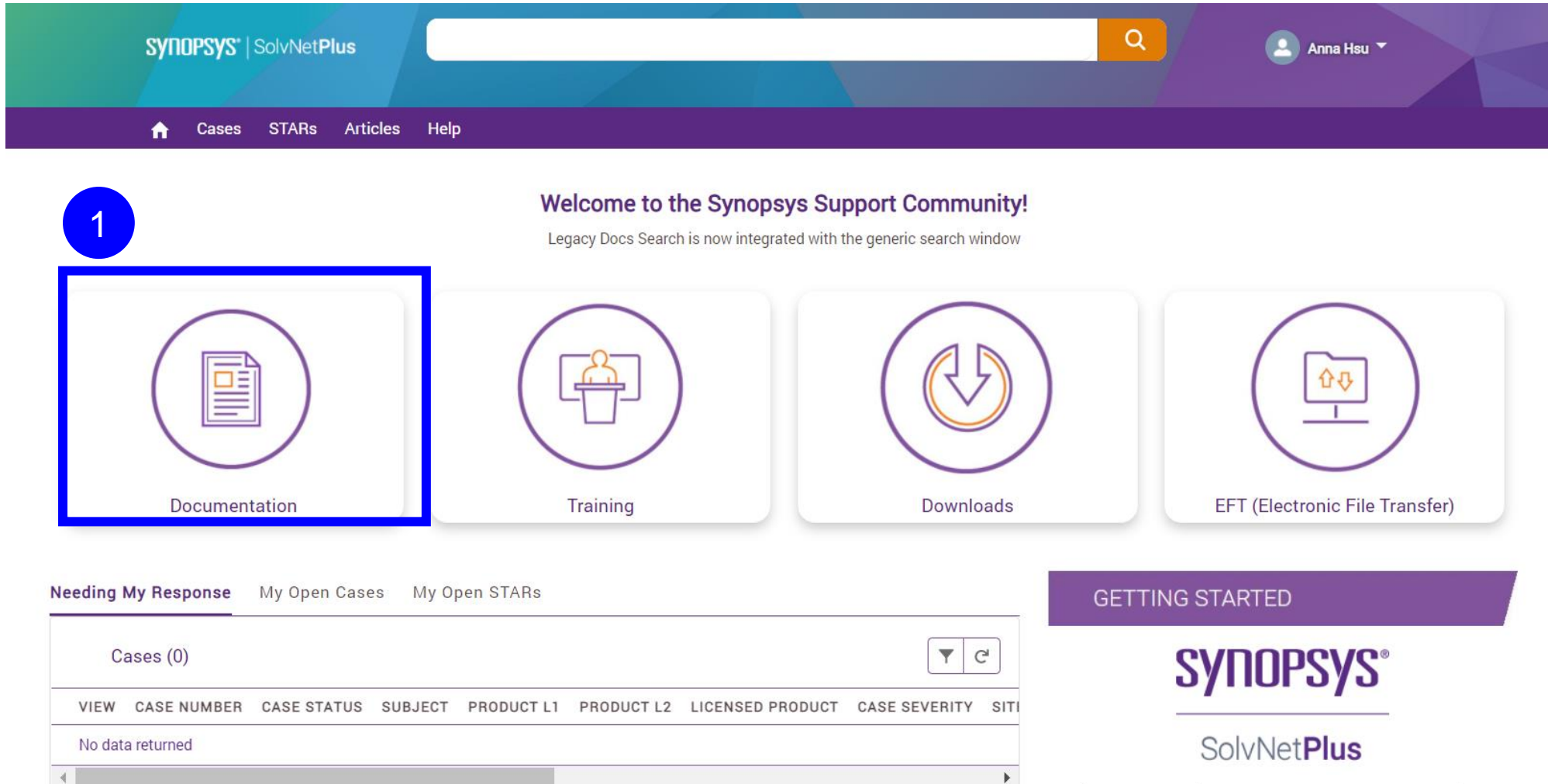
SIGN IN SUPPORT | TERMS OF USE | PRIVACY POLICY

<https://solvnet.synopsys.com/>

02 Read “GETTING STARTED” before use

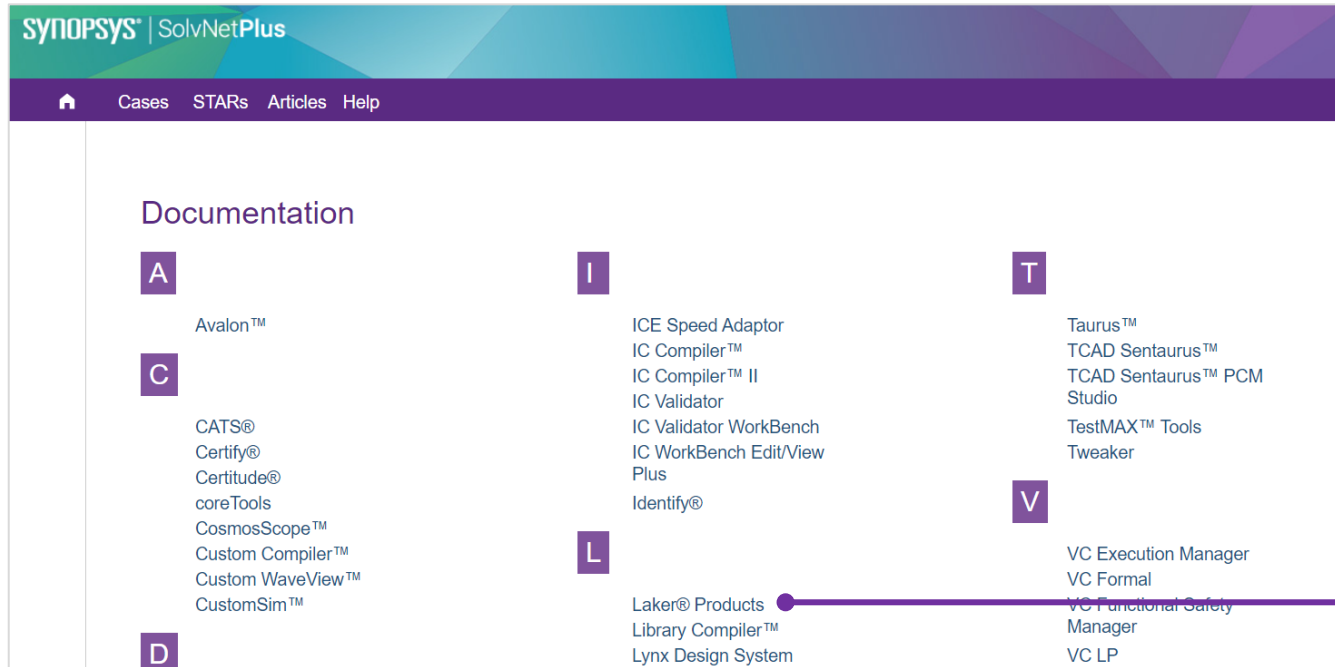


03 Click on “Documentation”



04 Search by product name to get tool documents

You can download release notes, installation guides & user guides and reference manuals from this section



Example : Laker

Laker

Laker3, L-2018.06, June 2018

- [Laker3 Installation Guide](#)
- [Laker3 Quick Start Guide for Laker3 User Interface, K-2015.06, June 2015](#)
- [Laker3 Command Reference Manual, K-2015.06, June 2015](#)
- [Laker3 Tcl Reference Manual, K-2015.06, June 2015](#)
- [Laker3 Bind Key Summary](#)
- [Laker3 Menu Summary](#)
- [Laker DRD Tcl Command Reference, K-2015.06, June 2015](#)
- [Laker CDPR LEF/DEF Tutorial, 2013.02, February 2013](#)
- [Laker CDPR Data Preparation and SDL Tutorial, 2013.02, February 2013](#)
- [Laker3 Release Notes Version, L-2018.06-SP1 \(January 2019\)](#)

Laker, 2020.03, March 2020

- [Laker User Guide and Tutorial, 2015.03](#)
- [Laker Command Reference, 2015.12](#)
- [Laker Tcl Reference, 2015.12](#)
- [Laker Bind Key Summary, 2015.12](#)
- [Laker Command Index, 2015.12](#)

05 Look for information in the “Search” bar

You can use search to retrieve information from various sources

2

report_timing

×

Q

Recent Searches:

report timina

Anna Hsu

Home

Cases

STARs

Articles

Help

Welcome to the Synopsys Support Community!

Legacy Docs Search is now integrated with the generic search window

Documentation

Training

Downloads

EFT (Electronic File Transfer)

Needing My Response

My Open Cases

My Open STARs

Cases (0)

▼

↺

VIEWCASE NUMBERCASE STATUSSUBJECTPRODUCT L1PRODUCT L2LICENSED PRODUCTCASE SEVERITYSIT

No data returned

GETTING STARTED

Synopsys

SolvNetPlus

This Help Page provides a reference to all of the new functions of SolvNetPlus including a primer on using the new search functions.

06 Choose needed info from the displayed search results

The information will be displayed from various sources, such as documentation, articles, training, YouTube, and so on (but NOT in cases & STARs)

Example : insert “report_timing”

The screenshot displays the Synopsys SolvNetPlus search interface. At the top, a search bar contains the query "report_timing". Below the search bar, a navigation bar includes links for "Cases", "STARs", "Articles", and "Help". The main content area shows search results for "report_timing" in 3.11 seconds, with 11,604 results found. The results are categorized by source and product line (L1). The "Source" section lists "Docs - Silicon Tools" (11,133), "Articles" (333), "SNUG" (130), and "Docs - Silicon IP" (8). The "Product L1" section lists various products including PrimeShield, PrimeTime, Design Vision, DC Explorer, HDL Compiler, Power Compiler, Design Compiler, and PrimePower. The search results list includes a "report_timing Command" entry under "Docs - Silicon Tools" and a "Path Timing Report" entry under "Docs - Silicon Tools".

Source

- ☐ Docs - Silicon Tools (11,133)
- ☐ Articles (333)
- ☐ SNUG (130)
- ☐ Docs - Silicon IP (8)

Product L1

- ☐ PrimeShield (3,051)
- ☐ PrimeTime (3,203)
- ☐ Design Vision (1,782)
- ☐ DC Explorer (1,826)
- ☐ HDL Compiler (1,782)
- ☐ Power Compiler (1,783)
- ☐ Design Compiler (1,855)
- ☐ PrimePower (1,465)

+ Show more

Search Results 1-10 of 11,604 for **report_timing** in 3.11 seconds

Relevance Date

Docs - Silicon Tools

report_timing Command

... are here: Other Documents > Synopsys Timing Constraints and Optimization User Guide, version R-2020.09-SP2 > Timing Reports > **report_timing** Report Contents **report_timing** Command The **report_timing** command provides detailed, point-by-point timing information for the paths that have ... The **report_timing** command offers a large number of options to control the scope of ... prompt> **report_timing** -nworst 2 -max_paths 8 ... The **report_timing** command has several more options not described here.

Product L1: [Power Compiler](#), [HDL Compiler](#), [Design Vision](#), [DC Explorer](#), [Design Compiler](#)

Release: [2021.03](#)

[Details](#)

Docs - Silicon Tools

Path Timing Report

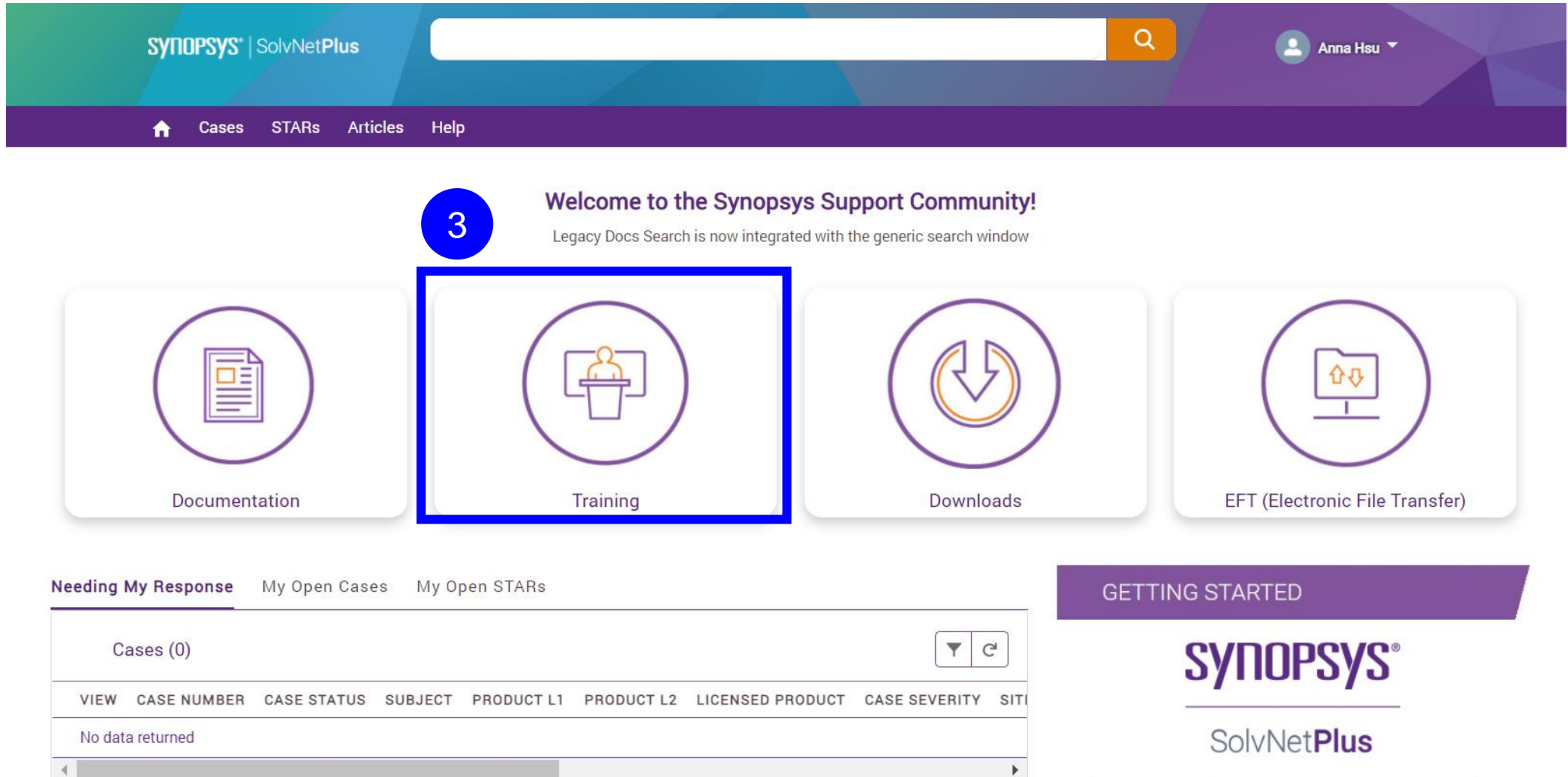
You are here: PrimeTime Suite Documents > PrimeTime User Guide, version R-2020.09-SP4 > Reporting and Debugging Analysis Results > Path Timing Report Path Timing Report You can use path timing reports to focus on particular timing violations and to determine the cause ... By default,

Knowledge Base

Synopsys Learning Center (Self-paced Learning)

1. Access via SolvNetPlus (<https://solvnet.synopsys.com/>)
2. Access via Synopsys Learning Center (<https://www.synopsys.com/support/training/self-paced.html>)

01 Login SolvNetPlus and click “Training”



02 SSO Login via SolvNetPlus

The screenshot shows the Synopsys Learning Center homepage. At the top, the Synopsys logo is on the left, and 'ENGLISH' and 'SIGN IN' are on the right. Below the logo, a 'Home' link is visible. A paragraph of text explains that subscriptions are active on the Synopsys Learning Center and provides information for university students. A 'Show more' link is present. A large 'Sign In' dialog box is centered on the screen, featuring a close button (X) in the top right corner. The dialog box contains the text: 'Click below to log in through SolvNetPlus. Alternatively, close this dialog box and browse through the list of available courses.' Below this text is a prominent orange button labeled 'SSO LOGIN VIA SOLVNETPLUS'. At the bottom of the dialog box, there are links for 'CATEGORIES' and 'FILTERS'. Below the dialog box, the page shows a section titled 'Instructor-Led Training' with a '1/4' indicator and navigation arrows. This section displays a row of course cards: 'VC SpyGlass Lint Overview', 'Signoff SiliconSmart', 'Signoff StarRC', 'Physical Implementation IC Compiler II', 'Language Training UPF Fundamentals', and 'Language Training System Verilog Assertions'.

SYNOPSYS®

ENGLISH ▾ SIGN IN

Home

Subscriptions are now active on Synopsys Learning Center. For more information on subscription models, see [Self-Paced Learning](#). Students from universities that are part of the [University Software Program](#) can select **University Program** from the User Menu on the top left

[Show more](#)

Sign In

Click below to log in through SolvNetPlus. Alternatively, close this dialog box and browse through the list of available courses.

SSO LOGIN VIA SOLVNETPLUS

CATEGORIES FILTERS

RDs ▾ NEWEST TO OLDEST ▾

1/4 < >

Instructor-Led Training

SILICON VERIFICATION
VC SpyGlass Lint Overview

SILICON DESIGN
Signoff
SiliconSmart

SILICON DESIGN
Signoff
StarRC

SILICON DESIGN
Physical Implementation
IC Compiler II

Language Training
UPF Fundamentals

Language Training
System Verilog Assertions

02 Access Synopsys Learning Center

The screenshot displays the Synopsys Learning Center interface. At the top, there is a navigation bar with the Synopsys logo, a search bar, and a notification icon. Below the navigation bar, the 'University Catalog' section is visible, featuring a grid of six course cards. Each card includes a title, a category (e.g., SILICON DESIGN, SILICON VERIFICATION), a 'New' badge, a description, a status (ENROLLED or FREE), and an 'E-Learning' icon. The 'TCAD Self-Paced Course Catalog' section is also visible, featuring a grid of six course cards with similar details. The interface includes pagination controls (1/4 and 1/2) and navigation arrows.

University Catalog
Courses for University Students

Course Title	Category	Status	E-Learning
Fusion Compiler Hierarchical Design Planning	SILICON DESIGN	ENROLLED	EN
Fusion Compiler Design Creation and Synthesis	SILICON DESIGN	FREE	EN
Fusion Compiler Design Implementation	SILICON DESIGN	FREE	EN
Formality Jump Start	SILICON DESIGN	FREE	EN
Virtualizer VDK Creation Quick Start	SILICON VERIFICATION	FREE	EN
Virtualizer TLM Creation Quick Start	SILICON VERIFICATION	FREE	EN

TCAD
Self-Paced Course Catalog

Course Title	Category	Status	E-Learning
TCAD Sentaurus	SILICON ENGINEERING	ENROLLED	EN
TCAD Sentaurus Sentaurus Visual	SILICON ENGINEERING	FREE	EN
TCAD Sentaurus Sentaurus Device	SILICON ENGINEERING	FREE	EN
TCAD Sentaurus Sentaurus Process Explorer	SILICON ENGINEERING	FREE	EN
TCAD Sentaurus Sentaurus Mesh	SILICON ENGINEERING	FREE	EN
TCAD Sentaurus Sentaurus Structure Editor	SILICON ENGINEERING	FREE	EN

✓ You can also directly access through: <https://training.synopsys.com/>

03 Click on “☰”

×

SYNOPSYS®

☰

All Channels

Course Catalog

My Courses and Learning Plans

My Activities

My Calendar

Featured Learning

Cookie Policy

☰

SYNOPSYS®

Search content in the platform

🔍

All Channels > Welcome

Subscriptions are now active on Synopsys Learning Center. For more information on subscription models, see [Self-Paced Learning](#). Students from universities that are part of the [University Softw](#) User Menu on the top left

[Show more](#)

☰ All Channels

FILTERS

Search...

🔍

👤 New invitation and subscriptions

This is all the new learning content selected for you

SILICON DESIGN

Not Started

Fusion Compiler Hierarchical Design Planning


FOUNDATION


Fusion Compiler: Hierarchical Design Planning


EN


E-Learning


04 Click on “Course Catalog”


 **SYNOPSYS®**


 All Channels

 **Course Catalog**

 My Courses and Learning Plans

 My Activities

 My Calendar

 Featured Learning

[Cookie Policy](#)

(*The courses are free to all users)



Course Catalog

All your courses and learning plans in which you're enrolled, including all your courses and learning plans in progress and already completed.

CATEGORIES

FILTERS
















Search...



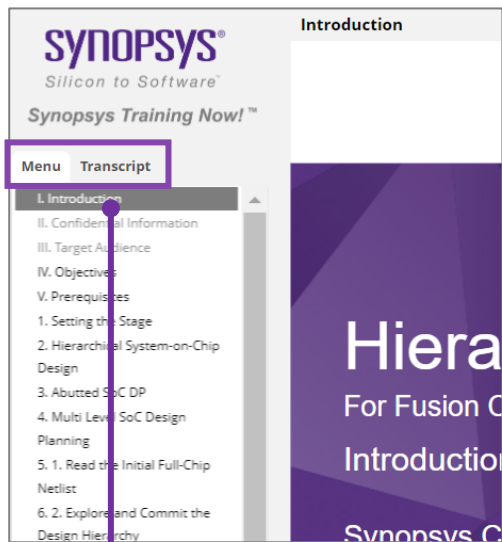
CARDS

Optical and Photonic Solutions

Courses for the Optical Solutions Group and Photonic Solutions

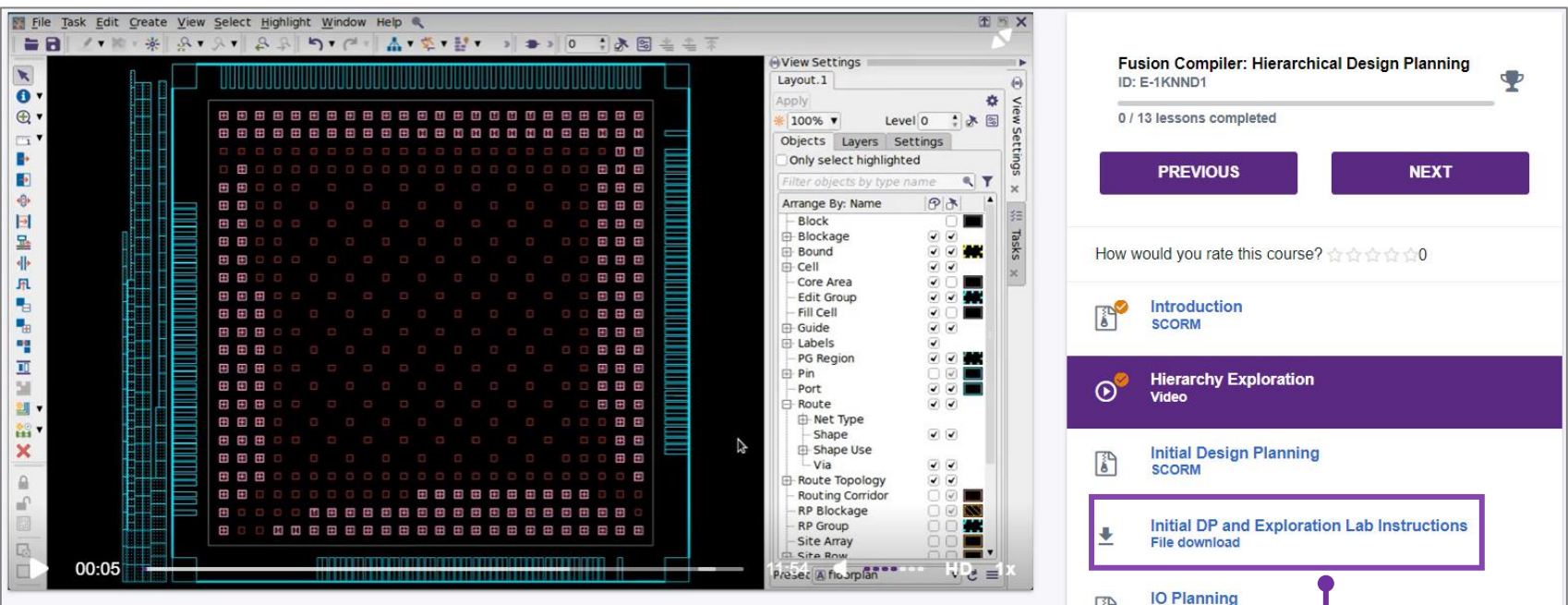
 	 	 	 	 
RSoft: 元件工具使用技巧 - Part I (May 2022 Tech Talk)	LightTools: Making Ray Files Work (User Group Webinar)	CODE V: Choose Glasses like a Pro with CODE V Glass Expert! (April 2022...)	LightTools: 2022.03 New Features (March 2022 Tech Talk)	CODE V Self-Guided Onboarding
FREE	FREE	ENROLLED	FREE	FREE
ZH 44m 00s	EN 35m 00s	EN 55m 00s	EN 45m 00s	EN 1h 15m
 E-Learning	 E-Learning	 E-Learning	 E-Learning	 E-Learning

05 The Interface of Courses



Menu and transcript are provided.

Scroll down to see course description, including abstract, objectives, audience profile, etc.



Course Description

ABSTRACT

In this hands-on course, you will use Fusion Compiler or IC Compiler II to create chip and block-level floorplans using a hierarchical (top-down) design planning approach. The focus is on multi-voltage (UPF) system-on-a-chip (SoC) designs with multiple levels of physical hierarchy, which can contain a mix of multiply-instantiated blocks (MIBs), black boxes, and partial netlists.

OBJECTIVES

At the end of this course you should be able to:

- Create an NDM design library
- Read the Verilog outlines
- Initialize the chip-level floorplan
- Place the flip-chip bumps
- Place the Signal IO drivers/pads
- Explore the physical design hierarchy

Downloadable files/instructions

06 Click on “My Courses and Learning Plan”

×

SYNOPSYS®

☐ All Channels

☐ Course Catalog

☐ My Courses and Learning Plans

🔄 My Activities

📅 My Calendar

☐ Featured Learning

[Cookie Policy](#)

(*All of your courses will be shown here.)

My Courses and Learning Plans
All of your courses and learning plans in which you're enrolled, including all of your courses in progress and already completed.

FILTERS

Search...

🔍

3 items

SILICON DESIGN

Not Started

Fusion Compiler Hierarchical Design Planning

FOUNDATION

Fusion Compiler: Hierarchical Design Planning

EN

E-Learning

OPTICAL SOLUTIONS

In Progress

CODE V

CODE V: Choose Glasses like a Pro with CODE V Glass Expert! (April 2022...

EN | 55m 00s

E-Learning

SILICON DESIGN

Completed

Physical Implementation

IC Compiler II

QUICK TIP

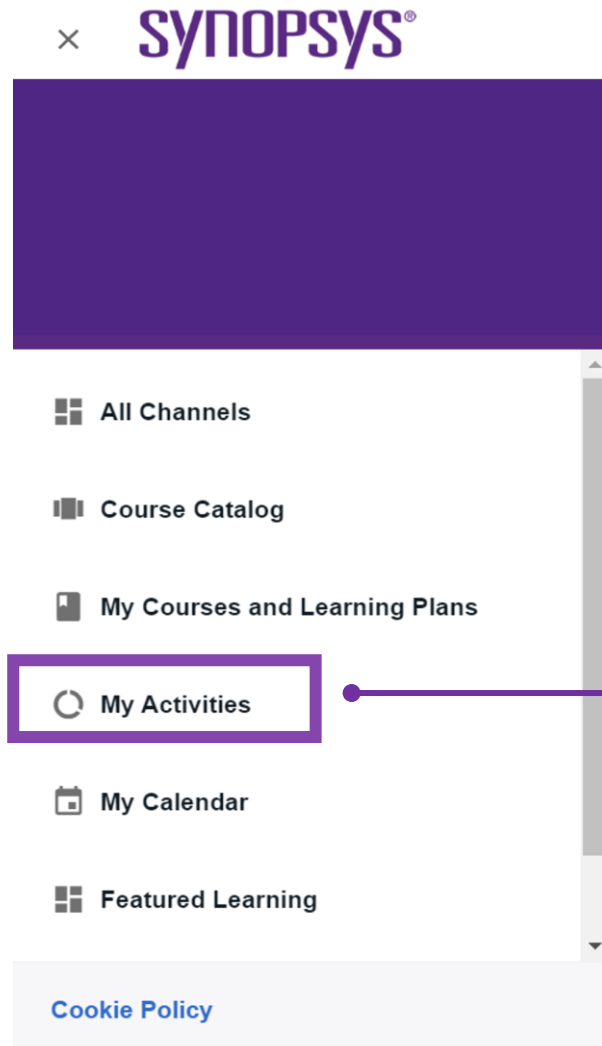
Quick Tip: Snapping block edges to grid during block resizing

EN | 01m 14s


★ 4.0

E-Learning

07 Click on “My Activities”


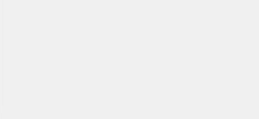



(*Your information, performance, badges, certification, etc. will be shown here.)




My Activities

- Statistics
- Additional Info
- Courses
- ILT (Instructor-Led Training)
- Learning Paths
- Badges
- Social
- Certification




Subscription date



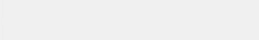
Total time

Progress



1 (33%)

See all activity within the last 30 days



4

08 Click on “University Program”

×

SYNOPSYS®

All Channels

Course Catalog

My Courses and Learning Plans

My Activities

My Calendar

Featured Learning

University Program

Academic users approved by Synopsys University Program (TW) are entitled to the “Elite” subscription model.
More details for the subscription model ([Link](#)).

University Program

Courses and resources intended for learners from universities that are part of Synopsys' University Program

CATEGORIES

FILTERS

Search...

0 Active Filters

Enrollment Status

Price

Language

Duration

Training Category

☐ Product Foundation Training

☐ Product Jumpstart Training

☐ Reference Methodology

☐ Language/Methodology Training

62 items

SILICON DESIGN

New

Fusion Compiler Hierarchical Design Planning

FOUNDATION

Fusion Compiler: Hierarchical Design Planning

ENROLLED

EN

E-Learning

SILICON DESIGN

New

Fusion Compiler Design Creation and Synthesis

FOUNDATION

Fusion Compiler: Design Creation and Synthesis

FREE

EN

E-Learning

SILICON DESIGN

New

Fusion Compiler Design Implementation

FOUNDATION

Fusion Compiler: Design Implementation

FREE

EN

E-Learning

SILICON VERIFICATION

New

Virtualizer VDK Creation Quick Start

SILICON VERIFICATION

New

Virtualizer TLM Creation Quick Start

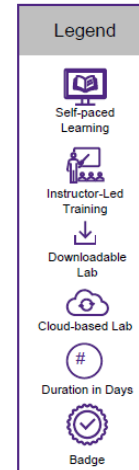
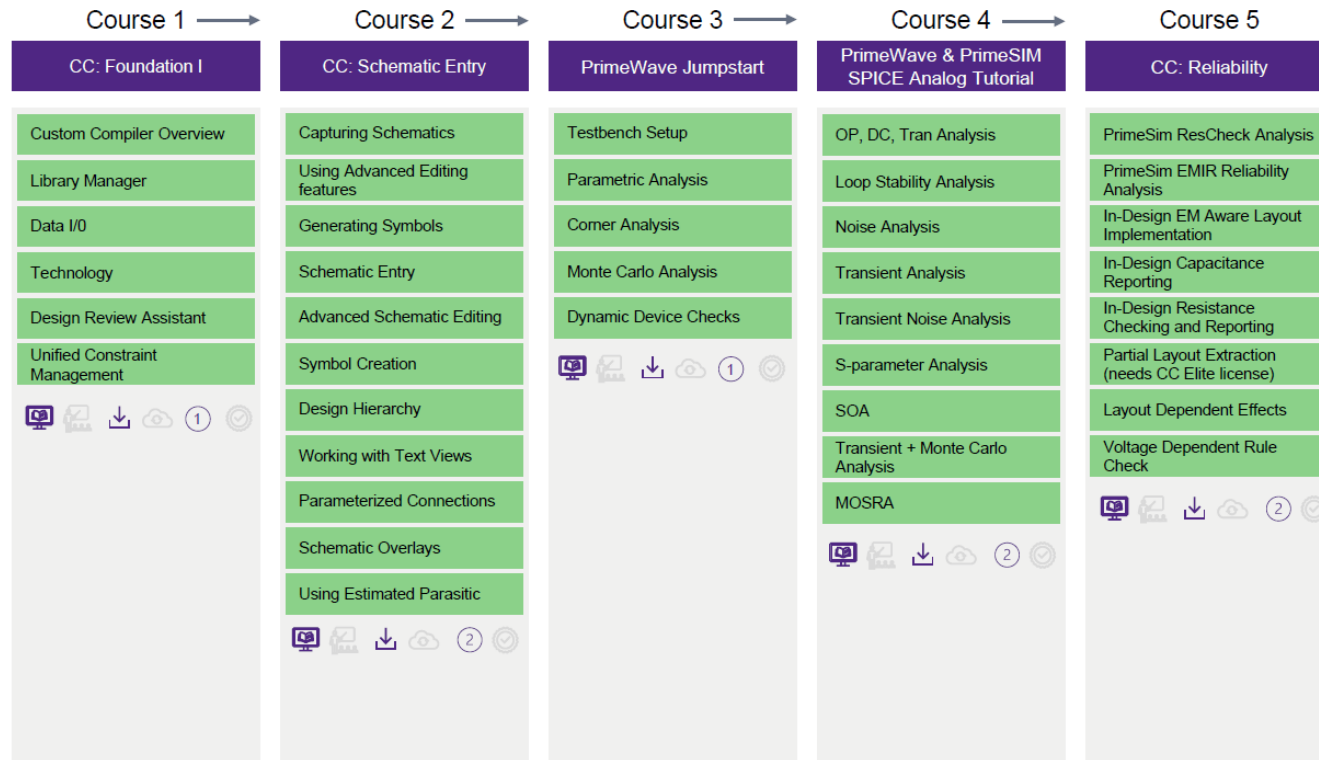
SILICON VERIFICATION

New

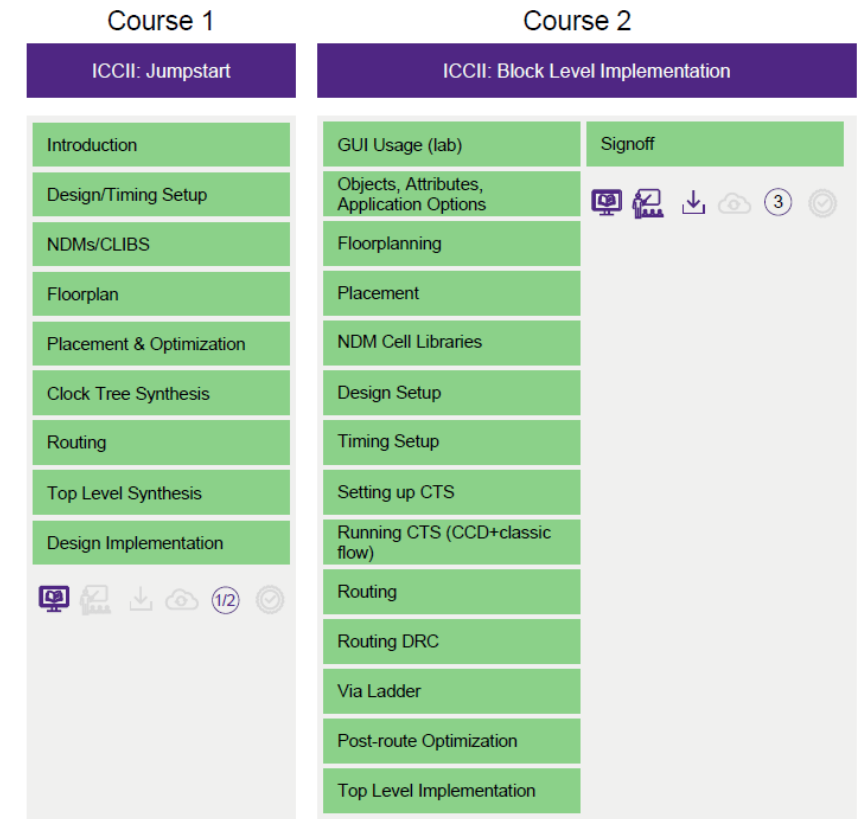
VDK: Debug Perspective of the Virtualizer Studio

09 Synopsys Learning Paths

Custom Compiler Learning Path **Analog Designer**



IC Compiler II Learning Path



Learning Paths are available on Synopsys Learning Center.
-> Explore more Synopsys Learning Paths ([Link](#))

Thank You

Synopsys University Program
(chunhsu@synopsys.com)

