SYNOPSYS®
Silicon to Software™

A Quick Guide to Synopsys University Program Resources

Courseware, SolvNetPlus & Synopsys Learning Center

University Program, Synopsys Taiwan

November 2022

Contents

- Membership Benefit

- Teaching Resources

  - courseware, generic libraries, PDKs

- Knowledge Base

  - SolvNetPlus

  - Synopsys Learning Center

Contents

- **Membership Benefit**
- Teaching Resources
    - courseware, generic libraries, PDKs
- Knowledge Base
    - SolvNetPlus
    - Synopsys Learning Center

Membership Benefits

Teaching Resources 教學資源

IC Design and EDA Curriculum:
- Full Semester Courses – *80+ courses* for Bachelor and Master programs
- Workshops/Lectures - *30 courses*
- Short Lectures/Labs - *28 courses*

Teaching Support:
- *14nm, 32/28nm* & *90nm* Generic Libraries and iPDK's
- Generic Memory Compiler

Knowledge Base 知識庫

Access Synopsys knowledge base:
- **Document –** contains product release note, installation guide, user guide & reference manual

- **Search –** provides an advanced search engine to retrieve information from various sources, such as documentation, articles, training, and so on.

- **Training –** Access *Synopsys Learning Center* for free self-paced training resources. The approved academic users are entitled to the **"Elite"** subscription model. Find more details here.

*Requires SolvNetPlus account to access above-mentioned resources.

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Teaching Resources

☞ **Access through:**
https://www.synopsys.com/academic-research/university.html

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SYNOPSYS®

Solutions   Products   Support   Company

University Software Program

Home ▾ / Academic & Research Alliances ▾ / University Software Program

Through our University Software Program we aim to inspire and foster the world's next generation of technologists and innovators by providing academic and research institutions with access to the EDA tools and technology needed to prepare highly-skilled graduates ready to work in the world of Smart Everything. Membership in the program includes access to leading-edge EDA software, technical support, curriculum, and more.

Support & Training

Teaching Resources

IC Design and EDA Curriculum

IC Design Curriculum

Bachelor

- Advanced Methods in Logic Synthesis and Equivalence Checking
- Analog and Mixed-Signal IC Physical Design
- Analog Integrated Circuits
- Computer Architecture and Engineering
- Digital ASIC Design (NCSU)
- Digital Integrated Circuits
- Electrotechnical Bases of Electronic Circuits
- Fundamentals of Telecommunications
- High Speed SerDes Design

- IC Design Flow (RAU)
- IC Design Introduction
- IC Simulation, Theory
- IC Testing
- Introduction to Logic Design (SU)
- Introduction to Microelectronic Circuits
- Introduction to Semiconductor Devices
- Introduction to VLSI Design (UT)

- Linear Algebra
- Logic Design
- Microprocessor Systems
- RF Circuits
- Numerical Methods
- Scripting Languages for Beginners
- Signal Processing and Systems Theory
- Static Timing Analysis
- Synthesis and Optimization of Digital Integrated Circuits
- Technical Writing

Master

- Analog Modeling with Verilog-A
- ARC Processor-Based Embedded Programming
- Complex Functions
- Crosstalk and Noise
- Design for Test
- Design of Embedded Systems
- Design of Special I/O's
- Digital Signal Processing
- Digital VLSI Design

- EDA Tools
- FPGA Prototyping
- IC Design for Thermal Issues
- IO Design
- Low Power Design
- Low Power Methodology Manual (SVTI)
- Mixed-Signal IC Design
- Modeling and Optimization of IC Interconnects
- Nano-Scale Circuits and Systems (SFSU)

- Rad-hard IC Design
- RF IC Design
- Synopsys EDA Tool Flow for Front-End Digital IC Design
- Synopsys EDA Tool Flow for Back-End Digital IC Design
- Thermal and Electro-Thermal Simulation: Achievements and Trends
- VLSI Design Verification and Testing

EDA Curriculum

Bachelor

- Algorithms and Structural Programming
- Analog Integrated Circuits
- Applied Probability
- Big Data
- Data Structures
- EDA Introduction

- Hardware Description Languages
- IC Design Introduction
- Introduction to Algorithms
- Linear Algebra
- Memory Schematic Design Basics
- Numerical Methods

- Operating Systems and System Programming
- Probability Theory and Mathematical Statistics
- Programming Languages and Compilers
- Technical Writing
- Theory of Algorithms
- Unix System Administration

Master

- Compilers Design
- Complex Functions
- Computational Geometry
- Computer Language Engineering
- Contemporary Software Development Kits
- Database Management System
- Databases
- Design of Programming Languages
- Discrete Mathematics and Probability

- EDA Mathematical Methods
- Fourier Transformations
- Fuzzy Logic
- IC Design Algorithms
- IC Schematic Design Algorithms
- IC Verification Algorithms
- Modeling and Optimization of IC Interconnects

- Object-Oriented Programming
- Operational Research 2
- Programming C++
- Semiconductor Devices and Technology
- Software Development Technology

Workshops / Lectures / Short Lectures / Labs

Workshops and Lectures

- **Verification**
  - Computer Arithmetic Applied to High-performance Cryptography (USP)
  - SystemVerilog Verification Tutorial (SFSU)
  - Universal Verification Methodology
- **Other**
  - Memory PHY and DRAM
  - Project Management
  - Python

- **Implementation**
  - Advanced Design of Digital Circuits for Specific Applications (USP)
  - ASIC Design Flow Tutorial Based on the Synopsys 32/28nm Generic Library (SFSU)
  - ASIC Design Flow Tutorial Based on the Synopsys 90nm Generic Library (SFSU)
  - Chip Design
  - Design for Testability (SFSU)

- Full Custom IC Design Flow Using Synopsys Custom Tools (SFSU)
- Custom Analog Design Flow Tutorial
- Synopsys Design Flow Tutorial

Short Lectures / Labs

- **Circuit Simulation**
  - Circuit Simulation: Transient Analysis (IITB)
  - Techniques for Circuit Simulation (IITB)
- **Low Power Design**
  - Low Power Methodology Manual for 14nm
  - Low Power Design with SAED 14nm EDK
  - Subthreshold Design and Implementation (RIT)
  - Verification Methodology Manual for Low Power

- **Other**
  - Basic Perl Programming
  - Characterization with SiliconSmart
  - Compiler Optimization and Code Generation
  - Computer Networks
  - Digital Design with Verilog
  - Digital System Design and Simulation with VHDL (SU)
  - Embedded Systems Design (CWRU)
  - How to Create an Interoperable PDK
  - IC Fabrication
  - Introduction to RF Communication
  - Introduction to Verilog HDL
  - Operational Research

- Optimization Methods
- Physical Verification Runset Development
- Power-Performance Optimization of Digital Circuits and Systems (UCLA)
- Process Variation Aware Design (RIT)
- Scripting Languages
- Sequential Elements
- Signal and Power Integrity: Current State and New Approaches
- Statistical Techniques for Timing Analysis: Current State and Trends
- Tool Command Language (TCL)
- User Interface Desi

Full Semester Courses

- Topics cover all aspects of IC/SoC design

- Courseware for Bachelor and Master level programs

- Full-semester courses contain ~15 weeks of material and include the following components

| Syllabus ✓ | Lectures ✓ | Labs ✓ | Homework ✓ | Exams ✓ | Projects ✓ |
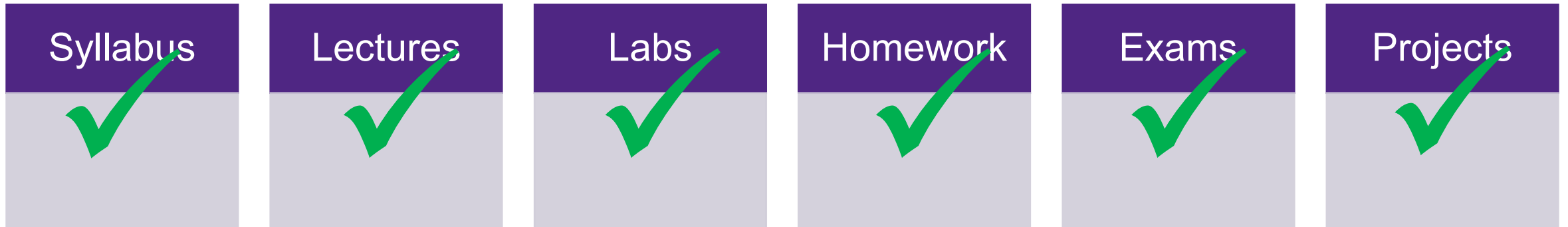
Teaching Resources

Teaching Support (Generic Libraries, PDKs, Generic Memory Compiler)

Generic Libraries (EDK)

- 14nm, 32/28nm and 90nm

- Enables students to master advanced design methods using the latest Synopsys EDA tools
- Includes:

Digital Standard Cell Library	I/O Cell Library	I/O Special Cell Library	Embedded Memories

Phase Locked Loop	Low Power Memories	Reference Designs

- Used by Synopsys for:

Curricula Development	Customer Education	Global Technical Services	Application Consultants
To support development of laboratory works and course projects.	To train customers with Leon3 and ORCA processors' design.	To train internal staff and customers on Synopsys tools and low power flows.	To develop and test sample designs and Reference Methodology scripts.

Interoperable Process Design Kits (iPDKs)

- 32/28nm and 90nm

- Enables students to master AMS/Custom design with the Synopsys custom implementation tool suite

- Includes:

Technology Files	Parasitic Extraction Files	Symbol Library and Python PCells	Embedded Memories
Physical Verification Files	HSPICE Models	Callback Scripts	Setup Files

Curricula Development	Customer Education	Global Technical Services	Application Consultants
To support development of laboratory works and course projects.	To train customers with Leon3 and ORCA processors' design.	To train internal staff and customers on Synopsys tools and low power flows.	To develop and test sample designs and Reference Methodology scripts.

Reference Designs Supported by Synopsys EDKs

- **DesignWare® ARC 600 Academic Core** - 32-bit RISC processor core optimized for embedded applications and DSP tasks

- **ARM® Cortex® - M0 DesignStart™ Processor** - Entry-level configuration of ARM Cortex-M0 microprocessor[1]

- **OpenSPARC T1** - 64-bit multicore processor[2]

- **LEON3** - 32-bit embedded processor[2]

- Sample Processor Designs - included in EDK

  - ORCA for timing analysis
  - ChipTop for low power design

1. *Available through ARM DesignStart for Processor IP portal*
2. *Available via GNU General Public License*

ORCA

ChipTop Layout
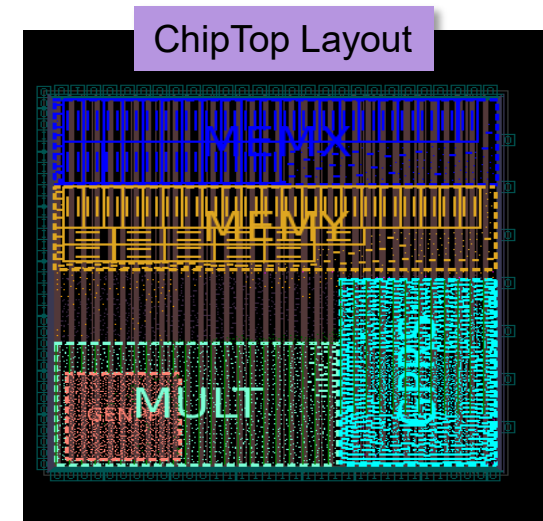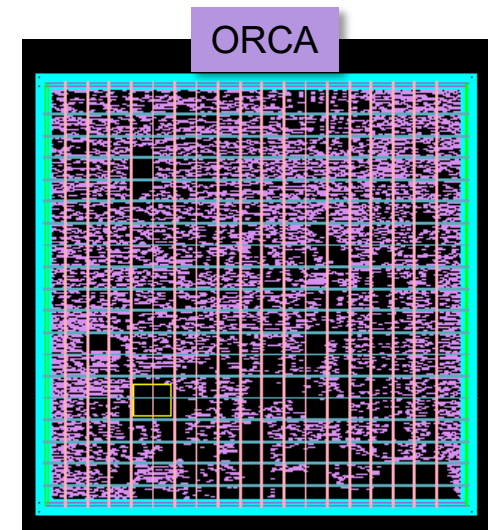
DesignWare ARC 600 Processor Design

- Synthesis scripts optimized for 32/28nm EDK that can be used to easily redesign the academic version of the ARC 600 processor

- Synopsys curriculum for the ARC 600

  – IC Synthesis Based on DesignWare ARC 600 Core, includes:

    – Lecture slides
      – Covers ARC 600 details and EDA tool use

    – Laboratory works
      – Step-by-step guide of the ARC 600 design process

Apply in Members Only for access to the DesignWare ARC 600 Academic Core:
https://www.synopsys.com/apps/protected/university/members.html
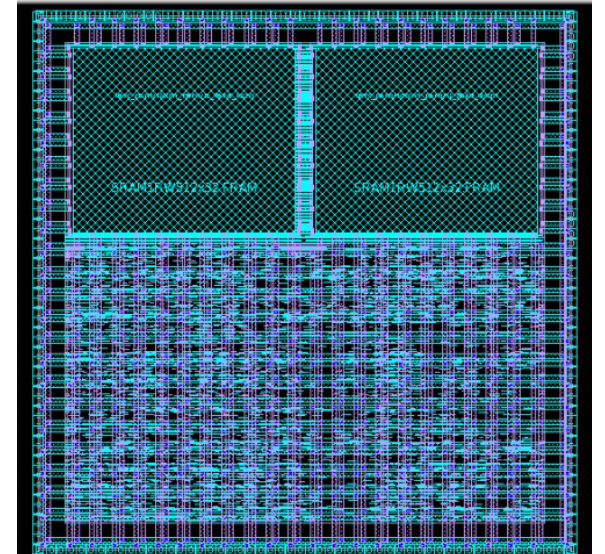
ARM Cortex-M0 DesignStart Processor Design

- Complete Synthesizable Solution
  - Pre-configured Verilog netlist derived from commercial Cortex-M0 processor
  - Simple testbench
  - Example test code
- Scripts to implement the ARM Cortex-M0 DesignStart design using Synopsys 32/28nm EDK and EDA tools
- Synopsys curriculum for the ARM Cortex-M0
  - IC Synthesis Based on ARM Cortex-M0 DesignStart Processor

Download from ARM DesignStart for Processor IP portal:
http://arm.com/products/processors/designstart-processor-ip
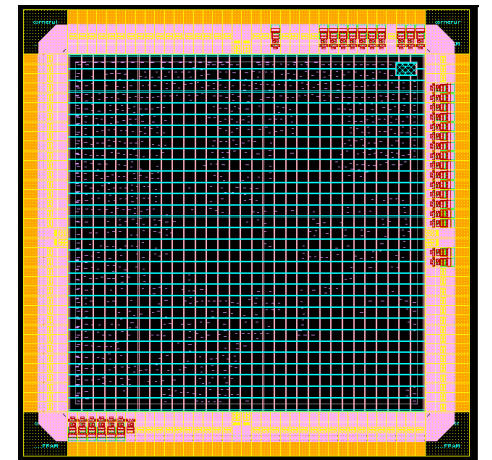
OpenSPARC Processor Design

- Scripts to enable OpenSPARC design using Synopsys 32/28nm EDK and Design Compiler
- Implemented low power design techniques
- Synopsys curriculum for OpenSPARC
  - Computer Architecture
  - Includes:
    - Physical design scripts for IC Compiler
    - Scripts to enable small block reuse for educational purposes
    - Various lab projects based on small blocks

Download OpenSPARC:
http://www.opensparc.net
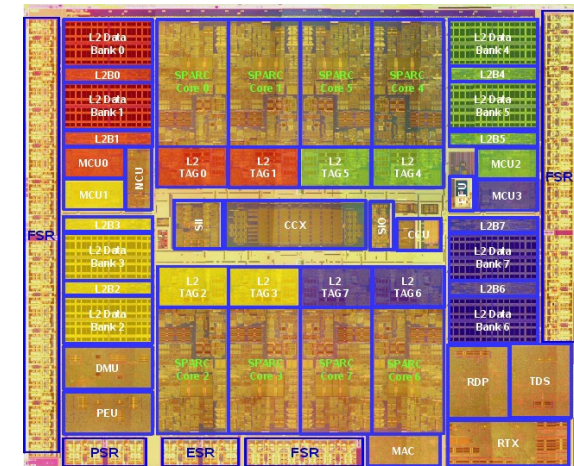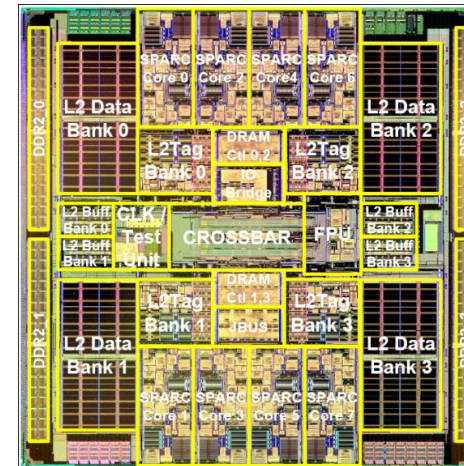
Synopsys Generic Memory Compiler

- Configurable software that automatically generates static RAM circuits of different types and sizes with all required deliverables
- Generate custom memory instances for educational ICs
- Designed for use with Synopsys EDKs and EDA tools
- Optimized for the Synopsys Digital Design Flow
- Supports multiple technologies (90nm, 32/28nm, etc.)

User interface
- Command line
- GUI

Supported memory types
- 1 port SRAM
- 2 port SRAM
- 1 port Low Power SRAM
- 2 port Low Power SRAM

*"Using the Synopsys Generic Memory Compiler in our complex processor for DSP application was a **great time-saving tool**. It helped the students generate the SRAM they wanted in a snap, saving them critical time to concentrate on the rest of the complex design."*

Dr. Maged Ghoneima, American University in Cairo

Get started w/ Teaching Resources

Link: www.synopsys.com/academic-research/university.html

01 Go to Electronic University Program website

Select the Teaching Resources that you need, then click on " Members Only website".

Link: www.synopsys.com/academic-research/university.html

Curriculum

Synopsys provides universities with access to comprehensive curricula for Bachelor and Master Programs in IC design and EDA development.

Each full-semester course contains 15 weeks of material including syllabus, lectures, labs, homework and exams. Synopsys tools are applied in the labs for a thorough and practical understanding of theoretical concepts introduced in each course. Professors at member universities may use these course materials to implement a new course or to supplement content in an existing course.
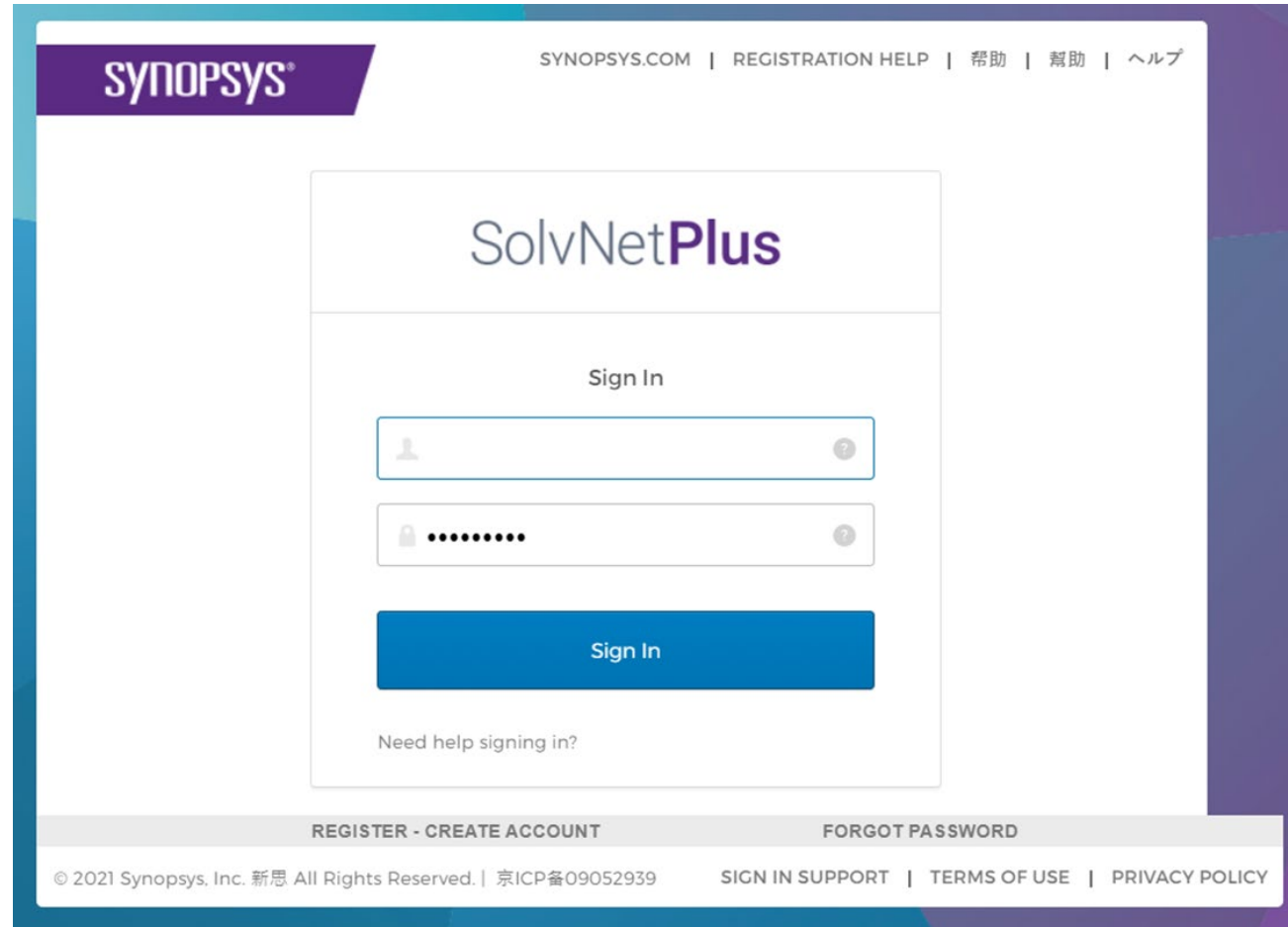
All courseware described below may be downloaded from the Synopsys University Software Program Members Only website (requires SolvNet ID and password). If your university is not yet a member of the Synopsys University Software Program and you would like to apply, please contact us.

Full Semester Courseware

IC Design Curriculum

- Requires a SolvNetPlus account to sign in.
- Please contact *Synopsys University Program – Taiwan (tw-up@synopsys.com)* for membership enquiry.

02 Log-in with Synopsys SolvNetPlus credential

https://www.synopsys.com/apps/protected/university/members.html

03 Insert course name in the search engine

Search by "Course Type"

Course Type:

1. Full Semester
2. Short Lectures / Labs
3. Workshops / Lecturers

03 Insert course name in the search engine (cont.)

Search by "Course Category"

Example : Full Semester

More Search Options

Course Type: Full Semester

Course Category: ----- Select Below -----

----- Select Below -----

Analog/RF Design

Digital System Architecture and Design

IC/Semiconductor Fabrication

Other

Course Degree:

Curriculum Type:

131 results wer

Advanced Design of
The objective of thi... ...used in the development of digital integrated circuits for specific... ...e used in the digital electronics market and will be used by student... ...n this area. The course reviews basic concepts of digital design and explores in depth the advanced techniques used by design professionals. These techniques involve ways of dealing with complex systems, ways to create faster systems, methodologies for design verification and evaluation of results. The course covers and compares the use of VHDL and Verilog, and the impact of coding style on final results. Note: This course can be used with permission from the 3rd party owner. All rights reserved.

> Lectures (18 MB)

Advanced Methods in Logic Synthesis and Equivalence Checking
The goal of the course is to study logic synthesis problem, logic optimization as well as advanced methods in synthesis. The course also focuses on logic design components and combinational and sequential equivalent checking.

> Syllabus (88.0 KB)
> Lectures (3,135,241 bytes)
> Labs (657 KB)
> Homework (263 KB)
> Labs & Homework (441 KB)

Course Category:

1. Analog / RF Design
2. Digital System Architecture and Design
3. IC / Semiconductor Fabrication
4. Other

03 Insert course name in the search engine (cont.)

Search by "Curriculum Type"

Example : Full Semester

Keyword Search:

| | search | view all |

More Search Options

Course Type: Full Semester

Course Category: ----- Select Below -----

Course Degree: ----- Select Below -----

Curriculum Type: ----- Select Below -----

----- Select Below -----

EDA

VLSI

131 results wer

Advanced Design of

The objective of thi   used in the development of digital integrated
circuits for specific   e used in the digital electronics market and will
be used by students of this course to develop their knowledge in this area. The course reviews basic concepts
of digital design and explores in depth the advanced techniques used by design professionals. These
techniques involve ways of dealing with complex systems, ways to create faster systems, methodologies for
design verification and evaluation of results. The course covers and compares the use of VHDL and Verilog,
and the impact of coding style on final results. Note: This course can be used with permission from the 3rd
party owner. All rights reserved.

> Lectures (18 MB)

Curriculum Type:

1. EDA
2. VLSI

04 Access to the courseware

Start to download course syllabus, lecturer slides, labs or exams

Example : Full Semester

Keyword Search:

	search	view all

More Search Options

Course Type: ----- Select Below -----

Course Category: [dropdown]

48 results were found under **'Full Semester' Course Type, 'VLSI' Curriculum Type.**

Analog and Mixed-Signal IC Physical Design - December 2018
This course covers the basics of IC design, custom design flows. The course mainly focuses on data of analog and mixed-signal IC physical design.

> Syllabus (90 KB)
> Lectures (4.6 MB)
> Labs (1.6 MB)
> Homework & Exams (244 KB)

Analog Integrated Circuits - October 2021
The goal of the course is to study principles of design, analysis and simulation of analog integrated circuits. The course also focuses on variants, parameter improvement methods, parameters analysis of different basic analog circuits: differential and operational amplifiers, switched capacitor circuits, oscillators, phase looked loops, data converters, secondary power sources, etc.

> Syllabus (108 KB)
> Lectures (17 MB)
> Labs (12 MB)
> Project (663 KB)
> Homework & Exams (498 KB)

Course Contents:

1. Syllabus
2. Lectures
3. Labs
4. Project
5. Homework & Exams

Contents

- Membership Benefit

- Teaching Resources

  - courseware, generic libraries, PDKs

- **Knowledge Base**

  - **SolvNetPlus**

  - **Synopsys Learning Center**

Knowledge Base

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☞ **Access through:**
https://solvnetplus.synopsys.com/

Get Oriented with SolvNetPlus

University users can access Documentation, Training & Search ; but CANNOT access Download, EFT, Cases & STARs.

Knowledge Base

SolvNetPlus (Documentation & Search)
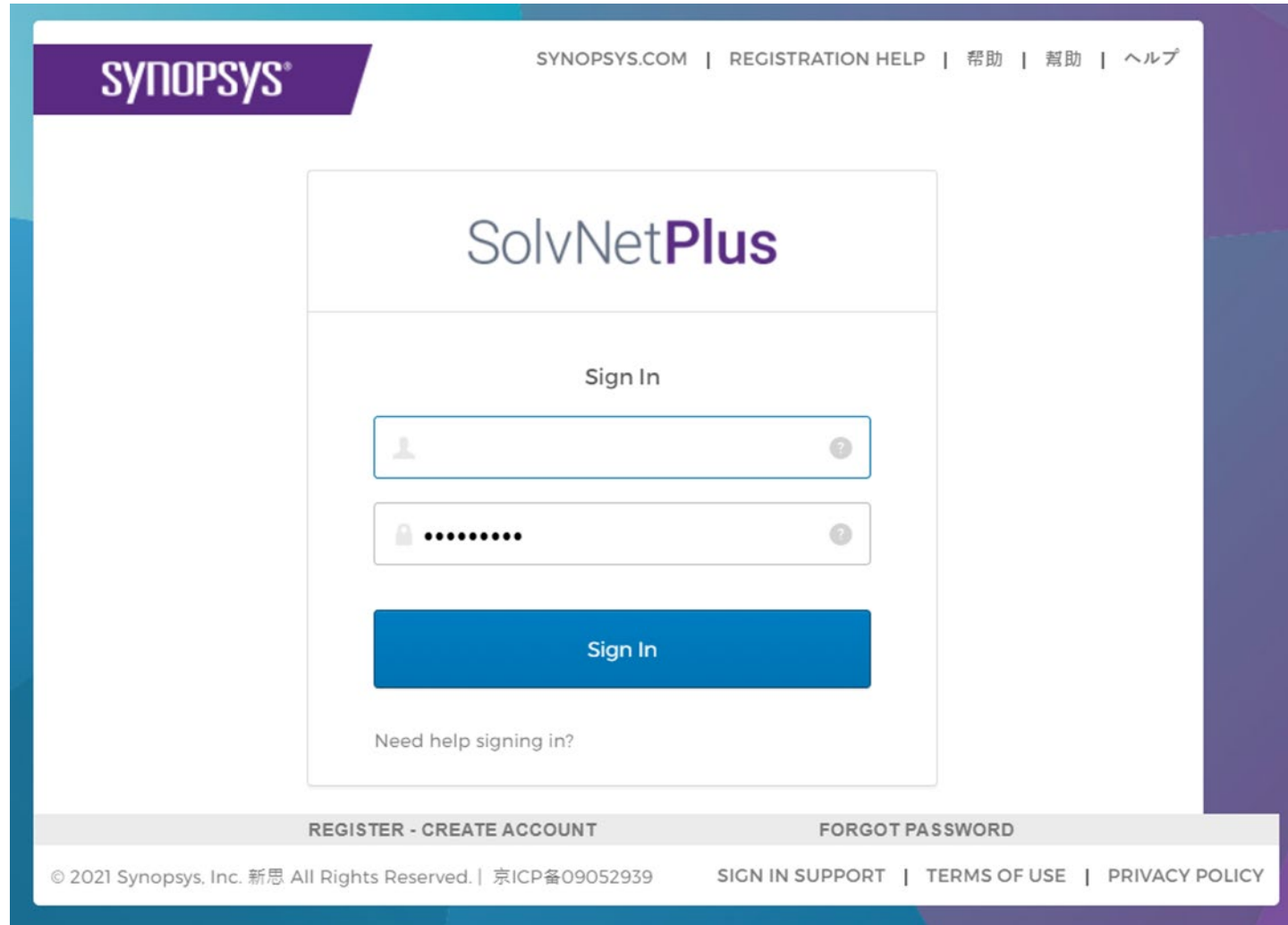
Get started w/ SolvNetPlus

https://solvnetplus.synopsys.com/

01 Log-in with Synopsys SolvNetPlus credential

https://solvnet.synopsys.com/

02 Read " GETTING STARTED" before use
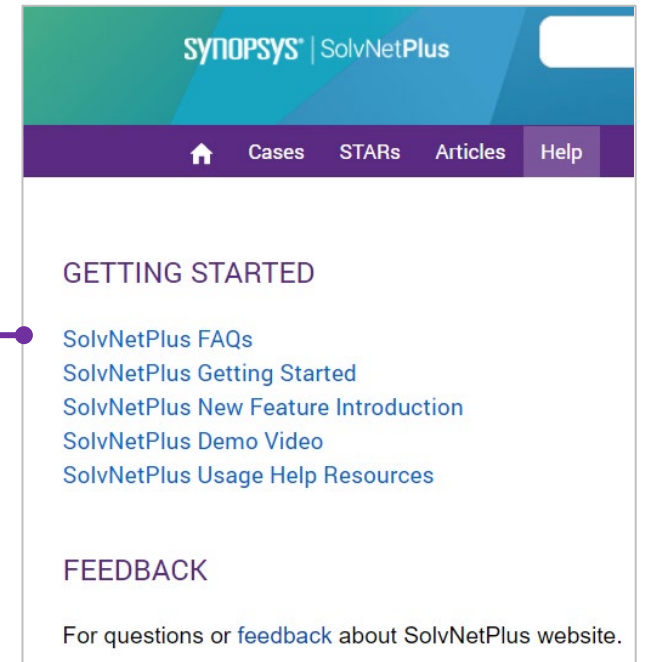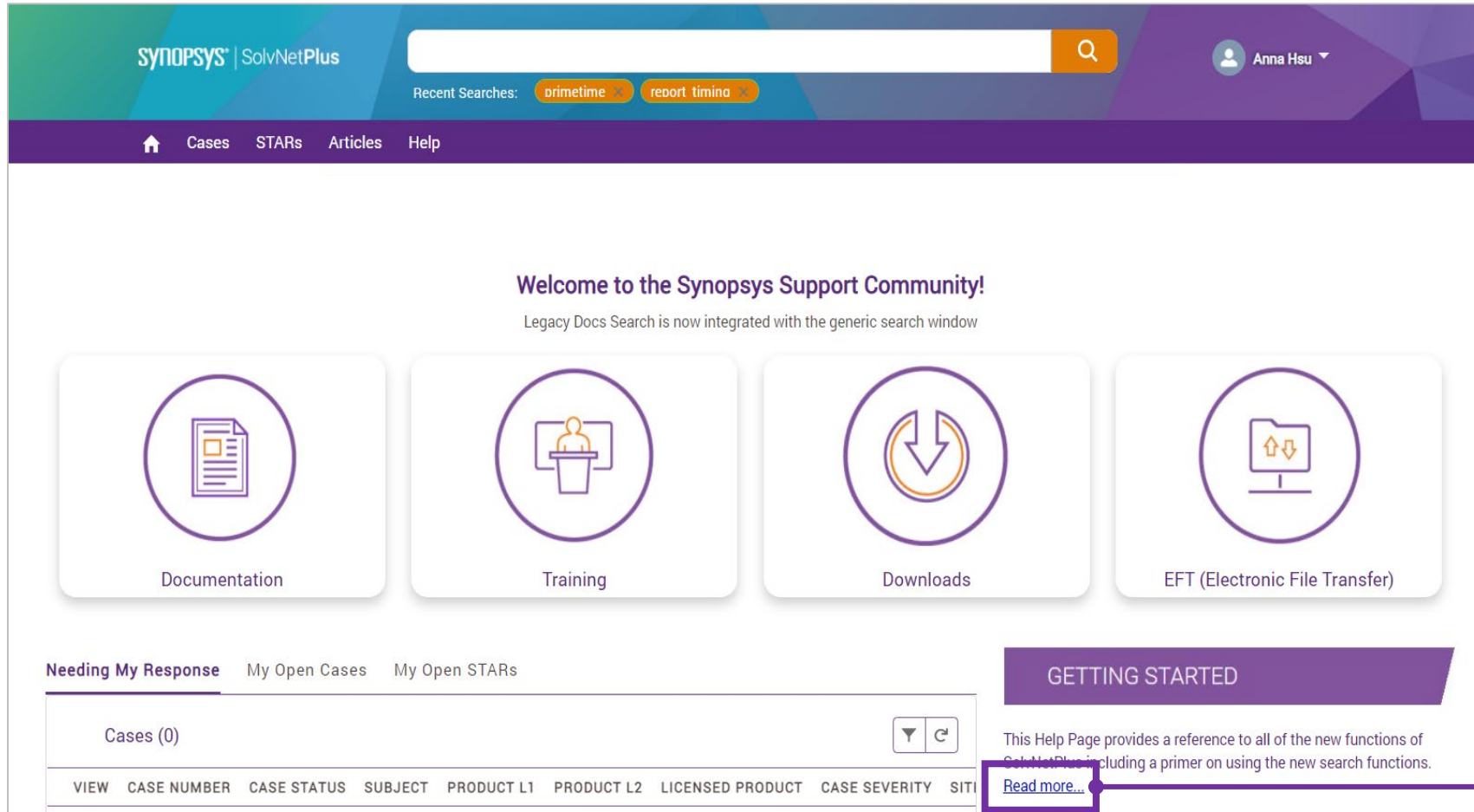
03 Click on "Documentation"
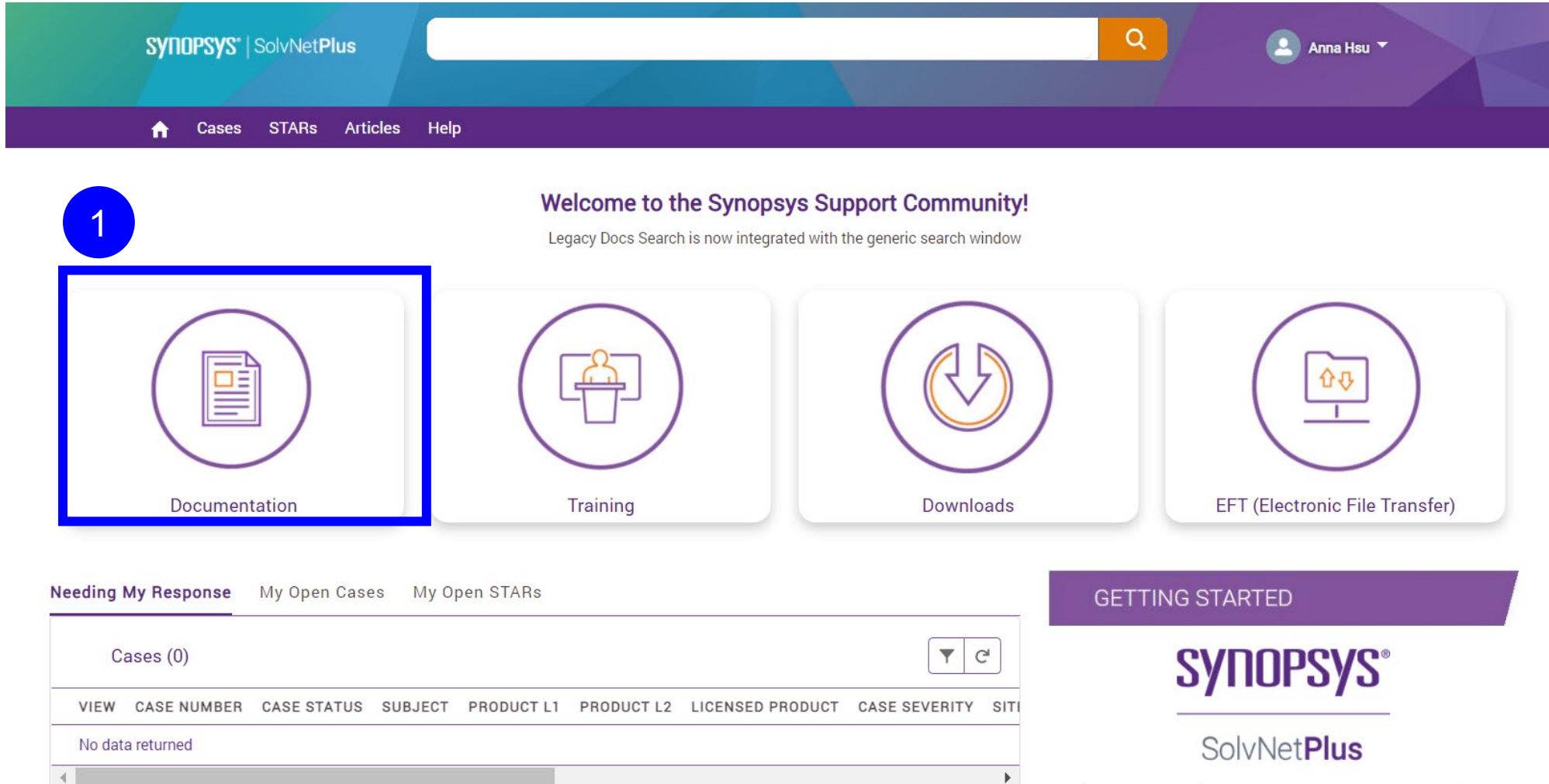
04 Search by product name to get tool documents

You can download release notes, installation guides & user guides and reference manuals from this section

SYNOPSYS | SolvNetPlus

Cases   STARs   Articles   Help

Documentation

A
  Avalon™

C
  CATS®
  Certify®
  Certitude®
  coreTools
  CosmosScope™
  Custom Compiler™
  Custom WaveView™
  CustomSim™

D

I
  ICE Speed Adaptor
  IC Compiler™
  IC Compiler™ II
  IC Validator
  IC Validator WorkBench
  IC WorkBench Edit/View Plus
  Identify®

L
  Laker® Products
  Library Compiler™
  Lynx Design System

T
  Taurus™
  TCAD Sentaurus™
  TCAD Sentaurus™ PCM Studio
  TestMAX™ Tools
  Tweaker

V
  VC Execution Manager
  VC Formal
  VC Functional Safety Manager
  VC LP

Example : Laker

Laker

Laker3, L-2018.06, June 2018

- Laker3 Installation Guide
- Laker3 Quick Start Guide for Laker3 User Interface, K-2015.06, June 2015
- Laker3 Command Reference Manual, K-2015.06, June 2015
- Laker3 Tcl Reference Manual, K-2015.06, June 2015
- Laker3 Bind Key Summary
- Laker3 Menu Summary
- Laker DRD Tcl Command Reference, K-2015.06, June 2015
- Laker CDPR LEF/DEF Tutorial, 2013.02, February 2013
- Laker CDPR Data Preparation and SDL Tutorial, 2013.02, February 2013
- Laker3 Release Notes Version, L-2018.06-SP1 (January 2019)

Laker, 2020.03, March 2020

- Laker User Guide and Tutorial, 2015.03
- Laker Command Reference, 2015.12
- Laker Tcl Reference, 2015.12
- Laker Bind Key Summary, 2015.12
- Laker Command Index, 2015.12

05 Look for information in the "Search" bar

You can use search to retrieve information from various sources

06 Choose needed info from the displayed search results

The information will be displayed from various sources, such as documentation, articles, training, YouTube, and so on (but _NOT_ in cases & STARs)

Example : insert "report_timing"

Knowledge Base

Synopsys Learning Center (Self-paced Learning)

1. Access via SolvNetPlus (https://solvnet.synopsys.com/)
2. Access via Synopsys Learning Center (https://www.synopsys.com/support/training/self-paced.html)

01 Login SolvNetPlus and click "Training"
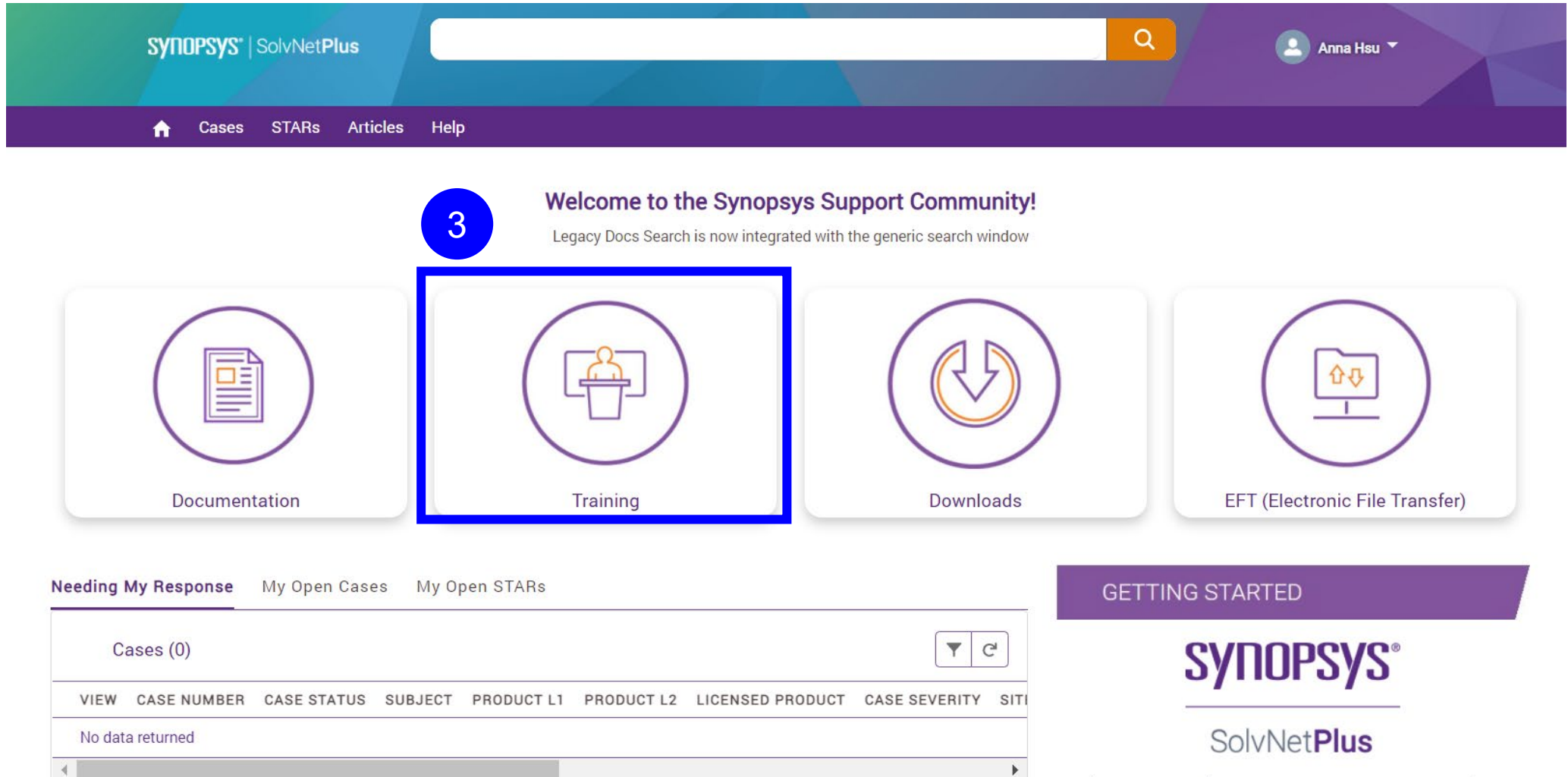
02 SSO Login via SolvNetPlus

02 Access Synopsys Learning Center

✓ You can also directly access through: https://training.synopsys.com/

03 Click on "☰"

04 Click on "Course Catalog"

SYNOPSYS®
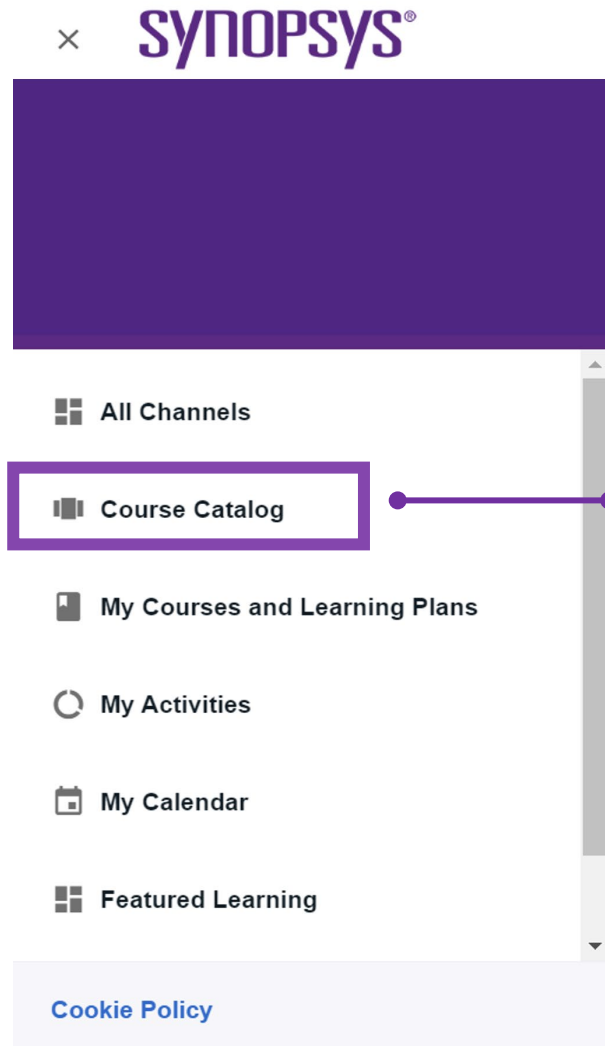
*(*The courses are free to all users)*

Course Catalog

All your courses and learning plans in which you're enrolled, including all your courses and learning plans in progress and already completed.

📁 CATEGORIES   ☰ FILTERS | Search...   🔍 | **CARDS**

- All Channels

- **Course Catalog**

- My Courses and Learning Plans

- My Activities

- My Calendar

- Featured Learning

Cookie Policy

Optical and Photonic Solutions
Courses for the Optical Solutions Group and Photonic Solutions

RSoft: 元件工具使用技巧 - Part I (May 2022 Tech Talk)	LightTools: Making Ray Files Work (User Group Webinar)	CODE V: Choose Glasses like a Pro with CODE V Glass Expert! (April 2022...	LightTools: 2022.03 New Features (March 2022 Tech Talk)	CODE V Self-Guided Onboarding
FREE	**FREE**	**ENROLLED**	**FREE**	**FREE**
ZH | 44m 00s	EN | 35m 00s	EN | 55m 00s	EN | 45m 00s	EN | 1h 15m ★ 5.0
▶ E-Learning	▶ E-Learning	▶ E-Learning	▶ E-Learning	▶ E-Learning

05 The Interface of Courses
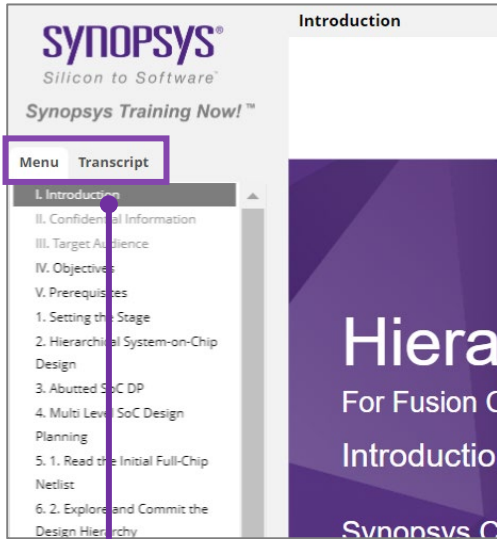
Menu and transcript are provided.

Downloadable files/instructions

Scroll down to see course description, including abstract, objectives, audience profile, etc.

06 Click on "My Courses and Learning Plan"

SYNOPSYS®

- All Channels
- Course Catalog
- **My Courses and Learning Plans**
- My Activities
- My Calendar
- Featured Learning

Cookie Policy

*(*All of your courses will be shown here.)*

My Courses and Learning Plans
All of your courses and learning plans in which you're enrolled, including all of your courses in progress and already completed.

FILTERS | Search... 🔍

3 items

Fusion Compiler: Hierarchical Design Planning
SILICON DESIGN
Fusion Compiler Hierarchical Design Planning
FOUNDATION
Not Started
EN
▶ E-Learning

CODE V: Choose Glasses like a Pro with CODE V Glass Expert! (April 2022...
OPTICAL SOLUTIONS
CODE V
In Progress
EN | 55m 00s
▶ E-Learning

Quick Tip: Snapping block edges to grid during block resizing
SILICON DESIGN
Physical Implementation
IC Compiler II
QUICK TIP
Completed
EN | 01m 14s | ★ 4.0
▶ E-Learning

07 Click on "My Activities"
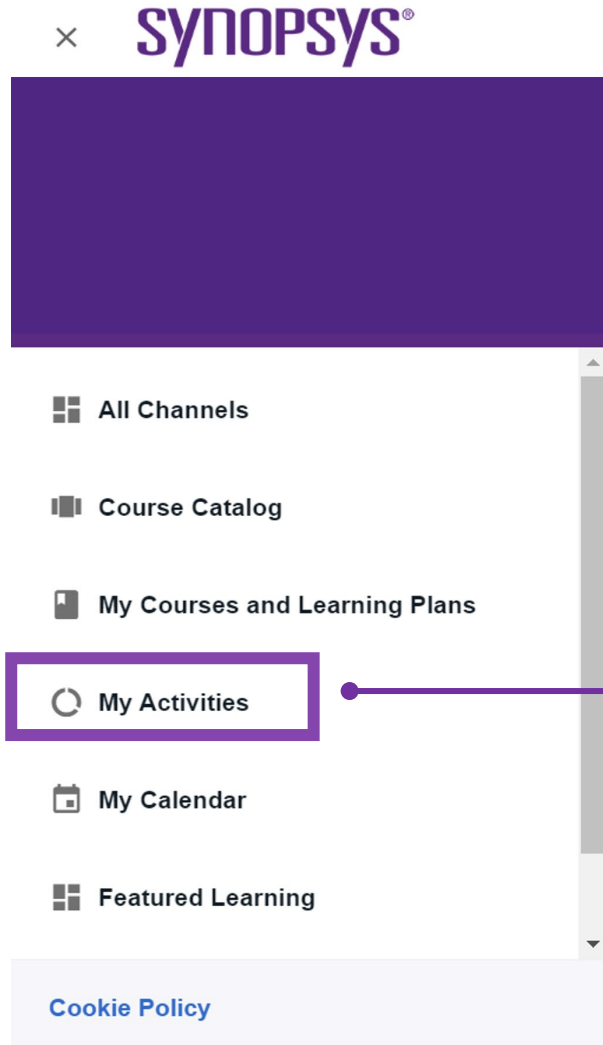
SYNOPSYS®

(*Your information, performance, badges, certification, etc. will be shown here.)

My Activities

- **All Channels**
- **Course Catalog**
- **My Courses and Learning Plans**
- **My Activities**
- **My Calendar**
- **Featured Learning**

Cookie Policy

Statistics	
Additional Info	
Courses	
ILT (Instructor-Led Training)	
Learning Paths	
Badges	
Social	
Certification	

Subscription date

Total time

Progress

1 (33%)

See all activity within the l

4
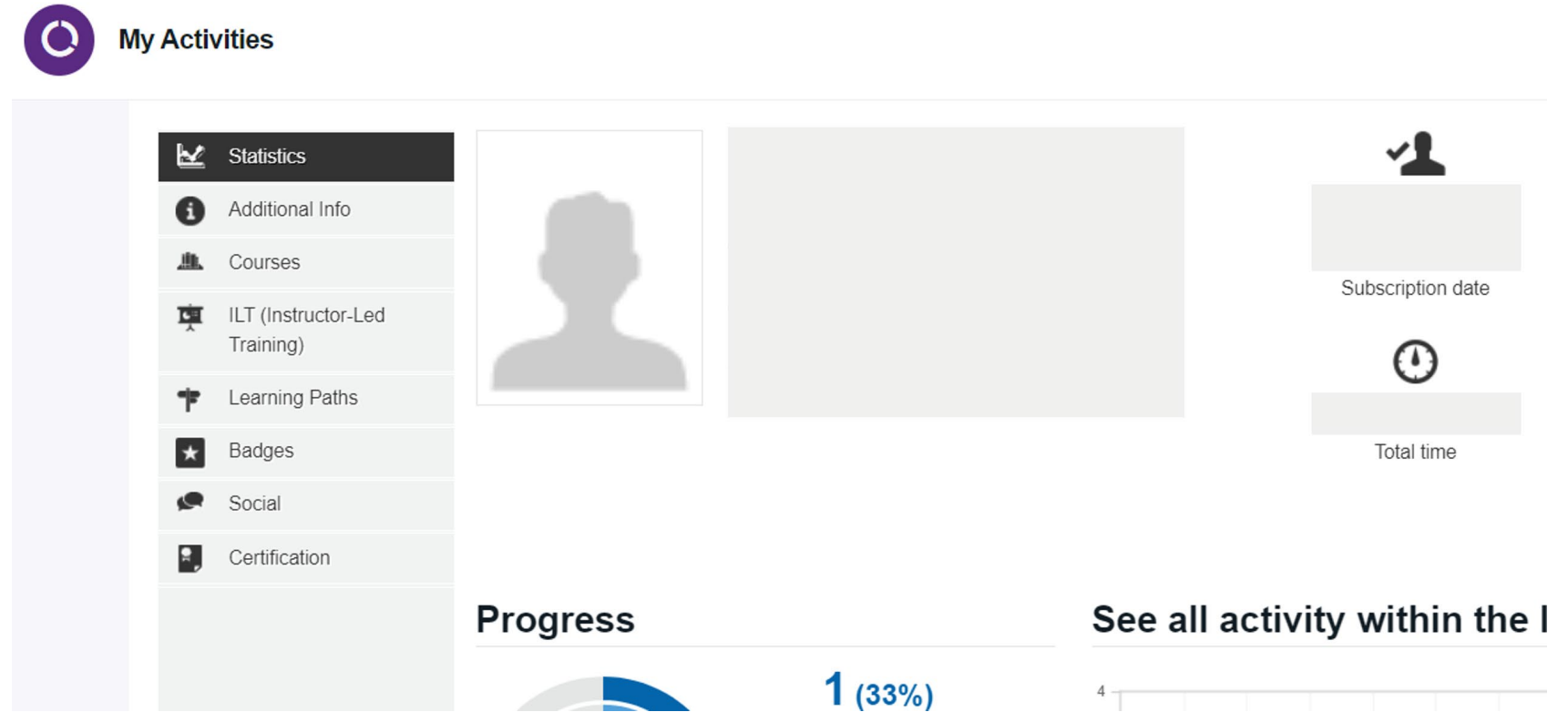
08 Click on "University Program"
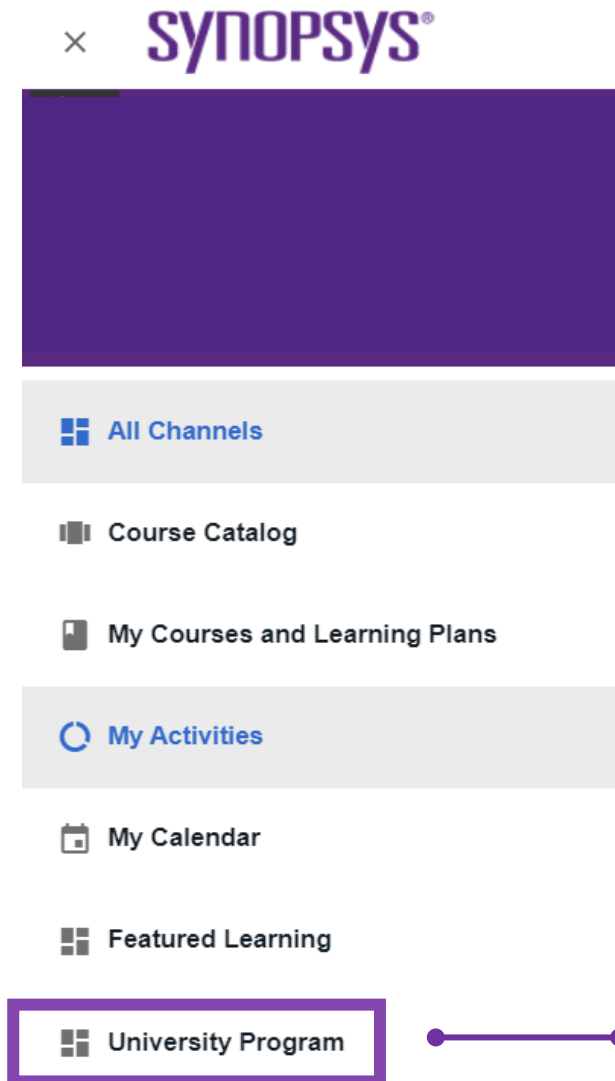
Academic users approved by Synopsys University Program (TW) are entitled to the "Elite" subscription model.

More details for the subscription model (Link).

09 Synopsys Learning Paths

Custom Compiler Learning Path **Analog Designer**

Course 1 →	Course 2 →	Course 3 →	Course 4 →	Course 5
CC: Foundation I	**CC: Schematic Entry**	**PrimeWave Jumpstart**	**PrimeWave & PrimeSIM SPICE Analog Tutorial**	**CC: Reliability**
Custom Compiler Overview	Capturing Schematics	Testbench Setup	OP, DC, Tran Analysis	PrimeSim ResCheck Analysis
Library Manager	Using Advanced Editing features	Parametric Analysis	Loop Stability Analysis	PrimeSim EMIR Reliability Analysis
Data I/0	Generating Symbols	Corner Analysis	Noise Analysis	In-Design EM Aware Layout Implementation
Technology	Schematic Entry	Monte Carlo Analysis	Transient Analysis	In-Design Capacitance Reporting
Design Review Assistant	Advanced Schematic Editing	Dynamic Device Checks	Transient Noise Analysis	In-Design Resistance Checking and Reporting
Unified Constraint Management	Symbol Creation		S-parameter Analysis	Partial Layout Extraction (needs CC Elite license)
	Design Hierarchy		SOA	Layout Dependent Effects
	Working with Text Views		Transient + Monte Carlo Analysis	Voltage Dependent Rule Check
	Parameterized Connections		MOSRA	
	Schematic Overlays			
	Using Estimated Parasitic			

IC Compiler II Learning Path

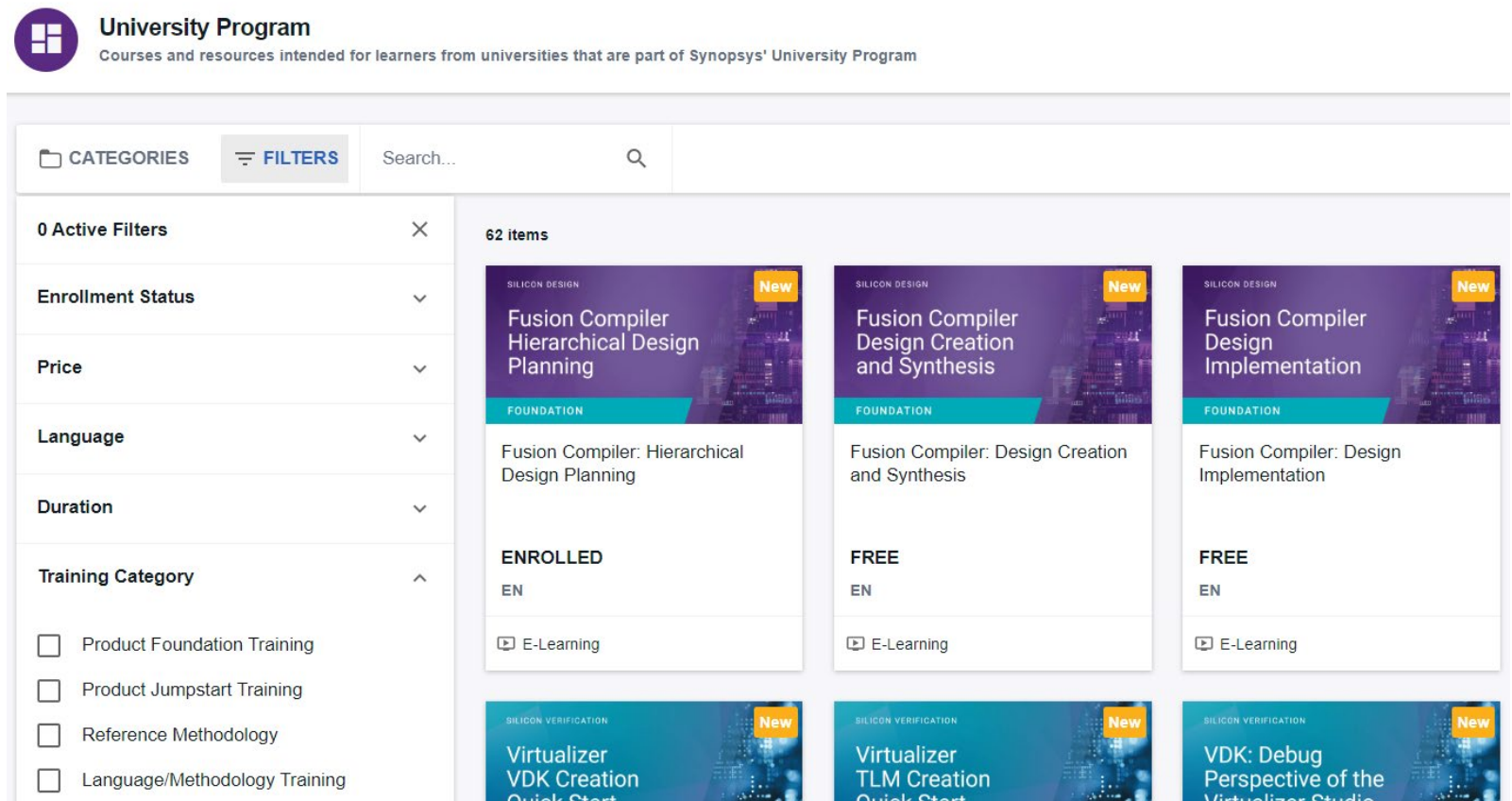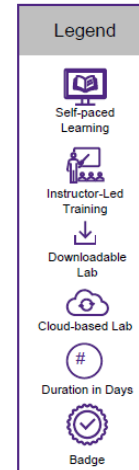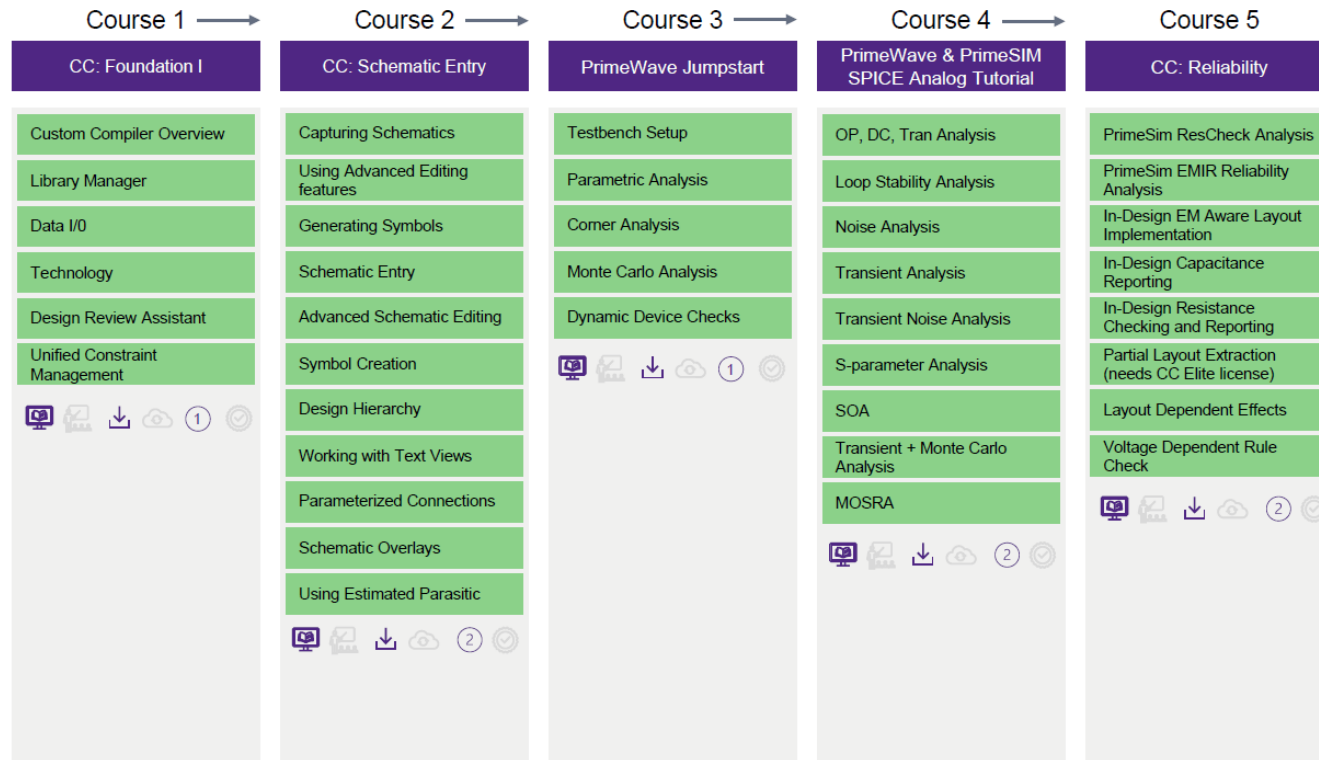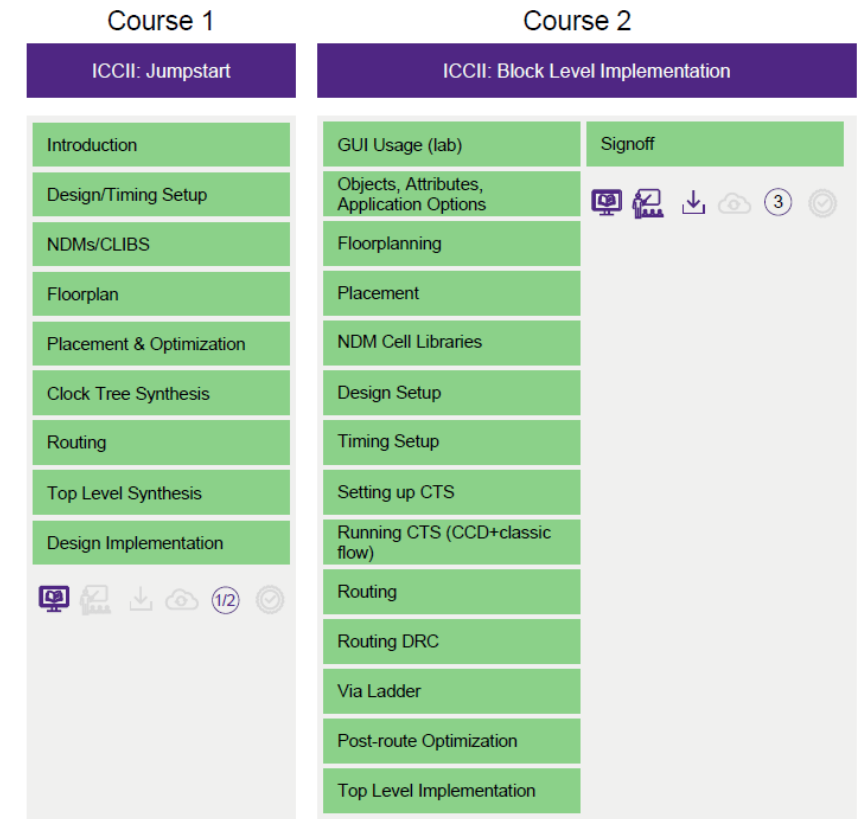| Course 1	Course 2	
ICCII: Jumpstart	**ICCII: Block Level Implementation**	
Introduction	GUI Usage (lab)	Signoff
Design/Timing Setup	Objects, Attributes, Application Options	
NDMs/CLIBS	Floorplanning	
Floorplan	Placement	
Placement & Optimization	NDM Cell Libraries	
Clock Tree Synthesis	Design Setup	
Routing	Timing Setup	
Top Level Synthesis	Setting up CTS	
Design Implementation	Running CTS (CCD+classic flow)	
	Routing	
	Routing DRC	
	Via Ladder	
	Post-route Optimization	
	Top Level Implementation	

Legend
- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- # Duration in Days
- Badge

Learning Paths are available on Synopsys Learning Center.
-> Explore more Synopsys Learning Paths (Link)

Thank You

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