Synopsys SLM UCIe Monitor Test and Repair (MTR) IP

Highlights

- Performs Monitoring, Test and Repair* of the UCIe die-to-die interconnect
- Fully synthesizable RTL enables usage independent of foundry and technology nodes
- Applicable to both UCIe-S and UCIe-A PHY types with support across multiple UCIe generations
- Enabled during production test via standard JTAG/IEEE1149.1 and in-system via APB interface for complete SLM (Silicon Lifecycle Management) support
- Compiler-based IP with fully automated flow offers ease of use and time to market

Key Features

- Access nearside SIM in UCIe PHY to eye parameter information
- Ability to run UCIe BIST with specific user-defined test pattern or built in algorithmic patterns
- Enables efficient repair with capability to read UCIe PHY reconfiguration registers and write/retrieve repair signature to/from eFuse

Overview

The Synopsys SLM UCIe Monitoring, Test and Repair (MTR) IP is a fully synthesizable RTL based IP designed to perform die-to-die lane monitoring, test and repair* for both Synopsys UCIe Advanced (UCIe-A) and UCIe Standard (UCIe-S) PHY products. The SLM UCIe MTR IP is independent of foundry and technology nodes as it activates and extracts the "eye" information from the SIM (Signal Integrity Monitors) embedded in the Synopsys UCIe PHY during mission mode. Designers can utilize the SLM UCIe MTR IP to perform internal loopback and die-to-die algorithmic Built In Self-Test (BIST) patterns via a standard JTAG/TAP controller during production testing. The UCIe MTR IP can also facilitate storing the faulty/marginal lane repair* information into a local e-fuse during manufacturing mode and retrieving this during subsequent power-up.

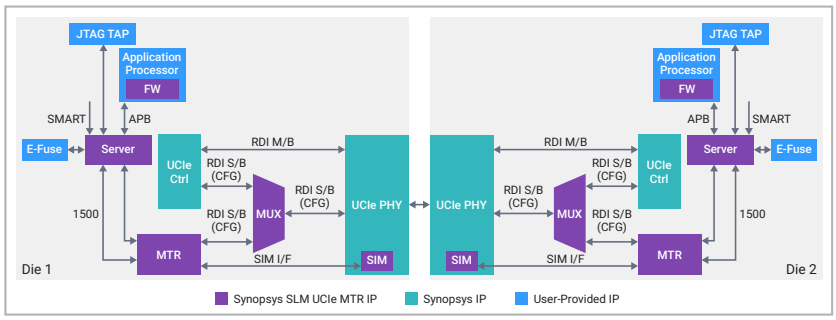

Figure 1: Synopsys SLM UCIe Monitor Test and Repair IP

Key Benefits

- Provides high-quality die-to-die interconnect fault coverage with user defined and algorithmic test patterns to mitigate coupling and crosstalk
- Accelerates silicon bring up for otherwise complex ATE based UCIe die-to-die test and debug
- Embedded SIM's offer high sampling resolution to meet Gigahertz data rates
- Improves RAS (Reliability, Availability and Serviceability) with mission mode capabilities for applications such as automotive and HPC/datacenter
- Compact area efficient footprint with low gate count due to co-optimized design with Synopsys UCIe PHY architecture

*Repair is applicable for only UCIe-A type of PHYs to be used with SLM UCIe MTR IP

Mission Mode Silicon Health Monitoring

The ability to monitor the integrity of the hardware link/interconnect during mission mode is important for applications such as AI Training, where unanticipated failures can result in significant outages and costly deviations from cloud providers Service Level Agreements (SLA's). With the embedded SIMs in the Synopsys UCIe PHY, the SLM UCIe MTR IP can be used to perform various lane eye margin measurements to proactively detect marginalities early and prevent subsequent catastrophic failures. The user has the flexibility to utilize the system CPU to control and measure the data collected over multiple measurement cycles or use the SLM UCIe MTR IP to autonomously measure and collect data and only respond to an interrupt of the measured value is deviating beyond the allowed threshold.

Test Quality and Coverage

Traditional ATE based probing for testing, diagnosis and debug particularly with UCIe's tight pitches and high data rates can be complex, time consuming and costly. Functional vectors or LFSR (Linear Feedback Shift Register) based loop back patterns may not sensitize different types of interconnect faults. The SLM UCIe MTR IP embedded as part of the chiplet design solves these challenges by offering a rigorous and proven algorithmic based test pattern approach offering high test quality thus minimizing test escapes and field returns. At the same time, the user retains flexibility to generate custom test patterns both during High Volume Manufacturing (HVM) and in-field.

Multi-Corner Repair

The SLM UCIe MTR IP handles complete standard and cumulative based repair flow with ability to read/write to the UCIe PHY reconfiguration registers (on both sides of the interface) as well as any local eFuse with minimal user intervention. The standard repair overrides UCIe PHY reconfiguration registers with the previously obtained signature stored in the eFuse, while the cumulative repair overrides UCIe PHY reconfiguration registers with combined signature obtained from the eFuse and UCIe PHY reconfiguration registers.

Deliverables

- SLM UCIe MTR SystemVerilog synthesizable RTL (*.sv)
- Block level SystemVerilog Testbench for verification (*.sv)
- Datasheet (*.ds)
- Synthesis script and design constraints (*.sdc)
- Verification scripts (*.tcl)
- Firmware Compiler delivering sample/reference firmware code (*.c)
- SLM UCIe MTR Compiler User Manual (*.pdf)

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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