Advanced Clock Generator IP

Advanced DFS/DVFS Capability and Rapid Droop Response

Features

- Droop and DFS/DVFS response profile
- Programmable droop and DFS/DVFS response rate
- Interfaces to multi-threshold droop detector
- APB interface for in-field control
- IEEE1149.1/1687 for connection to test fabric
- Core voltage supply
- Comprehensive debug capabilities
- 14-bit fractional output
- Foundry process portable
- 3rd party droop detector support

Applications

- Datacenter/Edge AI
- CPU
- GPU
- High Performance Compute
- High-Reliability SoCs
- Automotive
- Aerospace

Overview

Synopsys SLM Advanced Clock Generator (ACG) IP, part of the Synopsys Silicon Lifecycle Management (SLM) family, provides high-performance clock generation designed for droop mitigation and Dynamic Frequency Scaling (DFS) / Dynamic Voltage and Frequency Scaling (DVFS) application. ACG IP is among the most advanced, flexible and responsive SoC clocking solution on the market, providing ultra-fast adaptive clocking, extensive programmability to address varied use cases, architectures and workloads, and observability to allow monitoring of droop events, DFS/DVFS transitions, and clock health telemetry.

The ACG IP delivers the fastest frequency shift for droop mitigation in the market, allowing for fast and reliable mitigation for varying workloads and environments. The solution also features a programmable ramp rate to safely recover from a voltage droop and avoid potential ringing on the power delivery network (PDN).

The ACG's comprehensive telemetry is read out through an APB interface, which can be integrated into Synopsys' SLM silicon health and monitoring analytics platforms. It has a IEEE1149.1/1687 interface for connection to test fabric. Droop parameters can be obtained from this system in mission mode and during post-silicon bring-up. Furthermore, configuration settings such as droop and DVFS set points can be adjusted per-module to address various design objectives and architectures.

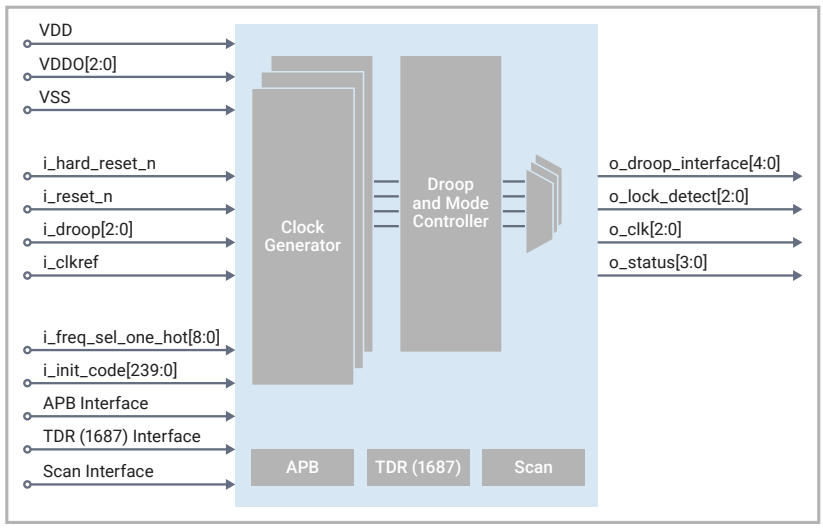

Figure 1: Advanced Clock Generator (ACG) IP

The Synopsys SLM ACG IP product is intrinsically flexible, and area efficient, because it is built as a synthesizable soft IP. By converting traditionally analog

functions into the digital domain, enables the development of feature-rich digital IP that is synthesizable and observable. With proven process portability and minimal area footprint, the ACG IP is ideally suited for large-scale distribution within an SoC.

Droop Response

The Synopsys SLM ACG IP is among the fastest for droop response which minimizes the chance for droop induced timing failure. It also provides the most advanced recovery mechanisms which adapt to the depth and duration of the droop event, which maximizes the performance available. The ACG IP is compatible with 3rd party droop detectors.

Distributed Clocking

A single clock for large, heterogeneous SoCs creates integration complexities such as full-chip routing and localized DFS enablement. Design teams can use distributed clocking to tune their performance needs per processor type or workload. On average, distributed clocking can save SoCs up to 10% energy reduction.

Post Silicon Programming

Silicon changes over time, which means your critical timing paths can also morph, altering setup and hold constraints that could lead to system failures. Users can reprogram the ACG IP after deployment to address the effects of aging circuitry.

Observability and Testability

The Synopsys SLM ACG IP provides clock-specific telemetry for design teams and integration into Synopsys' Silicon Lifecycle Management ecosystem. With the ACG IP users can aggregate metrics like instantaneous clock changes, lock behavior for environmental impact, and average clock frequency.

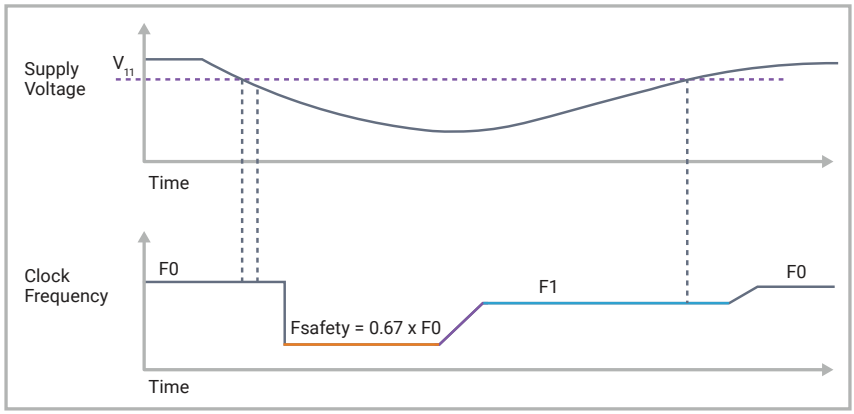

Figure 2: Droop Mitigation with Single-threshold Detector

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.