Model to Hardware Correlation

Silicon Lifecycle Management (SLM) Use Case

Challenges

The semiconductor industry is facing new challenges driven by continual scaling down to smaller design nodes and growth in overall design size and complexity. The increase in transistor density that comes with each new technology node has enabled larger designs but produced significant miscorrelation between predicted and actual silicon behavior. This can lead to serious yield loss due to manufacturing defects, process variation, and environmental conditions. It can also result in increased device power and reduced overall silicon and system performance due to leakage and higher resistance.

Successful chip design requires highly accurate models of silicon behavior throughout the development process. This enables accurate prediction of timing and power so that, when fabricated chips arrive back from the foundry, they operate in accordance with the product specification. Silicon foundries work hard to develop the best possible libraries for their customers, based on both calculations from the underlying physics and measurements from test chips during new process development. The library development process needs a better method to correlate models and silicon results.

Synopsys Solution

Model to Hardware Correlation is an advanced method that allows users to better understand the manufacturing stability of advanced process nodes and to validate how accurately the pre-silicon models can predict post-silicon parametric results. This improves consistency between the behavior predicted by the design models and the actual performance of the hardware. The results can be impressive, as shown by an actual case study.

In this study, the correlation improvement results are based on silicon measurements taken from a 7nm, ~300K gate ring oscillator (RO) design at 0.75v/25°C. The design margin reduction results are calculated based on actual derate removal from the same design.

Figure 1 shows that, compared to the foundry targets shown by the gray lines, the silicon was slower than the Slow-Slow (SS) process corner for some dies at low voltage (0.675V). As the voltage increases, the silicon results get closer to the ideal Typical-Typical (TT) values, eventually running a bit faster. The gap from the Fast-Fast (FF) process corner foundry target to the measured frequency shows that the design is over margined in terms of preventing hold violations. This means the implementation tools will create a larger design than is necessary because they are expecting cases of fast silicon that will not actually happen.

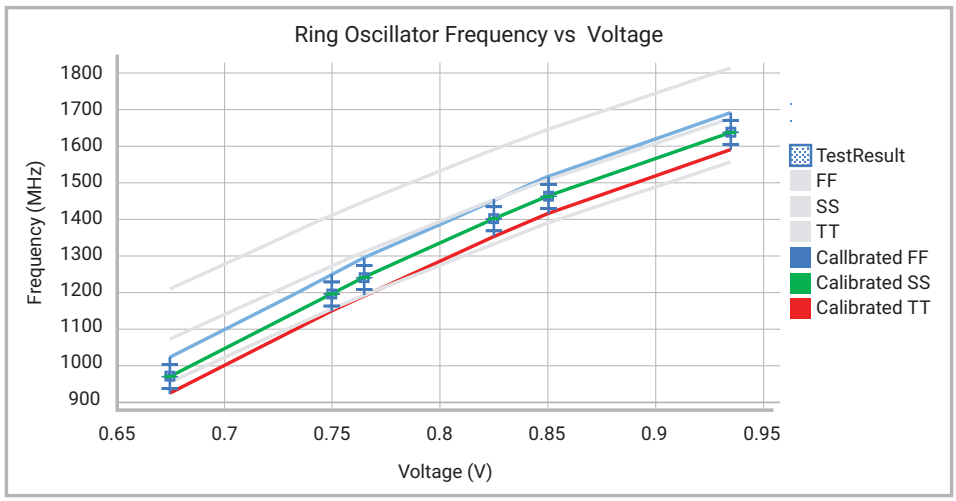

Figure 1: Ring oscillator frequency versus voltage

After calibrating the library based on silicon measurements from production test as depicted by the colored lines in Figure 1, the new TT process corner target aligns with the median of the silicon population. The FF corner is at the maximum frequency of the measured chips, and the SS corner is at the minimum. This means the design tools now account for the actual silicon performance, reducing Vmin fallout and avoiding the hold violation over margining. The result is a 6% correlation improvement between the models and the silicon, enabling a 3.5% reduction in design margins. The more accurate models enable users to identify and fix potential issues early in the design phase, avoiding surprises late in the project timeline or in the fabricated chips.

How It Works

Improved correlation between models and hardware is enabled using Synopsys SLM IP. SLM monitors, including Process Detectors (PDs) and Path Margin Monitors (PMMs), are inserted into the chip alongside customer-supplied ROs early in the design phase. Once early test chips are fabricated, silicon data from the SLM monitors is analyzed by Synopsys Silicon.da data analytics. The analyzed data is fed back to Synopsys PrimeShield, where SPICE models and both foundry and augmented .lib files are combined to create a Compact Timing Power Model (CTPM). This model is a database of calibrated timing information for the library cells that stores sensitivity information of library timing for voltage and process shifts.

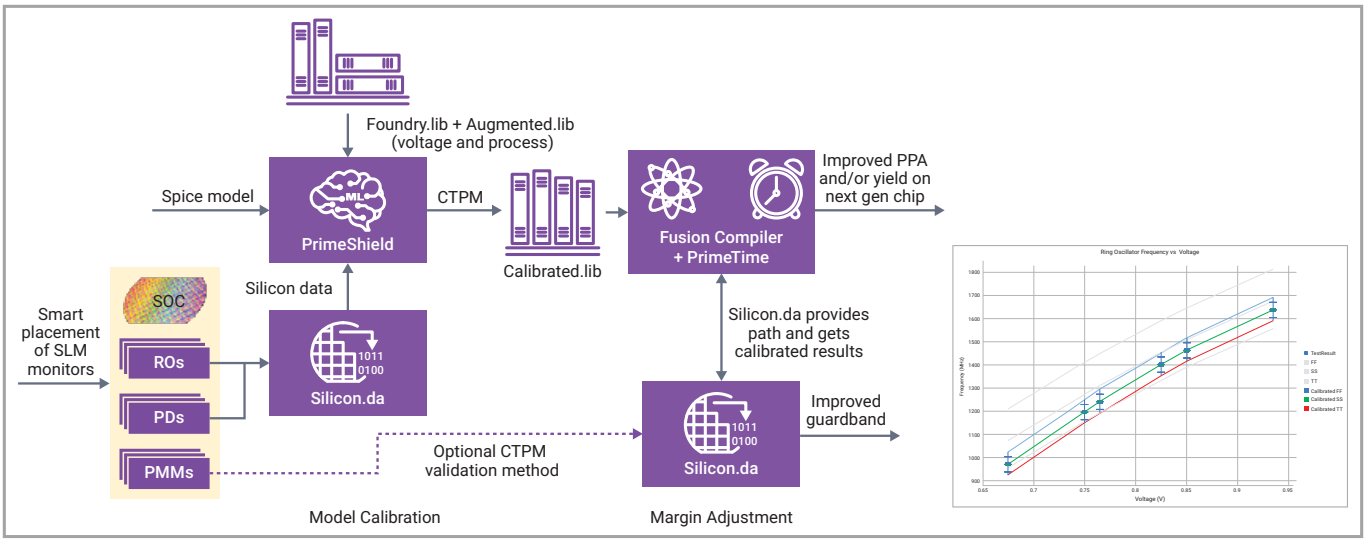

Figure 2: Synopsys SLM Model to Hardware Correlation tool flow

Once the CTPM is generated by PrimeShield, it is used by Synopsys PrimeTime® and Synopsys Fusion Compiler to estimate the change in functional path timing due to voltage and process sensitivity. This correlates the pre-silicon timing and the post-silicon results more accurately. For all future chips belonging to the same process, the calibration results in designs with better power, performance, and area (PPA) characteristics. If the chip being measured in silicon gets a design re-spin, perhaps because it does not meet the product performance specifications, the designers may choose to use the CTPM to improve the original design as well.

The flow shown in Figure 2 is used for generating the CTPM from PrimeShield using silicon data from PDs and ROs, which are needed for all standard cell voltage threshold (VT) classes. PMMs are used on functional design paths to validate the accuracy of the generated CTPM. The silicon margin data extracted from the PMMs during test can be correlated with the pre-silicon margins by using the CTPM. This technique can significantly improve post-silicon to pre-silicon correlation.

Model to hardware correlation produces better designs with lower margins by leveraging real-world measurements from production silicon. These results can also be provided to the foundry to help improve the supplied libraries. All parties benefit from this advanced method, from process engineers to end users, who now have better chips in their electronic products.