Synopsys SLM ext-RAM IP

Highlights

- Performs DRAM (and interconnect) Test and Diagnostics at production test (after DRAM assembly) or/and in-system
- Support for common protocols including DDR 3/4/5 (support for memory modules such as MRDIMM, RDIMM and UDIMM), LPDDR 4/5/5X/6, HBM 2/3/4 and cHBM (custom HBM)
- Foundry process/technology node and DRAM vendor agnostic
- Solution supports any DFI complaint PHY/controller combination
- Low Gate count/small footprint, silicon proven architecture
- Successfully used for several generations of designs targeting automotive, data center, enterprise and HPC

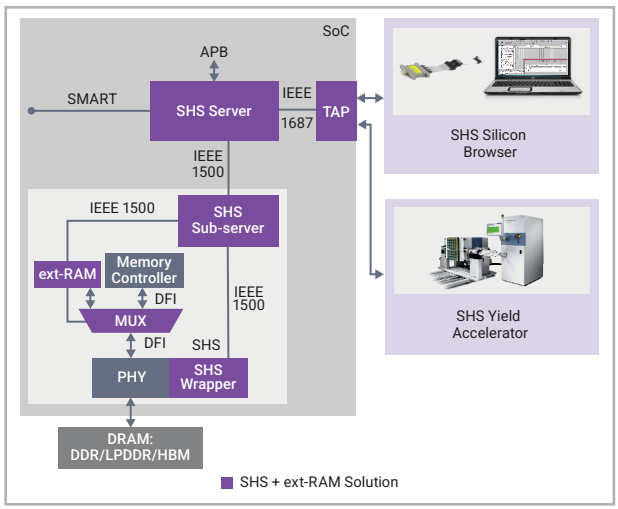
Key Features

- Supports Test, Diagnostics along with BIRA (Built In Redundancy Analysis)* and Post Package Repair (PPR)* to improve in-field reliability
- Addresses all common set of DRAM fault models including stuck-at, coupling, transition, read/write destructive, write mask, address decoder and row hammering
- User can load additional test sequences to programmable Test Algorithm Register (TAR) post-silicon
- Offers programmability for addressing modes and types, address ranges, chip selects, looping mechanism, background patterns, data patterns, timing, DQ trimming and PHY latency
- Stop-on-Nth Error (SONE) Diagnosis with multi level diagnostic information

Overview

Synopsys SLM ext-RAM IP is a comprehensive, user programmable high-quality test and diagnostics solution for logic-to-memory interconnect and DRAM memories. Common use case scenarios for customers leveraging multi die (2.5D/3D-IC) designs include those who ship full systems or multi chip modules (MCM). With the provided scripts and reference design, SoC designers can leverage ext-RAM across the silicon lifecycle by accelerating time to closure during design, maximizing yield during production and increasing reliability with in-field DRAM BIST using Built-In Redundancy Analysis (BIRA)* and Post Package Repair (PPR)*.

The Synopsys SLM ext-RAM IP is commonly deployed in conjunction with the SLM STAR Hierarchical System (SHS) which in turn can be used to automatically initialize the memory PHY via JTAG using pre-validated ATE patterns (for Synopsys PHYs) before initiating ext-RAM during manufacturing test phase.



Key Benefits

- Enables high product/system quality with superior test coverage
- Offers package and board flexibility via user programmability
- Broad interoperability with any 3rd party DFI complaint controller/PHY
- Pre-validated for use with Synopsys PHY's with reference/sample test cases to accelerate design closure
- Independent of foundry/process technology or DRAM vendors

*select memory protocols

High Performance Support

SLM ext-RAM IP allows at-speed test and diagnostics of high bandwidth, low latency external memories with support for single and dual channel interfaces. Optional pipelined flops can be instantiated along with SLM ext-RAM logic to maximize throughput and simplify timing closure.

Test Algorithm Programmability

March based algorithms offering high test coverage with optimal test time are hard coded into the ext-RAM engine. In addition to this, user can request a different/augmented set of algorithms prior to design time while always retaining the ability to load additional algorithmic sequences via JTAG or APB on silicon. Different algorithms can be invoked to trade off test time vs coverage based on use case scenarios (such as Manufacturing test, Power On Self Test (POST) and in-system/in-field).

ATE Test Vector Creation

Synopsys Yield Accelerator (YA) can leverage the SLM ext-RAM IP design database for the user to specify their chip initialization sequences, sequencing of test vectors, generation of testbenches (and firmware for in-system) for their specific SMS/SHS network in the SoC to ultimately generate the ATE vectors in WGL, STIL or other common formats.

Post Silicon Debug and Diagnostics

The user has the choice to perform post silicon debug and diagnostics either on ATE via Synopsys Yield Accelerator (YA) or on early prototype /board using PC/laptop (and commercially available USB to JTAG dongle) via Synopsys Silicon Browser (SiB) software. Stop-on-Nth-Error (SONE) diagnostic support with ability to report all failing addresses, failing row, failing rank and failing bank.

Deliverables

- SLM ext-RAM IP Processor RTL, Sub-server (if needed) and Sample/Reference Server RTL (*.v/*.sv)
- Block level Test benches for verification (*.v/*.sv)
- Datasheets for all RTL blocks (*.ds/*.pdf)
- Synthesis and design constraints (*.sdc)
- Automation scripts for IP integration and verification (*.tcl/*.txt)

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.