SLM Error Correction Code (ECC) IP

Highlights

- Highly automated RTL based flow with complete collateral for user to integrate, validate and synthesize into their design
- Multi-bit error detection and correction
- Configurable performance vs area tradeoff
- Memory vendor independent i.e. can be used with any 3rd party memory IP vendor
- Supports features and collateral needed for use in designs targeting ISO26262 ASIL-D compliance

Key Features

- Configurable Error Detection and Correction: Supports SED, SEC, DED, FED, and advanced multi-bit error detection and correction options
- Multi-Segment ECC Architecture: Automatic or manual segmentation of data words to optimize reliability, timing, and area
- Memory Bit Interleaving: Corrects multi-bit upsets by distributing physically adjacent bits across ECC segments using user-defined interleaving distances
- Write Masking and Wide Memory Support: Supports write masking per user segment and banking of wide memory instances
- Address Error Detection: Detects memory address decoder faults, supporting ISO 26262 safety requirements
- Error Injection for Safety Validation: Single, double, and flexible error injection capabilities without corrupting memory contents
- Pipelining Options: Optional pipelining on ECC encoder and decoder paths to improve throughput

Overview

Synopsys SLM Error Correction Code (ECC) IP is a user-configurable, vendor-independent error-correction solution that improves memory reliability by detecting and correcting transient faults in on chip and embedded memories. Integrated into the Synopsys Silicon Lifecycle Management (SLM) platform, SLM ECC IP supports in-field operation to help ensure data integrity and long-term reliability in advanced SoCs.

As technology nodes scale, memories are increasingly susceptible to soft errors and multi-cell upsets driven by lower supply voltages, higher clock frequencies, and shrinking geometries. SLM ECC IP addresses these challenges with standards based ECC techniques, flexible configuration options, and built-in safety features such as address error detection and error injection—making it well-suited for high-reliability applications in automotive, data-center, and aerospace and defense markets.

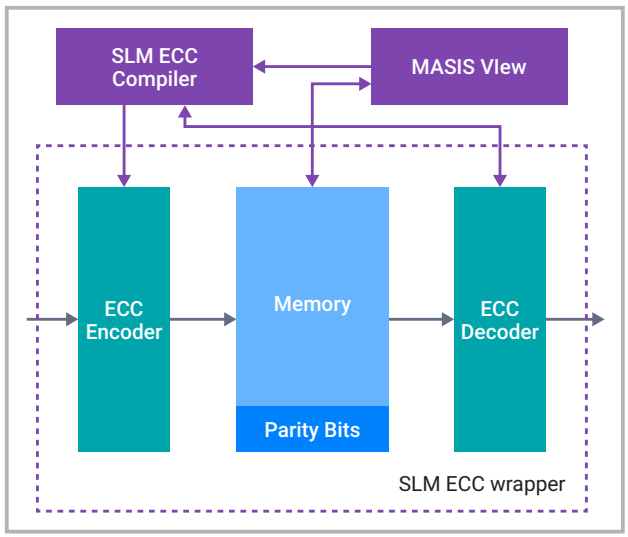

Figure 1: Synopsys SLM Error Correction Code IP

Key Benefits

- **Improved In Field Reliability:** Detects and corrects soft errors and multi cell upsets that increase with advanced nodes, higher frequencies, and lower voltages
- **Functional Safety Ready:** ISO 26262 certified and ASIL D compliant, with built in address error detection and error injection for safety validation
- **Flexible Area vs. Performance Trade Offs:** Configurable ECC segmentation, pipelining, and encoding options to meet system level timing and area goals
- **Vendor Independent and Reusable:** Works with memories from any vendor, simplifying integration and reuse across designs and memory types
- **Automated, Proven Flow:** Generates RTL, testbenches, synthesis scripts, and documentation to reduce integration time and risk

Deliverables

- SLM ECC Compiler generating the following views:
  - SLM ECC SystemVerilog synthesizable RTL (*.sv)
  - Block-level SystemVerilog testbench for verification (*.sv)
  - Datasheet (*.ds)
  - Synthesis script and design constraints (*.sdc)
  - Verification scripts (*.tcl)
- SLM ECC Compiler User Manual (*.pdf).

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.