Silicon Timing Failure Root Cause Analysis (RCA)

Silicon Lifecycle Management (SLM) Use Case

Challenges

The semiconductor industry and EDA vendors have worked hard to accurately predict chip characteristics so that pre-silicon analysis aligns closely with fabricated devices. The libraries delivered by silicon foundries reflect this effort but rely mainly on silicon data from relatively simple test chips for characterizing their libraries. Large, complex designs once fabricated may not correlate as closely with the libraries due to process variation as seen in advanced nodes. The net result is the creation of sub-optimal devices in power, performance, or area (PPA) or worse, requiring a respin of the device if the device specifications are not met.

A new method is needed that gathers silicon data from these larger devices during initial lab qualification, in-ramp, in-production, and even in-field to augment the foundry libraries. Combining this data with powerful analytics can determine the root cause of ilicon timing failures, improve chip yield, and lead to better PPA results for successor projects or for the current project if time permits in the schedule.

Synopsys Solution

Embedding in-chip sensors and monitors is a key element of a robust SLM solution that provides in-silicon health, visibility, and insight at each stage of the semiconductor lifecycle. The types of monitors typically include ring oscillators (ROs) or process detectors (PDs) and path margin monitors (PMMs). Data gathered from these monitors during wafer sort, final test, and system-level test can provide multiple benefits as shown in Figure 1. For refinement of vendor libraries, the focus is mainly on early in-ramp silicon data collection so that the analytics can optimize yield before the chip enters full production especially if there is an opportunity to respin the same device using more optimal libraries.

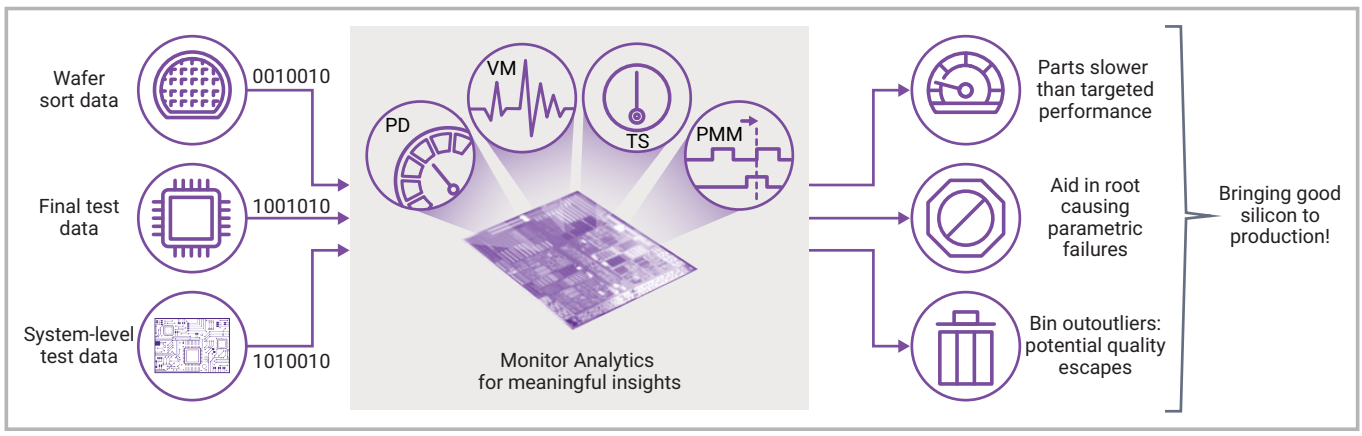

Figure 1: Gathering monitor data and applying analytics to improve yield

The industry leader in this space is the Synopsys Silicon.da solution. With Silicon.da, engineering teams can leverage silicon design, monitor, diagnostic, fab, and production test data to improve key chip production metrics such as quality, yield, and throughput, as well as key silicon operational metrics such as PPA. Traceability and debug of silicon with the aid of correlation techniques across all data types throughout the various test stages of chip production enable quick root cause analysis (RCA) of silicon timing failures along with proper corrective actions.

Silicon.da Monitor Analytics provides automated learning from PDs and PMMs. Synopsys PD IP or customer supplied ROs and Synopsys PMM IP are inserted into the design early in the development phase. As soon as fabricated wafers are available, users can start gathering test data from actual silicon. Monitor Analytics provides insight into any design or process issues that may produce in-ramp or in-production yield loss or highlight sub-optimal silicon power and performance as depicted in Figure 2.

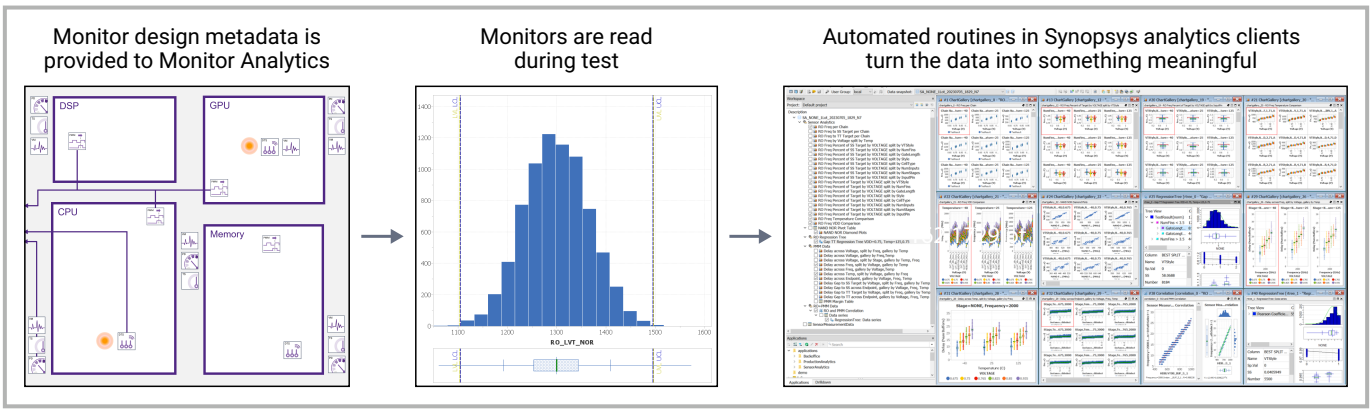

Figure 2: Results of Synopsys Silicon.da Monitor Analytics

For debugging timing related design issues resulting in potential yield loss or silicon failure, Silicon Timing Failure RCA connects silicon data through Silicon.da with TestMAX Diagnosis and PrimeShield timing sensitivity analysis, attempting to identify potential bottleneck cells in a design as possible root causes of performance issues. Timing anomalies identified from gap-to-target analysis using PMM data can also be used as an input to Silicon Timing Failure RCA to identify potential timing related design issues.

How it Works

Silicon Timing Failure RCA is critical in identifying potential bottleneck cells in a design as a possible root cause of performance issues such as failing timing tests. There are several components of this SLM flow:

- Synopsys PD IP or ROs (any source)
- Synopsys PMM IP (optional)
- Silicon.da
- Silicon.da Monitor Analytics (Silicon Timing Failure RCA use case)
- Synopsys TestMAX Diagnosis
- Synopsys PrimeShield timing sensitivity analysis

Monitor Analytics evaluates the observed PD or RO frequency in silicon against the design target. Comparing pre-silicon simulation and post-silicon test results at the design corners provides insights into real-world timing behavior. For example, a fabricated chip might be faster than the fast-fast (FF) design corner, potentially improving performance while raising the risk of hold violations, or setup times might be at risk if paths are slower than the simulated slow-slow (SS) corner. Silicon Timing Failure RCA enables the designers to understand where and how silicon differs from expectations.

PMMs measure the number of delay stages inserted to the end of a path before the path has negative slack. Monitor Analytics charts each path to verify that increasing voltage increases the margin and generates population level charts to see how each voltage, frequency, and temperature affects the margin. These trends of voltage and test frequency give the designers additional insight into how the fabricated chips compare with the design margins. The measured delay is also correlated to the results from the PDs or ROs.

Figure 3 shows how the components of the Synopsys solution are connected. Monitor Analytics and Silicon Timing Failure RCA enable several key and unique enhancements to the traditional design and product test engineering flow:

1. PD/RO monitor data from silicon captured in Silicon.da is sent to PrimeShield with the push of a button
2. PrimeShield uses this silicon data along with the pre-silicon SPICE timing model and libraries to generate a per-die Compact Timing Power Model (CTPM)
3. Synopsys TestMAX diagnostics with transitional delay fault (TDF) information are passed to Silicon.da where they identify the failing paths attributed to the silicon test results that did not match the expected results
4. Silicon.da sends paths that have or are close to having negative slack to PrimeTime where static timing analysis (STA) is run on these paths incorporating the CTPM to calculate calibrated slack and cell delay information on each path
5. PrimeTime sends slack shift analysis back to Silicon.da for further analysis
6. Silicon.da identifies timing sensitive cells that may be contributing to the timing failures
7. Design changes can be made in the next revision of the chip based on STA using libraries calibrated from the results

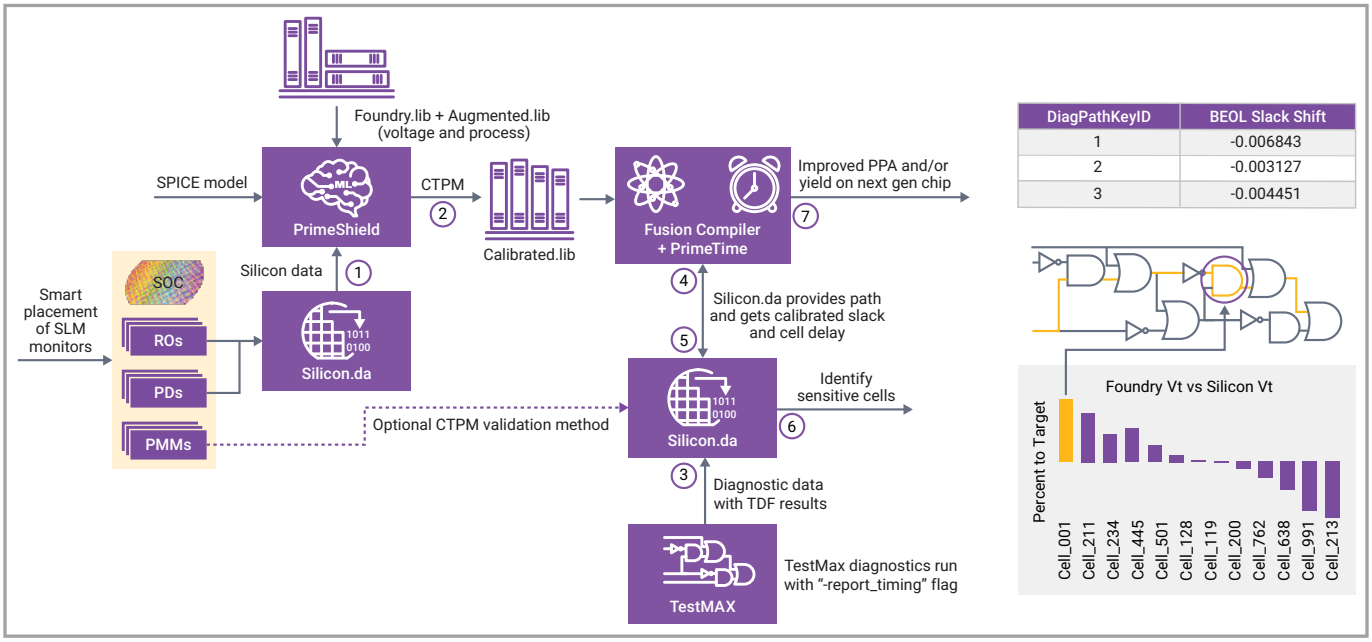

Figure 3: Flow showing library calibration and weak or sensitive cell identification

The Synopsys solution offers an unparalleled method for instantiating SLM monitors, gathering in-ramp silicon results, comparing and correlating these results to design targets, and producing insights that lead to data driven actions for design, fabrication, production test, and system level test. The result is better yield and better PPA results.

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