SYNOPSYS®

DATASHEET

In-Chip Monitoring and Sensing

Distributed PVT sensing solutions for performance optimization, enhanced reliability and analytics enablement

Overview

Driven by the demand for ever-increasing design complexity and device gate density, the adoption of Process, Voltage and Temperature (PVT) monitoring is now critical to successful advanced node chip design. Included within the Silicon Lifecycle Management (SLM) Platform from Synopsys, the In-Chip Monitoring Subsystem (formerly Moortec technology) provides true visibility of real-time chip conditions during in-field operation and allows for a greater understanding of device fabrication. The sensing technology, available from 28nm down to 3nm, allows for life-cycle analytics, increased performance optimisation and enhanced reliability for applications such as Data Center, AI, Automotive, 5G and Consumer.

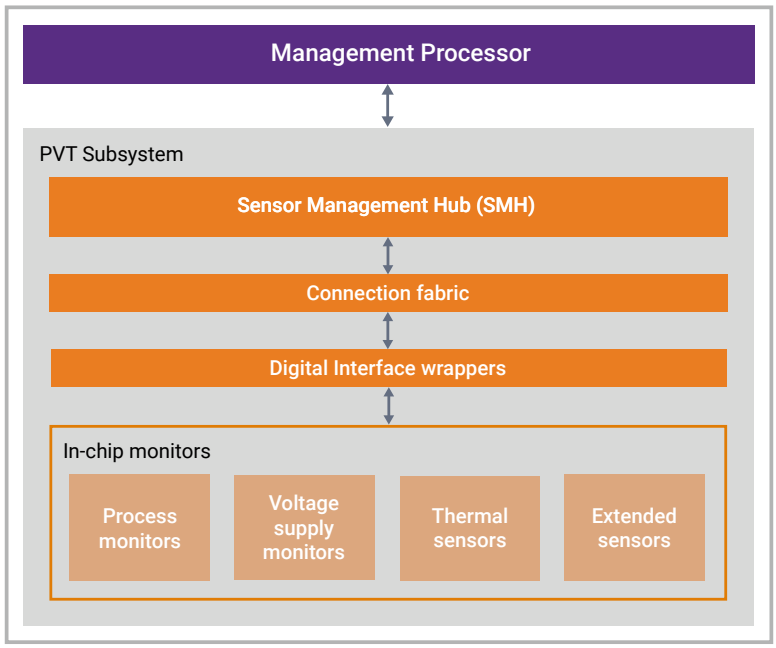

Figure 1: In-chip PVT Subsystem sensing solution

See, Control, Optimize

Once integrated, the monitoring subsystem consists of a suite of embedded sensing IP providing visibility of thermal, supply and process conditions that is accessible via standard interfacing. Through chip assessment and by accurately measuring dynamically changing conditions, the subsystem will support device screening and power/performance optimisation schemes. The localised, low latency sensing solution enables an enhanced opportunity for power reduction, increased data throughput and extended device lifetime at both chip and system level. Features include:

- Real-time thermal mapping across the die
- Localised supply voltage analysis
- Silicon assessment for enhanced device screening and increased performance
- Energy and power optimisation scheme support (DVFS, AVS)
- Extended reliability and support for predictive maintenance and failure

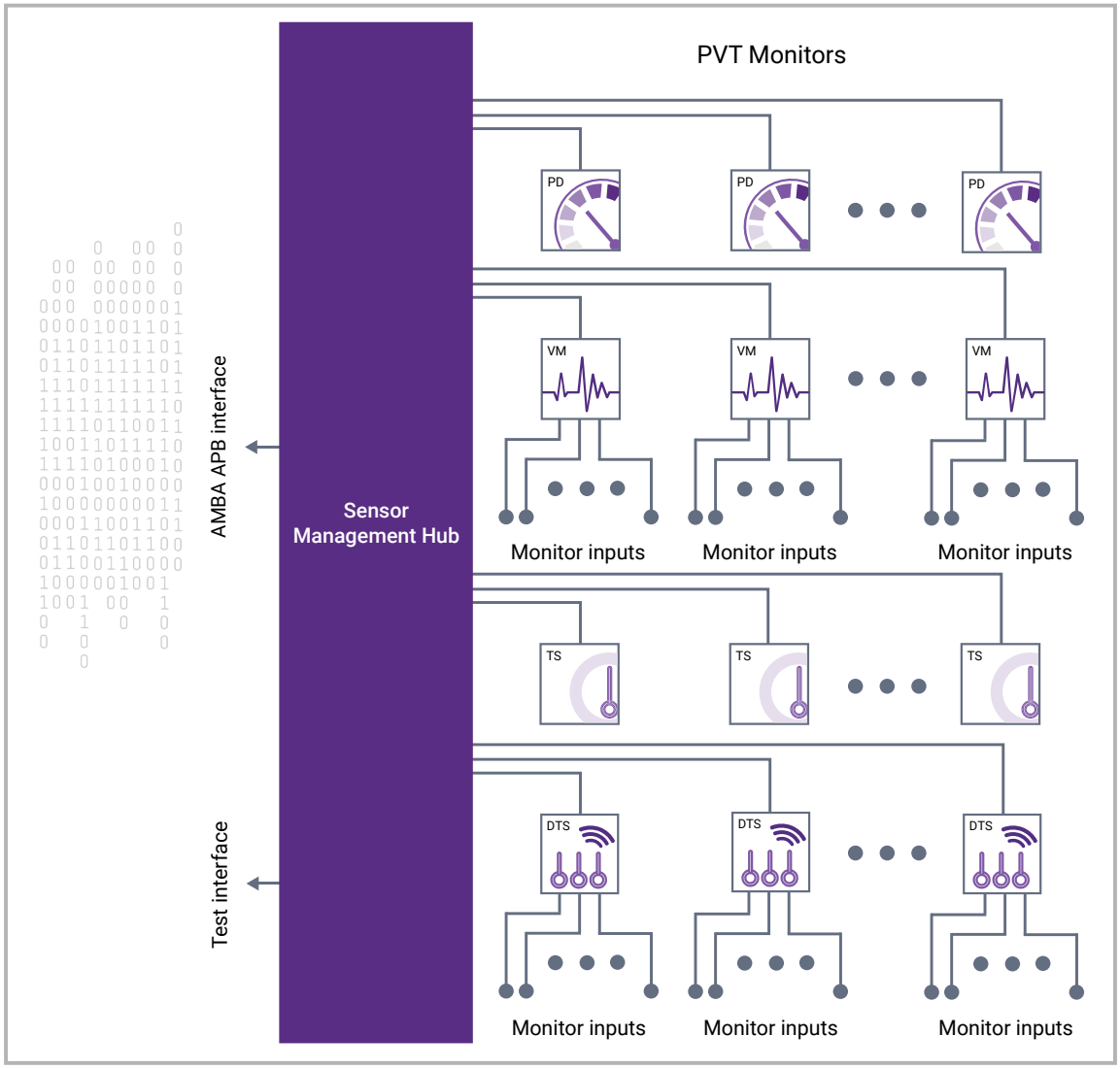

Figure 2: Sensor Management Hub (SMH) and embedded PVT Monitors

Embedded PVT Monitors

Easy to integrate, the embedded monitoring subsystem includes the following key components:

Process Detection (PD)—Assessment of silicon for device screening, age monitoring and tracking of real-time circuit speed performance.

Voltage Monitoring (VM)—High accuracy supply measurement and IR drop analysis during bring-up, production test and in-field device operation.

Thermal Sensing (TS & DTS)—Distributed, low-latency thermal mapping across the die allowing for real-time analysis device activity.

The PVT sensing IP consists of the following features:

- Highly accurate and distributed sensing throughout the die
- Local sensing for multi-processor architectures
- Low latency, real-time measurement
- Small sized remote sense points for low silicon area overhead
- Digital interfacing for reliable sensor communications
- Internal self-checking for sensor health status management providing operational reassurance
- Easy integration with extensive support documentation

Sensor Management Hub (SMH)

The comprehensive subsystem solution consists of a range of sensors communicating to a central Sensor Management Hub (PVT Controller). Configurable by application, the SMH is easily integrated into the design-flow and architecture of the chip. As a major contributor to the Silicon Lifecycle Management platform, the flexible monitoring subsystem accommodates the evolving landscape of PVT sensing, extended sensing and analytics solutions designed to measure in-chip conditions continuously throughout a silicon chip's lifetime, from fabrication to end-of-life. SMH features include:

- Standard interfacing, including AMBA APB and iJTAG test access support
- Flexible configuration when implementing the SMH and register map
- Supports of multiple sensor IP instances
- Auto-polling and configurable sensor duty cycling
- Low system overhead, relieves system control of sensor management tasks
- Alerts, alarms and trigger conditions for safer, more reliable chip operation

Silicon Lifecycle Management Platform

The Synopsys SLM Platform provides insight into critical performance, functionality, reliability, safety, and security challenges for the entirety of a chip's lifespan. This enables the optimization and analytics of operational activities for all participants throughout the life of an SoC. SLM's value is realized by multiple teams involved in the development and delivery of complex silicon solutions, including design, bring-up, test as well as the end-users of systems.

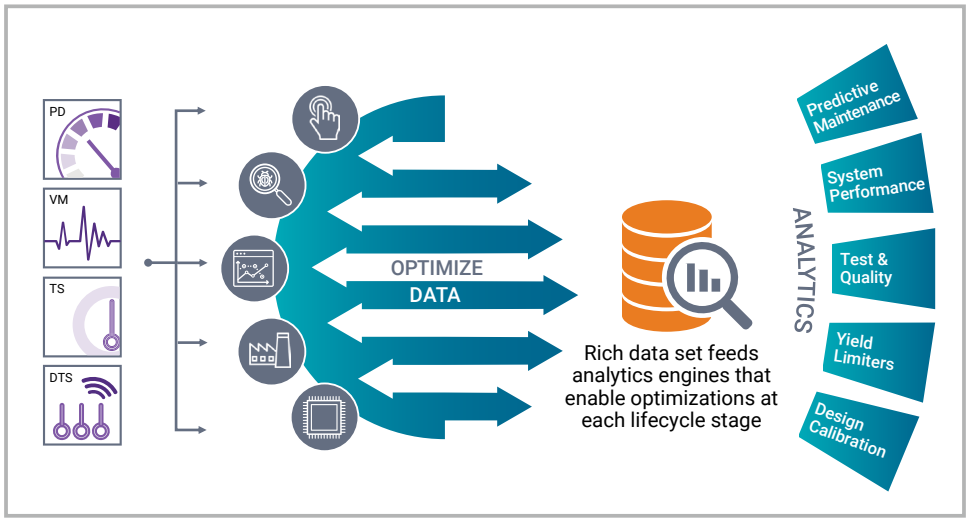

Figure 3: Embedded monitoring, a fundamental component of the Silicon Lifecycle Management (SLM) Platform

Key Benefits:

- Enables tight thermal control of silicon in real-time
- Chip-level and system-level power and data throughput performance optimisation
- Deep real-time insights to chip activity for enhanced product reliability
- Integrated within the Synopsys SLM platform

Synopsys SLM Platform integration:

- SLM family includes:
  - Yield Explorer for design-centric yield management for product ramp and NPI
  - SiliconDash for monitoring and data analytics from the wafer substrate to the end product
  - TestMAX ALE and TestMAX SLT for adaptive high-bandwidth test
  - PrimeShield integration for improved design robustness and silicon lifecycle efficiency

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com, contact your local sales representative or call 650.584.5000