Gap-to-Target Analysis

Silicon Lifecycle Management (SLM) Use Case

Challenges

When it comes to measuring key operational metrics such as power and performance of silicon, in-chip monitors provide the valuable measurements and insights that are required. Data captured from these embedded monitors allows product teams to understand whether their silicon is meeting the required power or performance requirements during the chip manufacturing stage prior to in-field operation. The challenge today is that the analysis of this data, assuming it can be collected, is a manual process and requires the expertise of experienced product engineers to accurately interpret the results. Therefore, a faster and more automated method of detecting gaps between the manufactured chip and the pre-silicon design models is required to address performance limiting yield issues.

Synopsys Solution

Gap-to-target analysis is a technique that allows product teams to characterize their silicon based on the expectations from the foundry model. Data from embedded monitors such as ring oscillators (ROs) can be used to identify potential bottleneck cells or class of cells (e.g., specific Vt, drive strength, cell type, etc.) that are causing low margin and timing fails. Gap-to-target analysis is one of the key applications of the SLM Silicon.da Monitor Analytics solution.

Figure 1 below shows the result of an automated gap-to-target analysis. It is a standard funnel plot depicting one RO chain with the same physical characteristics from within all produced chips tested at several different voltages and compared against the simulated design target from the foundry.

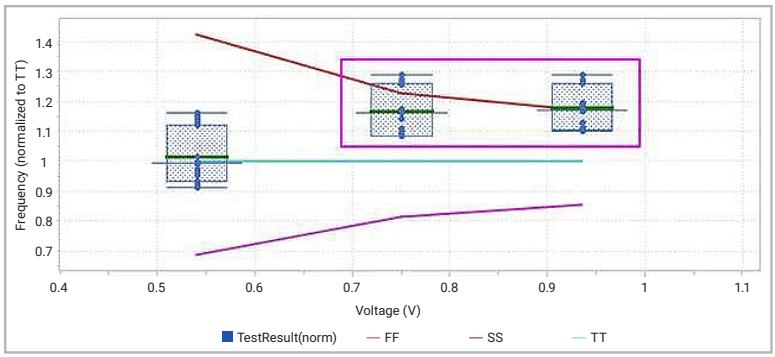

Figure 1: Funnel plot of a single ring oscillator chain tested at three different voltages.

The measured result from the tester is taken and divided by the TT target where TT represents the typical NMOS and typical PMOS simulated timing results. Also shown is the FF (Fast NMOS, Fast PMOS) target and the SS (Slow NMOS, Slow PMOS) target to complete the bounds of the funnel. Both the FF and SS targets are also divided by the TT target to generate their position in the funnel plot.

In this example, as you increase the voltage during testing, half of the population of silicon is running faster than the FF target which is indicative of a scan hold timing violation.

By comparing the RO chain performance in the silicon to the simulation targets, information can be extracted about the silicon health. The set of ring oscillator chains works as a physical design of experiments so designers can understand the performance gaps for various standard cell configurations. For example, it reveals how the number of fins or gate length of a standard cell impacts the gap-to-target.

Key Benefits:

- Identifies which class/characteristic of standard cells, is not performing to the expectation from the model
- Improves device performance

Figure 2 shows the monitor analysis expanded to include three RO chains of uniquely different physical characteristics. Each chain shares the same number of fins, same gate type, and same load cap but different Vt (e.g. threshold voltage) style. They each have their own dedicated Vt style labelled as VT1, VT2, and VT3.

The results show a larger skew between the RO chains at higher voltage where VT2 is roughly on target but VT3 is lagging. Such a skew is indicative of potential timing failures.

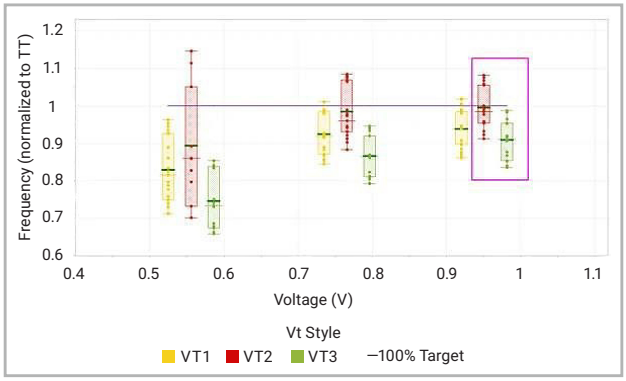

Figure 2: Box plot showing analysis of three unique RO chains with varying Vt.

How it Works

ROs and/or path margin monitor (PMM) IP are embedded early in the design process. During the chip production the metadata from the monitors is combined with the test data results collected during wafer sort and system level testing to run the gap-to-target analysis. The application can run from the Synopsys Silicon.da local or web client.

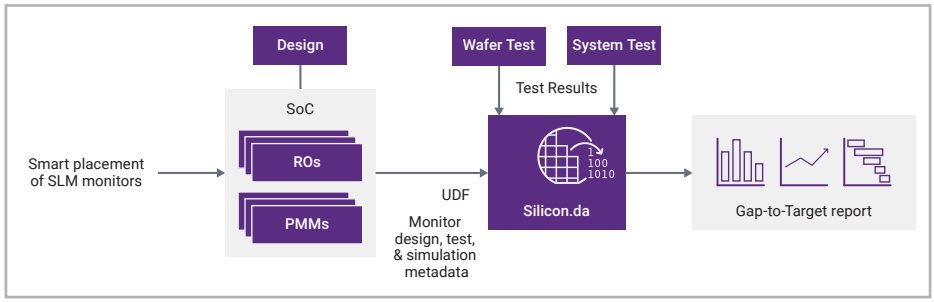

Figure 3: Synopsys Gap-to-Target Analysis flow

During the data integration phase, the Unified Data Format (UDF) file needs to be manually created and integrated into Silicon.da. The UDF file contains sensor-specific design, test and simulation meta data.

The solution allows product teams to characterize their silicon with respect to the expectations from the foundry model. The RO data can also be used to identify potential bottleneck cells or class of cells (e.g., specific Vt, drive strength, cell type, etc.) that are causing low margin and timing fails. Lastly the PMM data can be used to identify specific critical or non-critical functional paths that have low margin for further analysis and debug.

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