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PVT Aware Production Testing

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THE TOPIC OF EMBEDDING PROCESS, voltage, and temperature (PVT) monitors in silicon is heating up. Embedded sensors will help close the loop between Electronic Design Automation (EDA) tool models and system applications, whether on the tester or in the field. But the open-loop power/thermal mitigation application space started many years ago. This is because it was always known that the manufacturing test process excites more of an SoC simultaneously when compared to its mission mode of operation, compounded by a desire to use close-to-maximum test speeds – and this means more power and thermal issues. Academic investigations had confirmed that there certainly was a correlation between switching activity and power. Chip design automation tools began addressing these issues with Design-for-Test (DFT) and Automatic Test Pattern Generation (ATPG) techniques. But the mitigation techniques were driven by trial and error. Embedded PVT monitors as well as other sensors will help ensure that the application of mitigation techniques aligns with the needs of the application. As shown in Figure 1, the correlation between in-chip sensor data and production test data will provide insight to device behaviors and trends, promoting an opportunity for increased test efficiency and reduced device stress.

During the production phase, one or more manufacturing tests are applied to chips. These tests may be applied at the wafer stage or at the packaging stage of the manufacturing process, or both. For large SoCs, these tests are typically applied via scan chains built by the EDA tools. These scan chains allow ATPG tools to easily load all the flip-flops of an SoC with deterministic values while these flip-flops are set to their shift mode of operation. Then, after switching to the mission mode of operation (often called the cap-

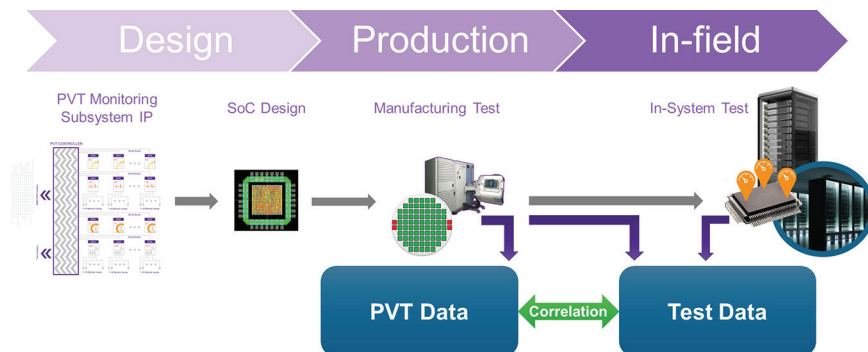


Figure 1. PVT-Aware Testing.

ture phase of the test), one or more functional clocks are applied to the design. Once complete, the flip-flops switch again to their shift mode to unload the results of this pattern and load the next pattern. The offloaded results are compared with the expected results to verify correct operation of the circuitry. Manufacturing defects such as gross failures (open and shorts) and more subtle failures like timing fluctuations due to process variations are detectable when a sufficient set of scan vectors are applied during production test.

Manufacturing test mitigations performed by EDA implementation tools try to address issues during both the shift and capture phases of the testing process. DFT solutions addressing shift power reduction can include q-gating and scan chain loading techniques that either try to reduce the switching activity of the functional cones of logic in the fanout of flops in the scan chains, or reduce the switching activity of the flops performing the shift operations, themselves. Capture power reduction techniques typically leverage clock gating logic, either functional or DFT-only, to reduce the number of clocks firing in the capture phase of a pattern. ATPG solutions try to achieve the same goals as the above hardware mitigation techniques. ATPG is

usually less efficient at solving the problem, but the multiplicity of options can be combined to favorable effect without over-constraining either domain. Recent advances in the modeling of power effects at the cell level in the ATPG domain have led to more accurate matches between power use estimated by the ATPG tools and that measured by sign-off applications, with the side-benefit of fewer patterns.

During the production test of large SoC designs with significant logic gate counts, we see high circuit activity during scan test. The high gate densities within advanced node designs equate to high and pronounced power densities within the die, resulting in what is often irregular self-heating producing localized thermal hot spots. Such hot spots often manifest in or around processor cores, high speed interfaces, and high bandwidth memory (HBM) – a problem which is further exacerbated if the final application possesses a 2.5D or 3D chiplet arrangement, where configurations of stacked die can exhibit higher thermal densities and restricted heat dissipation. If uncontrolled during the testing phase, the scan sequence can result in significant power being consumed and therefore thermal stress being applied to the device at a point of comparative

infancy in its existence. Secondary issues can also emerge with the likelihood of probe pin burn-out being increased. So even before being deployed into the field within a product, the silicon has endured a thermal stress and power consumption unlikely to be seen again during its operational lifetime. Also, worth considering is the data collection metrology of test data collected, as when under an open-loop control scheme, power consumption variability from device to device will be pronounced due to inter-chip deviation of process corners and leakage.

By ‘closing the loop’ with localized, high accuracy, responsive thermal feedback during the scan testing phase, there is an opportunity for PVT-aware decisions to be made by the Automated Test Equipment (ATE) in order to throttle clock frequency, and hence regulate activity and overall power consumption (representative plot shown in Figure 2). The resultant benefit is that by allowing early-life device stress to be reduced and to tighten the spread of results of device power consumptions over many wafers, detrimental effects attributable to heating such as electro-migration, accelerated aging, and decomposition can be minimized.

Counter to the thermal stress issue is a scenario of under-clocked scan frequencies, where the die under test is sufficiently ‘cool’ such that higher speed testing can be accommodated without undue stress. By accurately sensing in-chip temperature conditions, an opportunity is presented to increase and optimize the scan test frequency, hence potentially offering test time improvement. In the absence of being able to apply supply variation schemes, dynamic scan clock frequency adjustment provides a convenient lever with which to control and manage test conditions. Under such control mechanisms, the opportunity for increased test time efficiency will correlate to thermal sensor accuracy and placement granularity. Temperature sensing circuits able to be highly proliferated throughout the die and able minimize measurement errors between sensed temperature versus actual junction temperature allows for tighter scan frequency control and subsequently greater test time optimization. Further benefit can be realized by increasing accuracy through the calibration of thermal sensing circuits, assuming that the test

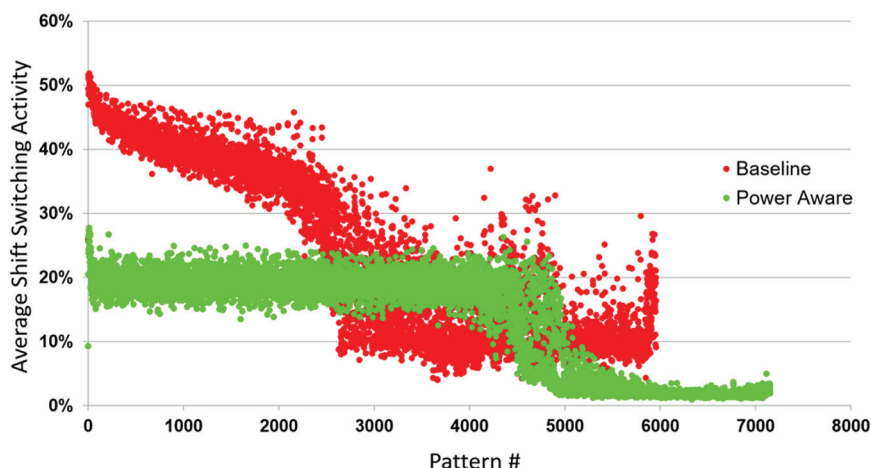


Figure 2. Power-aware testing, controlling switching activity.

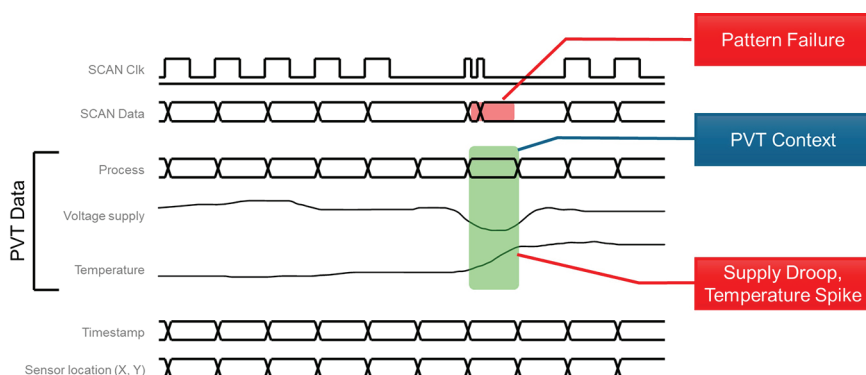


Figure 3. Test failure showing PVT context.

environment is sufficiently temperature controlled, and the time to calibrate can be tolerated within test time budgets. Calibrated sensor accuracies of approximately $\pm 1^\circ\text{C}$ over a commercial temperature range is a reasonable expectation, which will be dependent on the technology node targeted.

The ability to analyze and diagnose the root cause of device failure is enhanced if related data sets can be enriched by supplementary information. By including embedded sensor data, further context can overlay primary results information and provide insight as to why a particular device and scan vector has failed. Elevated localized die temperature, inherent IR drops, dynamic droops in voltage supply, or silicon being manufactured on the extreme edges of process spreads may provide clues as to why devices have failed. A PVT-aware diagnosis of failing parts offers a complementary perspec-

tive to determine failure, but in order to be fully beneficial, the supplemented data requires time-stamping and locality information to be in-sync with scan information. Once these data threads are aligned, not only can the investigation into mid-production failures be aided, but potential in-field failures can be predicted. On this latter point, imagine devices being deemed as ‘good,’ having passed the predetermined suite of tests but also having exhibited anomalous behavior indicated by unusual in-chip sensor readings. Based on the supplementary PVT information, the further color and context provided can allow for better known good die decisions to be made. Pass margins can be adjusted based on sensor information opening the opportunity for underlying failure mechanisms, undetected by binary testing, to be exposed that would otherwise not be exhibited until in-field operation. Adding a greater degree of optics to screening

and selective deployment of silicon is of particular interest to those sectors striving for high reliability, good examples being within automotive contexts where advanced technology silicon is being integrated within product where lifecycles may be in excess of 15 years.

The potential use cases for embedded sensing are far reaching within the test context and presents the industry with an opportunity to further improve upon the two fundamental desires: to improve performance, and to improve semiconductor reliability. The concept of PVT-aware testing applies beyond the production test environment, and opportunities exist to apply the same principles of enhanced, contextualized test and diagnosis to products during mission mode, while operational in its intended system. Such in-field testing is not only beneficial to feedback trends of failure to improve wafer or package testing, but to also provide feedback for generational improvement of the design flow, where margins of the operational design space can be adapted. Adaptive high-bandwidth test solutions applied

to the silicon while in-situ offer the ability to apply manufacturing-level testing through functional interfaces such as Universal Serial Bus (USB) and PCI Express, providing a channel for the efficient transfer of large-scale test data. Concepts of data captured and analytics at each stage of the silicon lifecycle offers much promise. The ability to share meaningful, contextualized information between design, manufacture, test, deployment, and in-field phases of a product's lifecycle is, without doubt, a 'hot topic' worth handling. ♦

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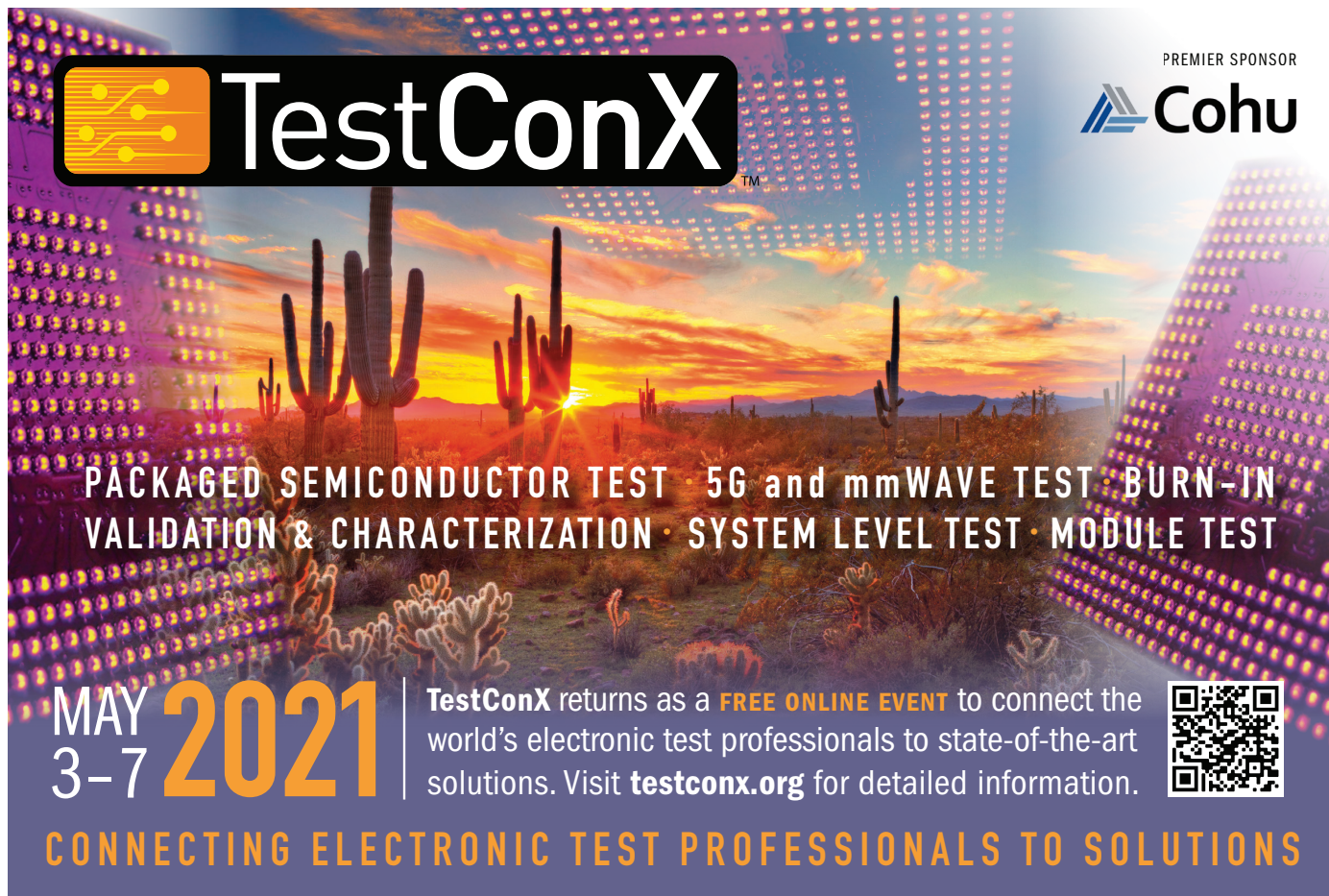
Stephen is Programs Director for the Silicon Lifecycle Management initiative within Synopsys, working with customers to establish value based success through the adoption of in-chip sensing and analytics technologies. Former founder and CEO of Moortec Semiconductor, Stephen has over 25 years' experience working within the electronics and semiconductor design community and in particular in the provision of embedded monitoring solutions for advanced node silicon technologies.

Adam Cron **Principal Engineer, Synopsys**

Adam Cron is a Principal Engineer at Synopsys working with customers worldwide on complex DFT, ATPG, and Security issues for digital ICs. He is part of the Hardware Analytics and Test R&D group, and has been with Synopsys for over 23 years. A Syracuse University graduate, Adam also worked in test-related fields at Motorola and Texas Instruments for over 36 years in the industry. Adam is Chair of IEEE Std 1838 which standardized 3D-IC test access, and is an IEEE Golden Core recipient. He has authored various papers and book chapters through the years, and is frequently a moderator, panelist, or invited speaker at various test- or security-focused conferences.

About Synopsys

Founded in 1986 in North Carolina, USA, today Synopsys is among the "Top 15" largest software companies in the world and a recognized leader in the areas of Electronic Design Automation (EDA), Technology Computer Aided Design (TCAD), and Software Quality, Integrity and Security (APPSEC) tools and services. Headquartered in Mountain View, California, Synopsys employs over 14,000 engineering and support staff globally.




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