Synopsys' Journey to Enable TCAD and EDA Tools for Superconducting Electronics

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***Abstract*— As part of the IARPA sponsored SuperTools program, Synopsys is collaborating with industry and academia experts in the field of low temperature, high performance, and energy efficient Josephson Junction based Superconducting Electronics (SCE) to develop a comprehensive set of physics based Technology Computer Aided Design (TCAD) and Electronic Design Automation (EDA) tools that enable the automation of digital SCE designs, thereby increasing the integration scale, efficiency, and manufacturability of these designs. SCE technology has the potential to propel the Electronics Industry beyond CMOS, enabling a major leap in processing speeds and power efficiency, advancing high-end computing applications, low noise sensors, high-speed communication links, and control logic and interfaces for Quantum Computing systems. The Synopsys team just completed its first two years of Phase 1 of the IARPA sponsored project. I will describe the current state of the project targeting the SFQ5ee fabrication process at MIT Lincoln Laboratory, highlight current tools capabilities, and discuss Synopsys' development plans for Phase 2 which started in October 2019. Many of the tools in this program can be used today to explore the performance and power benefits of Superconducting Electronics.**

Keywords — Josephson Junction (JJ); Superconducting Electronics (SCE); Energy-Efficient Rapid Single Flux Quantum (ERSFQ) Logic; Adiabatic Quantum Flux Parametron (AQFP) Logic; Electronic Design Automation (EDA); Technology Computer Aided Design (TCAD)

I. INTRODUCTION

Superconducting Electronics (SCE) are integrated circuits based on the Josephson Junction (JJ). [1] The JJ's quantization of magnetic flux, which has several inherent technological advantages over CMOS including low power, high speed, and flux quantum sensitivity, makes it a leading candidate for beyond CMOS technology. SCE has the potential to be an enabling technology for a number of applications at the core of the Intelligence Community's mission, including cryogenically operated imagers, quantum limited sensors and communication links, and quantum computing architectures based on superconducting qubits, and potentially other qubit modalities. Furthermore, developments in this area will serve as a control logic and interface foundation for emerging Quantum Information Science (QIS) devices and systems for applications in sensing, communication and information processing.

Despite its potential, JJ based superconductor circuit performance and complexity have fallen short of prior projected benchmarks due to a number of challenges.[2] A lack of suitable design infrastructure has been one of the primary bottlenecks. As a result, fabricated circuits have seen substantially less than optimal operating margin as a function of operating clock frequency that would otherwise be predicted by simulations. While smaller chips have been successfully fabricated in SCE technologies [3], the full potential of SCE can be realized by scaling the chips to larger sizes with increasing complexity. This requires developments in both manufacturing techniques [4] and in the methods and tools used for circuit design. The IARPA SuperTools Program IARPA-BAA-16-03 requested proposals for development of a comprehensive and interoperable set of EDA and TCAD tools to enable design scaling, improve the potential for first time design success, as well as reduce uncertainties in circuit fabrication outcomes.

This paper will discuss the efforts of Synopsys and our collaboration with SCE experts in industry and academia to answer the call of IARPA-BAA-16-03. Synopsys has developed a wide range of EDA and TCAD products used in the design of application specific integrated circuits (ASIC), and is the only commercial entity to offer the full spectrum of tools that span process and material characterization and modeling, device simulation, design implementation and verification tools, manufacturability and yield enhancement tools through high quality fully tested IP for ASIC.

Participation in the IARPA SuperTools program has enabled Synopsys to develop where needed and enhance its tool capabilities to support SCE and deep cryogenic temperatures, 4 Kelvin and below, with an integrated, intrinsic modification of industry proven models and tools, improving upon the extrinsic, patch-work design flows that are currently in use. The combination of validated EDA tools, technical guidance and verification from our SCE experts in industry and academia, and support from the Government sponsored foundry at MIT Lincoln Laboratory for their SCE processes SFQ5ee, aims to enable at-scale demonstrations of SCE technologies. In this

paper we will highlight the results of our participation in Phase 1 of the SuperTools program and will briefly describe our implementation plans for Phase 2 of the program.

II. An Advanced Design Methodology for SuperConducting Electronics based on ASIC Design Technology Co-Optimization (DTCO) design flow

There are two distinct approaches to developing design automation tools for SCE:

1. In the first approach, one starts with a collection of small, custom built, SCE specific point design tools. Effort is then focused on scaling these tools for robustness, capacity, performance, and additional functionality. Unfortunately, as a literature survey shows [5], this approach has not proved fruitful over the last two decades. The methodology and tool gaps that were identified some twenty years ago still exist. The investment and time required to achieve capacity and functionality with high performance and robustness cannot be underestimated. SCE specific tools alone will be challenged to sustainably offer a well-qualified, robust, fully maintained, accurate and high performance software tools that work well with one another.

2. The second approach is to leverage the robust semiconductor methods and tools infrastructure that has evolved synergistically between manufacturing, design, and consumer products over the last fifty years in universities, vertically integrated companies, and at companies that specialize in EDA tools. Adapting SCE design flows and tool requirements to mesh with semiconductor techniques requires changes to tool methodology, functionality and flows.

Synopsys, together with our partners in SCE industry and academia, proposed and received a contract from IARPA to investigate the second approach. Our initial delivery of Phase 1 tool enhancements has so far demonstrated this looks to be a practical way to create a viable and sustainable SCE capability quickly and with minimal investment.

To address the SCE design infrastructure bottleneck, Synopsys has developed an advanced design methodology (Figure 1) to enable realization of complex SCE digital logic circuits with a high degree of model-to-hardware correlation. This approach, inspired by the latest advancements in ASIC Design Technology Co-Optimization (DTCO) design flow and brought to the field of superconductor digital integrated circuit design, is expected to vastly improve model-to-hardware correlation which has been hereto lacking.

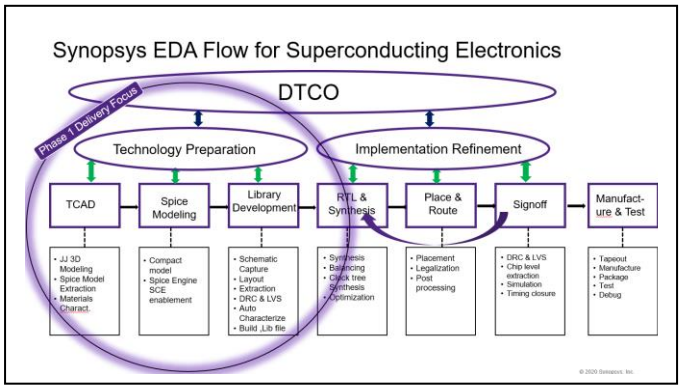

Figure 1: A Tool Methodology for SCE extended from Synopsys' DTCO based ASIC Flow

III. Enhancing TCAD Device and Statistical Compact Models Exrtraction for SuperConducting Electronics

TCAD refers to the use of physics based computer simulation to model semiconductor processes and devices using detailed descriptions of the materials, properties, chemical and physical phenomena that govern the fabrication and behavior of semiconductor devices.

Commercial ASIC TCAD tools have lacked relevant models for SCE technology, so the TCAD tool enhancements have focused on the detailed physical modeling of Josephson Junctions with the aim of supporting scaling to sub-micron junctions as required for high density circuits. The core of the TCAD development in Phase 1 has been the implementation of a self-consistent non-equilibrium Green's function-based algorithm to simulate electrical properties of JJ and arbitrary superconducting geometries in 1 dimension (1D) (Figure 2). The modeled physical phenomena includes the Proximity effect, anomalous density of states, current-phase characteristics, and current-voltage characteristics.

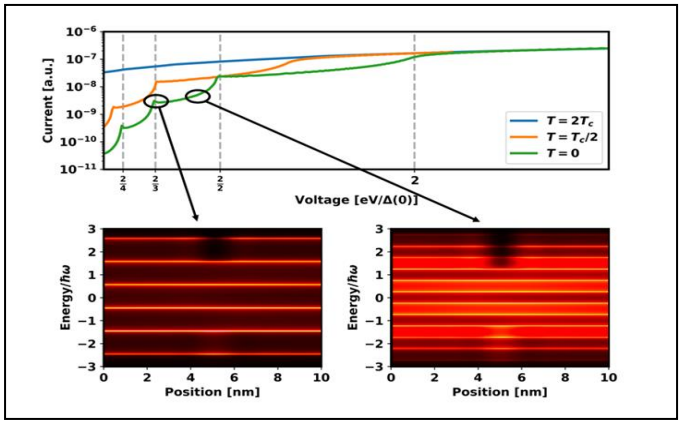

Figure 2: Characteristics of a JJ simulated with recursive Green's function approach

Such detailed physical modeling will permit the calibration of the models to non-ideal junctions so as to reflect the limitations and inherent variability in fabrication processes. These models will be applicable to Superconductor-Insulator-Superconductor (SIS) junctions. Although the models will be verified to data measurements of JJs in the Nb/Al/AlOx/Nb system, they could be extended to other material systems in the future, if necessary.

Statistical Compact Model (SCM) extraction constructs highly accurate nominal and statistical compact models though the linkage of TCAD data, Measurement Data and SPICE simulation with Monte Carlo-based analysis. Synopsys MYSTIC SCM is designed to overcome the challenges of large-scale statistical circuit simulation, analysis and characterization needed to address the device and statistical variability issues prevalent in compact model extraction and optimization. (Figure 3)

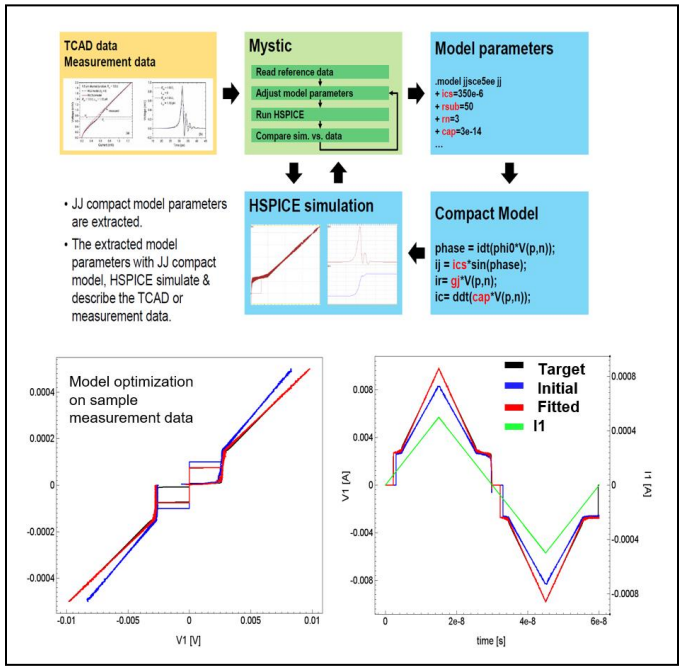

Figure 3: The flow of SCM(MYSTIC), SPICE(HPSICE), and TCAD(SENTATRUS) for extraction of compact model optimization.

The output from TCAD simulations and Statistical Compact Model Extraction delivers the functionality, flexibility and efficiency that is required to construct highly accurate nominal and statistical compact models, serving as target data for SPICE compact modeling, both for nominal and variation analysis.

IV. Enhancing Synopsys Tools for Spice, Inductance, Design Rule Checking (DRC) and Layout-vs-Schematic (LVS) for SuperConducting Electronics

While general SPICE simulators can handle limited SCE devices via a tangent plane approximation within a linear signal processing framework, large SCE design efforts require enhanced support for a nonlinear simulation capability. Synopsys' HSPICE tool has been enhanced to support nonlinear JJ devices via introduction of a Werthamer theory-based model as well as MiTMoJCo microscopic model. A voltage-based PDK with the enhanced RCSJ model was developed and validated with existing public domain tool WRSPICE[7], showing highly correlated output (Figure 4) Important enhancements were added to tune the engine and enable relevant data share with upstream and downstream tools as shown in Advanced Flow Figure 1.

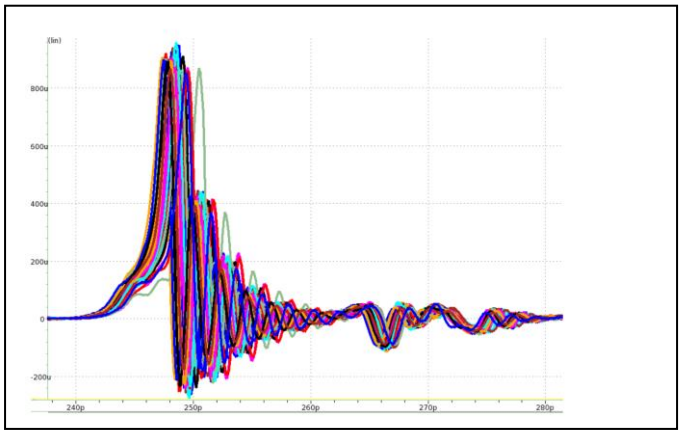

Figure 4: HSPICE Waveform of output SFQ with 300 random samples.

Extraction of inductance from the layout is a critical step whose output needs to be accounted for in the circuit simulation and timing analysis of SCE circuits. Synopsys' STAR RC was enhanced based on FastHenry to enable inductance of relatively small structures for the purpose of creating and calibrating more abstract models, such as geometric pattern matching engines, with fast enough runtime to support extraction of inductance for a full chip and consequently the timing analysis of large scale SCE circuits. Other code was added to STAR to create a table model of inductance as a function of conductor width and length. This model runs very quickly and can handle circuits with millions of JJs. On the DFF the delay error was 12% and on the JTL the delay error was 16%.

While Synopsys' DRC / LVS signoff tool IC Validator required no internal enhancements to support Superconducting Electronics, a significant effort was undertaken to create validated rulesets in support of the MIT Lincoln Laboratory SFQ5ee fabrication process, based on government furnished documents. Capacity testing was completed on a scaled test case containing more than 1 million circular JJs.

V. A SCE Custom Design Enviornment and creation of a PDK for the MIT Lincoln Laboratory SFQ5ee fabrication process

The Synopsys Custom Compiler Platform is a unified suite of design and verification tools that was designed to accelerate the development of robust custom ASIC designs. Anchored by the Custom Compiler custom design environment, the platform features industry-leading circuit simulation performance, and a fast, easy-to-use custom layout editor complemented with best-in-class technologies for parasitic extraction, reliability analysis, and physical verification. For SuperTools Phase 1 delivery goals, Synopsys demonstrated Custom Compiler with a SCE enabled PDK as a useful platform for a SCE designer's cockpit, enabling design entry and layout creation, as well as control of the entire frontend flow of tools including HSPICE, IC Validator (DRC/LVS), and STAR (Extraction). (Figure 5)

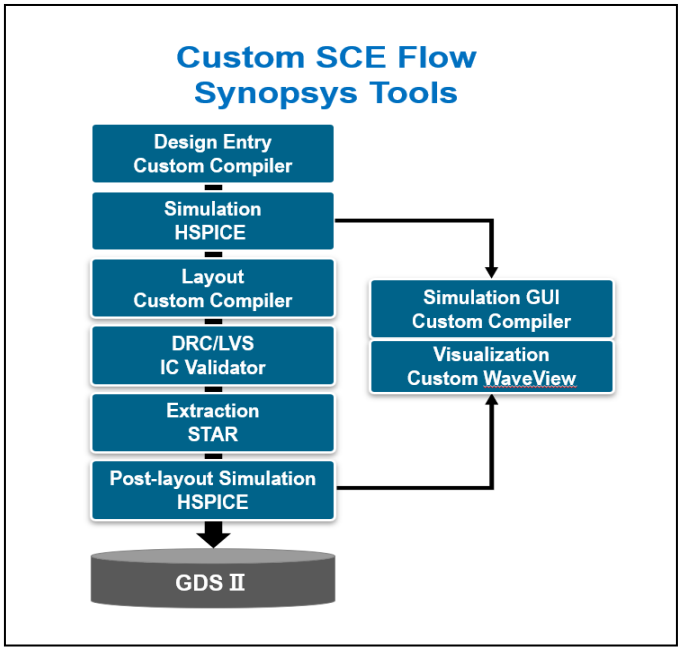

Figure 5: Custom Design SCE Flow enabled Custom Compiler featuring all the tools enabled in Phase 1.

Synopsys created a SCE focused Process Design Kit (PDK) for the MITLL SFQ5ee process based on information provided by IARPA and MIT Lincoln Laboratory. The PDK provides a complete set of SCE design parameters and guides to create custom designs in Synopsys Custom Compiler or any ASIC design environment system supporting the iPDK standard [6]. Device Schematic, Device Layout, Technology File (techfile/tech.db), DRC and LVS runsets and SCE SPICE simulation models are included in the PDK. (Figure 6)

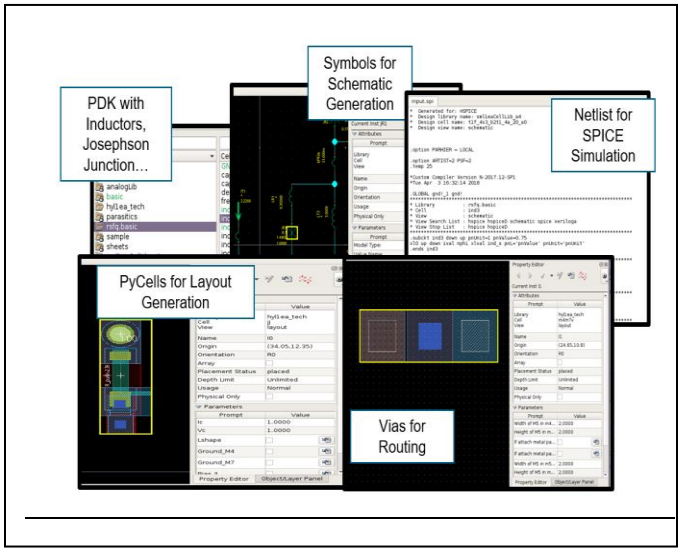

Figure 6: Various components of the Process Design Kit

No software toolset is complete without documentation, examples, training, strong technical support and extensive quality assurance testing. To that end, the Synopsys customer portal SolvNET website houses all software, 11 hours of training videos specifically focused on SCE enabled tool use, helpful application notes and examples. Synopsys Global Technical Support is accessed through SolvNET, directly connecting customers to our tool experts. Regarding Quality Assurance (QA), Synopsys is a leading provider of software quality assurance and integrity tools including Coverity and Black Duck, which are part of a very rigorous testing infrastructure that all Synopsys tools under development endlessly undergo.

VI. Contributrions from our Project Partners

Synopsys partnered with recognized experts in industry and academia to research, contribute and advise on this project to enable a successful Phase 1 delivery. HYPRES Inc. and Professor Nobuyuki Yoshikawa's group at Yokohama National University created cell libraries for ERSFQ and AQFP, the two logic families supported in this project, using our software and performed extensive flow testing. Professor Dmitri Averin of Stony Brook University researched and advised on Werthamer models. Professor Eby Friedman and his students at the University of Rochester researched and advised on optimal solutions for Passive Transmission Lines (PTLs), Power Delivery (PD) and Clock Tree Synthesis (CTS). Dr. Stephen R Whiteley, founder of WRCAD[7], initially advised us and then later joined Synopsys as a member of our technical staff. All have provided Synopsys staff with outstanding counsel as we expanded the tool functionality in this domain.

VII. Next Steps

In Phase 2 of the program, over the next two years Synopsys will address the backend flow of the advanced design methodology shown in Figure 1, as well as further enhance the tools provided in Phase 1 of the program. TCAD will add support for 3D quantum transport simulation of JJs with a hybrid Green Function-Scattering Wave Function approach. MYSTIC will implement temperature dependant extraction and variability analysis. HSPICE will develop advanced models and circuit optimization, as well as explore a DC Phase mode model. STAR will improve Cell and Table model flow, explore support for PTLs, power buses and substrate currents. IC Validator will add smart metal support. HYPRES and Yokohama will refine libraries in support of synthesis and for larger design flow testing. We will also begin an early effort looking into Design-for-Test (DFT) support which is targeted for the final year in Phase 3. In Phase 3, Synopsys will focus on needful improvements and refinements to the tools based on participant feedback and achievements accomplished.

VIII. Conclusion

Synopsys embarked on a government sponsored research contract to explore and enable the automation of large-scale JJ based superconducting circuits. We have concluded Phase 1 establishing a full frontend tool flow, PDK and Libraries enabling SCE custom design projects. For phase 2, we are well poised to effect a full backend flow covering synthesis, place and route, power delivery and clock tree synthesis. It has been an incredible journey to engage and interact with IARPA, our collaborators, the ColdFlux academic team, and the Test and Evaluation Teams including MIT Lincoln Laboratory, NIST, SANDIA National Laboratory, and Laurence Berkeley National Laboratory. We are excited to bring powerful and high-quality EDA and TCAD tools to the growing SCE community. Software tools mature and develop with user feedback, making them even more useful to a wider audience. We invite you to contact the authors to explore the currently implemented flow and look forward to your feedback on how we can help you with your next design challenge.

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About Synopsys

Founded in 1986 in North Carolina, USA, today Synopsys is among the “Top 15” largest software companies in the world and a recognized leader in the areas of Electronic Design Automation (EDA), Technology Computer Aided Design (TCAD), and Software Quality, Integrity and Security (APPSEC) tools and services. Headquartered in Mountain View, California, Synopsys employs over 13,000 engineering and support staff globally.

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