SNUG Israel 2017
Call for Papers FAQ

What is SNUG (Synopsys Users Group)?
SNUG began as a single user conference in 1990 in Silicon Valley. Today, it's a global program with 13 conferences held in 10 countries attended by more than 10,700 users. As SNUG expands to address the complexities of the entire 'Silicon to Software' ecosystem, we continue in our tradition of co-creating a high-quality program that is centered on providing you with hands-on information and insights into today's toughest challenges. SNUG also provides a fantastic opportunity to learn from and network with your gifted peers and Synopsys experts who are eager to learn about your challenges and collaborate with you to solve them.

What do past participants say about SNUG?
"I learned more on the first day alone than I had previously learned reading materials and doing web research."
"Like-minded engineers. . . papers providing good solutions."
"Great forum to get answers and meet/talk to technical experts from Synopsys on their tools and flows."

I've never submitted a paper for SNUG. What is involved?
SNUG has a proven process and a dedicated technical committee who will work with you to create and deliver your real-world experience paper that reflects your innovation using Synopsys tools. The process and deadlines are outlined on the SNUG Israel Author Kit.

When are abstracts due?
The abstract submission deadline is March 6, 2017

When will I know if my paper proposal has been selected?
The SNUG Technical Committee will review the submitted proposals and notify authors whether their proposal has been accepted by March 20, 2017. Once your proposal is accepted, the paper writing process begins.

Do you have some topics for me to think about?
Here is a list to get you started – please do not limit your ideas!

- Analog and Mixed-Signal Simulation (SPICE, FastSPICE)
- Advanced Application Methodologies (ARM, Graphics/GPUs, Processors)
- Advanced Design Methodologies (High Performance, Low Power, Area Optimization, Time to Market)
- Low Power Design, Analysis and Power Reduction Methodologies and Techniques, Static and Dynamic Low Power Verification
- Static and Formal Verification (Advanced linting, Clock and Reset Domain Verification, Timing Exception Verification, Formal Property Verification, Formal Apps)
- Design and Verification Debug (RTL/Gates, Testbench, UVM, Protocol, UPF, Hardware/Software)
- Test Automation (Design-for-Test (DFT), Yield Analysis, ATPG, Diagnostics, Compression)
- Accelerating SoC Verification (Verification Planning & Coverage, Analog-Mixed Signal, UVM Verification)
- Functional Safety Verification (Fault Modeling, Fault Simulation)
- Applying Advanced Technologies (7/10/14/16nm, 3DIC, FinFET)
- Maximizing Results with Established Technology Nodes
- Accelerating Functional ECOs
- Characterization (Standard Cell, Memory, I/Os, Complex Cells)
- FPGA Design and Verification

- Prototyping (Virtual Prototyping, HAPS, Hybrid Prototyping)
- System Design and Validation
- Design Closure and IC Signoff (DRC/LVS, STA, Extraction)
- Full Custom Design and Methodologies
- IP integration into SoCs (Interfaces, Processors, Security, Foundation IP, etc.)
- Addressing Software Quality and Security Concerns
- Managing and Optimizing the Compute Infrastructure for EDA Applications

For more information, please visit the SNUG Call for Papers or Author's Kit

Ready to submit your abstract? Get started now