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Issue 4 | Summer 2012

Wafer FOCUS

In This Issue

Welcome to the Summer 2012 issue of Wafer Focus. In this issue we focus on future device technologies with a contributed article on thin channel transistors and two articles covering recent trends in power electronics. We trust you will find this issue informative and we welcome, as always, your input and feedback on this issue and topics you'd like to see covered in future issues.

Dr. Howard Ko
Sr. VP/GM Silicon Engineering Group, Synopsys

Thin Channel Transistors: The Dawn of a New Era

Klaus Schuegraf, Ph.D., Chief Technology Officer, Silicon Systems Group, Applied Materials

Moore's law has served as a beacon for the semiconductor industry predicting device density and performance improvements for over forty years. Named after Intel Corporation co-founder Gordon E. Moore, the law describes the doubling of integrated circuit transistor count every two years. CMOS logic was invented in 1960s and the technology entered into high volume production in the 1980s because it enabled lower power consumption circuits while keeping to the cadence of Moore's Law. CMOS transistor features were scaled following a simple set of scaling rules proposed by Dennard [1]. Dennard scaling serves as a guideline for predicting the change to basic physical properties such as gate length, gate oxide thickness and junction depth needed to achieve higher transistor density and performance. During the 1990's PC boom, so strong was the demand for increased device performance that gate length was actually scaled faster than called for by the Dennard scaling framework. Further, the operating voltage reductions specified by Dennard were not followed due to system considerations. Taken together, at the turn of the century, these two Dennard deviations resulted in the alarming forecast that high levels of integrated circuit power consumption would place a fundamental constraint on the further progression of Moore's Law.

Continued on page 2

The Coming Revolution in Power Electronics

Ric Borges, TCAD Senior Product Marketing Manager, Synopsys Inc.

While the impetus to keep scaling semiconductor devices along Moore's Law is a dominant driving force in the semiconductor industry, there is another no less relevant semiconductor trend which promises to fundamentally impact the lives of consumers: the evolution of power electronics. The world runs on energy, and its production, storage, distribution and conversion is undergoing fundamental changes. The growing global awareness for the impact of greenhouse gases (GHG) on the Earth's climate and the desire on the part of many nations to secure more diverse and greener sources of energy are primary considerations for policy makers and the energy industries at large.

Diversification of energy production with increased focus on renewable sources of electricity such as wind,

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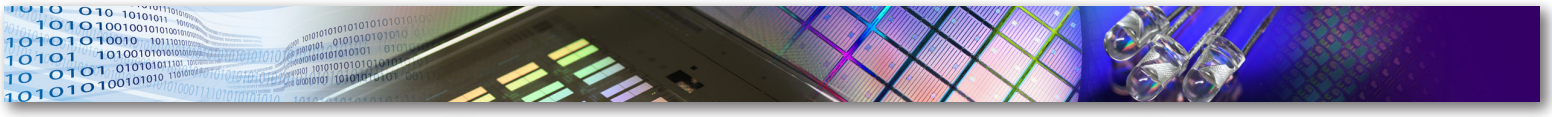


Thin Channel Transistors continued from page 1

In response, new circuit and transistor technologies were invented to keep power consumption in check at a system level. The introduction of new materials into the transistor represented a major breakthrough. In 2003, Intel adopted strain engineering in high-volume manufacturing at 90 nanometer node to increase electron and hole mobility. At subsequent nodes, gate length scaling slowed to keep transistor off-state leakage within acceptable limits. Instead, progressively increasing strain levels enabled continuing increases in device performance. Similarly, the silicon dioxide gate dielectric had reached a thickness limit where tunneling leakage currents were unacceptably high. In 2007, Intel replaced the forty year old silicon dioxide gate dielectric with a new insulator containing hafnium oxide and thereby started upon a new trajectory that allows for gate dielectric thickness scaling without compromising on insulator leakage.

Today, the leakage power continues to be the single biggest challenge to sustaining Moore's law. In this article, we discuss the need for new transistor architectures that will enable tomorrow's lower-power smartphones, tablets and mobile PCs.

New Transistor Architectures Demystified

The long quest for lower off-state current leads to a thin-channel architecture. A transistor serves as an on-off switch. An ideal switch should have high current in its on-state and zero current in its off-state. In reality, a transistor does leak current in its off-state. As the size of the transistor shrinks, the current in the off-state increases exponentially and so does the power consumption. In 2001, the transistor current in off-state was reaching the same level as the on-state current. This resulted in the inability to scale the channel length following Dennard's rule. So, in effect Moore's law continued through gate pitch scaling, but transistor length scaling had stalled. The slowing of transistor channel length reduction would have stalled increases in on-state drive current if not for major technological breakthroughs in strain engineering and high-k metal gates (HKMG). However, to sustain the device packing density according to Moore's law places renewed pressure on a solution to scale gate lengths below 25nm.

For such short channel lengths, low off-state leakage current can only be achieved if the electric field applied on the transistor gate nearly fully controls the electrons or holes moving in the channel. This may be achieved if the silicon body of the transistor channel is thin enough (< 12 nanometers). This challenge has sparked distinct approaches amongst semiconductor chip makers. One approach is to build a three-dimensional FinFET or a tri-gate transistor where the channel is a "fin" of silicon surrounded by a gate on three of its sides. A second school of thought extends conventional planar transistor scaling, but employs an ultra-thin silicon channel which sits on an insulator, called an ultra-thin body silicon-on-insulator or UTB-SOI.

In the late 1990's, Professor Chenming Hu of the Electrical Engineering Department at the University of California at Berkeley led an ambitious study to determine pathways forward. This pioneering study demonstrated the feasibility of both UTB-SOI and FinFET structures at gate lengths less than 20nm and later below 10nm for FinFETs.

Gate Architecture Schematics

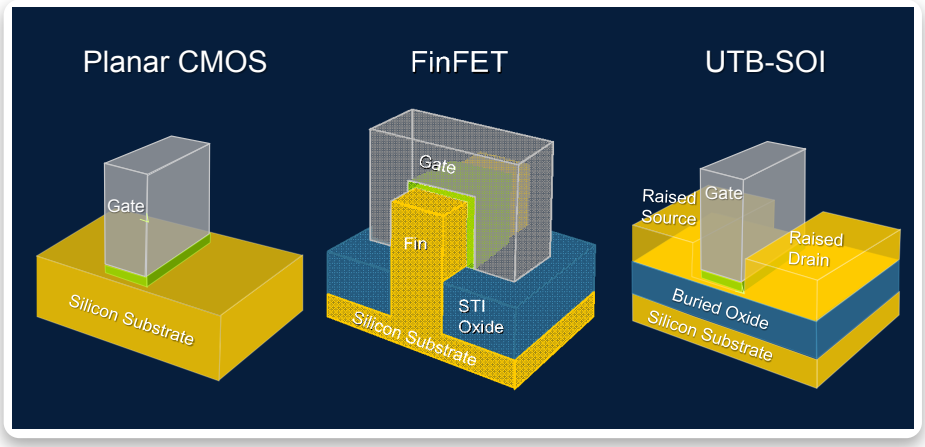
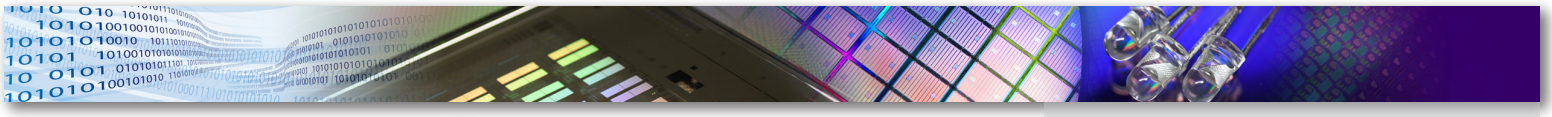
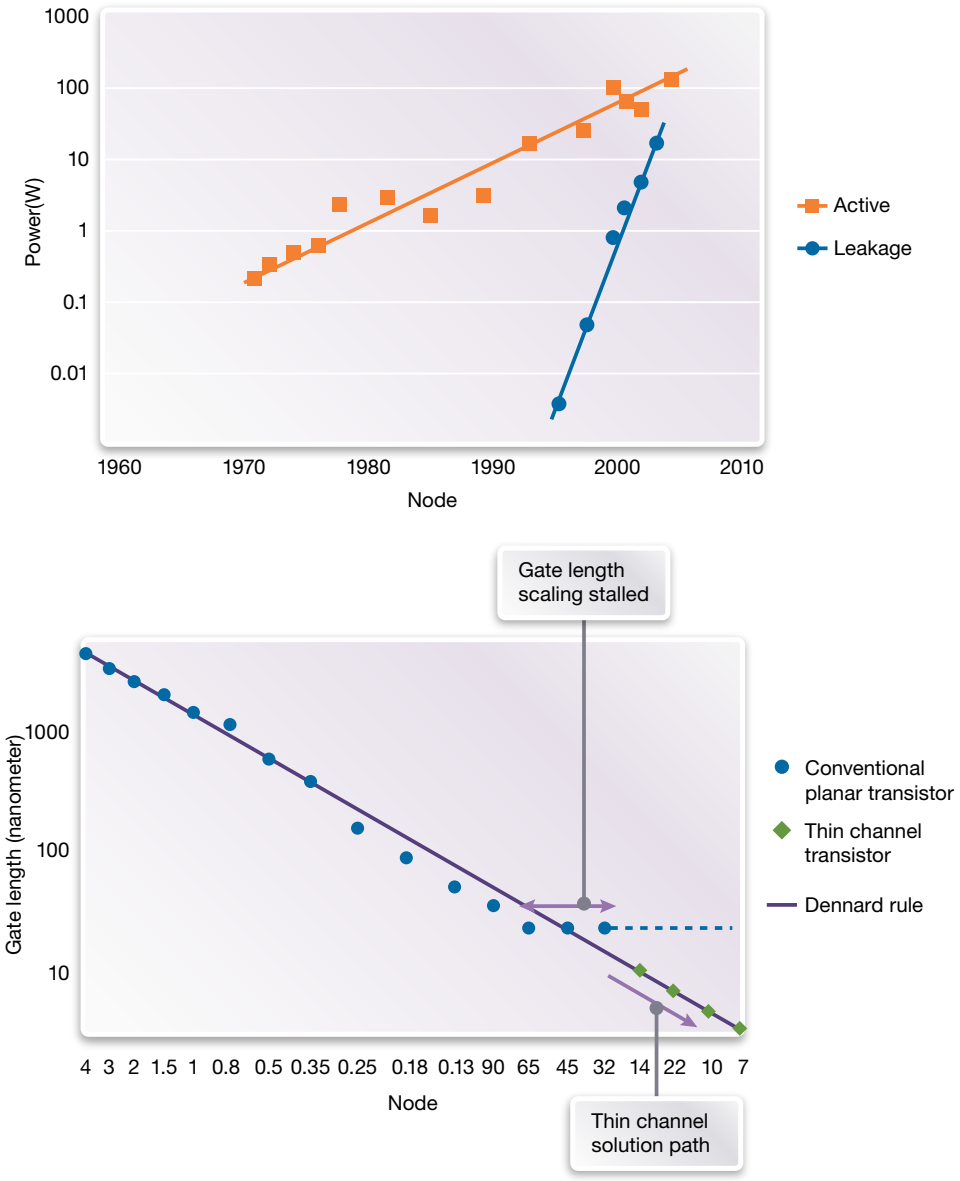


Figure 1: In the next few years, traditional planar CMOS field-effect transistors (left), will be replaced by alternate architectures that boost the gate's control of the channel. The UTB SOI (right) replaces the bulk silicon channel with a thin layer of silicon mounted on insulator. The FinFET (center) turns the transistor channel on its side and wraps the gate around three sides.

The world of FinFET

In May 2011, Intel announced a production-worthy tri-gate solution for the 22 nanometer technology node. This proved for Intel to have been a formidable manufacturing challenge, as characterized by Dr. Kaizad Mistry, Intel's Vice President of Technology and Manufacturing, who has been involved with each of Intel's major technology breakthroughs for the last decade: "The biggest challenge with the tri-gate technology is to have a robust manufacturing process, to pattern the fins with the required fidelity of the fin width and height, and do





Source: Gordon Moore, Intel. ISSCC 2003

Figure 2a, 2b: As transistor channel length was scaled down every two-three years, leakage power dissipation (consumed during idle state) increased exponentially until it became almost equivalent to active power dissipation (consumed during computation). Switching to alternate architectures will allow continued scaling with better transistor density and performance.

it for billions of transistors." However, the transistor cost and performance benefit of accomplishing this transition were large, according to Dr. Mark Bohr, Intel's Senior Fellow of Technology and Manufacturing (and National Academy of Engineering fellow): "The low-voltage and low-power benefits far exceed what we typically see from one process generation to the next."

What's New

TCAD

In June 2012, we released TCAD Sentaurus 2012.06, with new models for plasma doping (applicable to FinFETs), variability from grains in metal gates, 3D Monte Carlo device simulation, and thermoelectric transport, among others. We also introduced a new visualization tool, Sentaurus Visual, which offers significantly improved visualization and scripting capabilities over the current visualizer.

In April 2012 we delivered a webinar on the application of Sentaurus to the design of electrostatic discharge (ESD) protection structures, a major reliability concern in the semiconductor industry. The webinar can be viewed on demand. To access it please select the Webinars tab on the Synopsys TCAD website: http://www.synopsys.com/Tools/TCAD

Mask Synthesis

Synopsys completed the technology acquisition of Luminescent's Mask Patterning Division. Luminescent's leading-edge inverse lithography technology (ILT) will be integrated into Proteus' high-volume manufacturing platform later this year to offer advanced applications like hotspot fixing within the Proteus Pipeline Technology.

The Mask Synthesis Team hosted another successful Technical Forum at the SPIE 2012 Advanced Lithography with over 70 technologists in attendance. This year's event offered presentations from Dr. Chris Mack, Dr. Franklin Kalk from Toppan, Hironobu Taoka from Renesas, and Dr. Seung-Hune Yang from Samsung http://synopsys.com/tools/manufacturing/pages/spie-advanced-lithography-2012.aspx.

Look for the Proteus and Sentaurus Lithography Teams next in the Korea Workshop this August and SPIE Photomask Technology (aka BACUS) in September.

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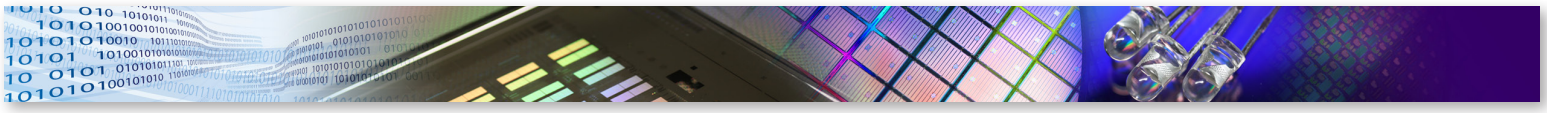


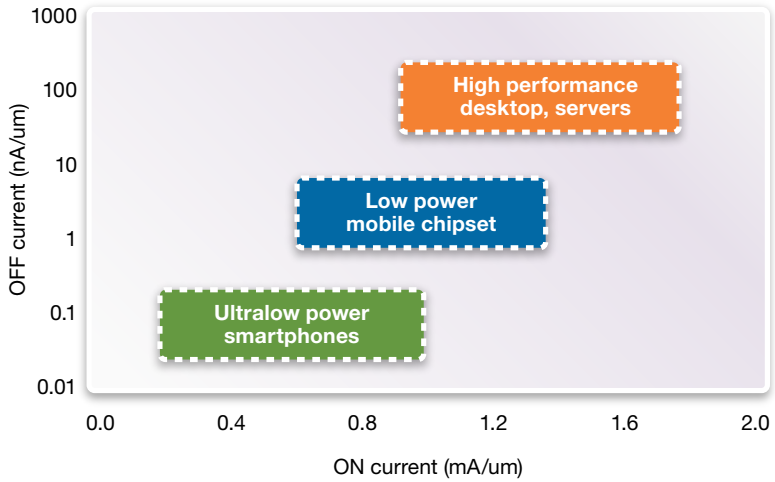


Figure 3: Transistor OFF current versus ON current. Transistors are designed differently for different end applications. Transistors used for ultra-low power applications have relatively longer channel length (+5 nanometers) with lower OFF current and lower ON current. Transistors used for high performance applications have relatively shorter channel length (-5nanometers) with highest OFF current and highest ON current.

FinFET architecture provides greater electrostatic control of the conduction channel through the gate electrode. The current flows in a small silicon fin having an approximately rectangular cross-section with three sides that are covered by the gate. Design estimates call for 12 nanometer fin widths and 24 nanometer fin heights for a channel length of 25 nanometers. The multiple surface channels (that carry on-state current) and all sub-surface leakage paths (that carry off-state current) are in optimal close proximity to a gate. A high on-state current results from the cumulative contribution of multiple channel surfaces. The undesired off-state power consumption is greatly reduced because of effective control from close-proximity gates. The FinFET design thereby enables chips to cover the computing continuum from high speed servers to ultra-low power smartphones.

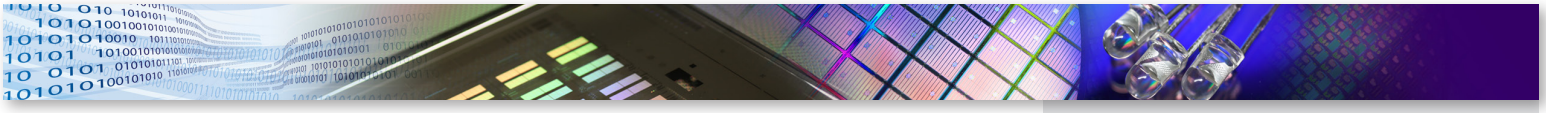
The world of UTB-SOI

Proponents of the UTB-SOI school of thought often highlight the relative simplicity of this technology in retaining the existing planar structure and minimizing changes needed in the manufacturing process flow. Dr. Thomas Skotnicki, STMicroelectronics Fellow and Director of Advanced Devices remarks that "CMOS integration…on SOI… may be technologically much simpler than any known Double-Gate technology, and thus may be a [work] horse for end-of-the-roadmap CMOS." This is echoed by Dr. Olivier Faynot, the Innovative Devices Laboratory Head of CEA-Leti: "Fully depleted SOI devices are easier to integrate than the non-planar devices like FinFETs."

UTB-SOI architecture consists of a thin silicon channel held by an insulator on a silicon substrate. Design estimates call for a silicon body thickness of 6 nanometers for a channel length of 25 nanometers. This thickness requirement is half the fin width thickness of the FinFET architecture. Here the current carrying surface is along one plane only due to the continuation of planar CMOS technology unlike the cumulative contribution seen from multiple surfaces on FinFET transistors. The sub-surface leakage paths (off-state current) are in close proximity to the gate and are under its strong electrostatic control which greatly reduces the undesired off-state power consumption. The UTB-SOI design thereby enables chips that excel in the segment of ultra-low power devices.

Manufacturing FinFET Architecture

There are many challenges in implementing FinFETs in production. We focus on key ones in this section. The first set of challenges arises from the requirement to fabricate very narrow and uniform fins. For a 20 nanometer transistor, a fin width of 10 nanometers will be required with a width uniformity of 1 nanometer for acceptable performance and leakage characteristics. Double patterning technology solutions can be employed to precisely define these thin tall silicon fins. Two approaches are being pursued in double patterning: a Litho-Etch-Litho-Etch patterning scheme and the Self-Aligned Double Patterning (SADP) scheme. In the latter, the wafer is exposed to two different reticles which are each offset from one another to achieve a net effect of a smaller feature size. It is desired that the etching process produce vertical (90° angle), smooth, void-free surfaces to optimize electron transport in on-state current. Furthermore, the precisely formed fins undergo many subsequent thermal treatment, doping, film deposition and film removal process steps. It is extremely critical to keep the fin dimensions unchanged in these process steps because any deviation caused can lead to adverse effects in final device performance. Another set of challenges pertains to the processing of the gate stack, the layered material stack that includes gate insulator and gate electrode. The gate insulator and metal gate must almost perfectly conform to the 3D body of the fin. Atomic Layer Deposition (ALD) technology will likely be required to deposit such thin and highly conformal film layers.



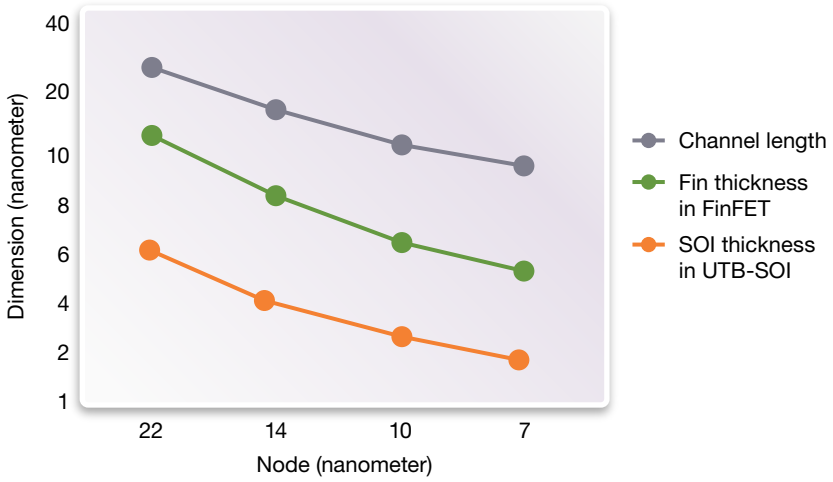


Figure 4: Estimated channel length, Fin thickness in FinFET, and SOI thickness in UTB-SOI for future technology nodes.

Node (nanometer)	22	14	10	7
Contacted gate pitch	80	60	40	30
Gate length	24	16	11	8
FinFET Fin width	12	8	6	4
FinFET Fin height	30	22	14	10
UTB-SOI thickness	6	4	3	2

Figure 5: Estimated FinFET fin dimensions (width and height) and UTB-FET UTB-SOI thickness for future technology nodes

Also, the metal material selection for NMOS and PMOS must be different in order to realize the performance benefit of the "gate-last" HKMG integration scheme employed today. For future technology nodes, the fin pitch will need to be scaled down to a very small level such that little space is left for insulator and metal film deposition. It is conceivable that on an advanced 7 nanometer node with a fin pitch of 30 nanometers, the thickness of gate insulator and gate metal layers combined will be in the range of 12 nanometers.

Beyond these geometrical considerations, there are other key challenges which emanate from the electrical requirements of the device.

Given the narrow width of the fins, there is inadequate silicon present for consumption in the formation of a recessed structure, so the source drain contacts have to be in a raised configuration. Raised structures have a high doping to lower the intrinsic resistance and, because they grow out of the body of the fin, they are located in close proximity to the gate which creates an unwanted

What's New continued from page 3

Mask Data Prep

The latest release of CATS (2011.03-SP8) has comprehensive support for management and scheduling of resources required for distributed processing jobs. CATS users can now allocate resources and priorities to maximize utilization of CPU cores and software licenses. In the upcoming release (2012.09) CATS MRCC capability has been expanded to include polygon sizing, pattern generation and matching and additional data creation commands allowing users to develop efficient verification and metrology flows. In addition, CATS continues to offer faster turn-around time for data prep while shrinking the output filesize to enable higher mask manufacturing throughput. known marginal locations, and enable automated response actions for the high value defects captured on wafers in progress.

Manufacturing Yield Management

With Synopsys' acquisition of Magma Design Automation, the Silicon Engineering Group now has responsibility for the Camelot failure analysis and Yield Manager yield management products. These additions enhance Synopsys' ability to enable customers to improve yield of ICs and new technology nodes.

The latest release of Yield Explorer v2012.06 offers further enhancements on the proven Automated Volume Diagnostics application and enables fabless-foundry collaboration while retaining the privacy of sensitive data on either side.

GLOBALFOUNDRIES and Synopsys delivered a webinar explaining our fabless-foundry collaboration model for design-centric yield enhancement using Yield Explorer.

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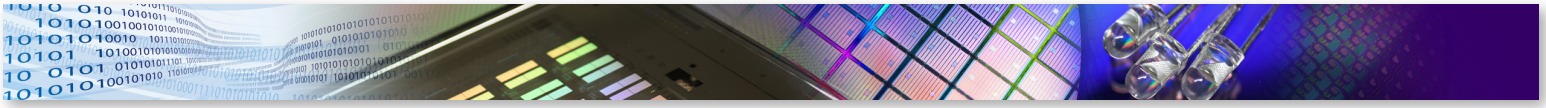


capacitive coupling and power drain. New materials that reduce the coupling through usage of a lower dielectric constant layer between them, like a low-k spacer or others, will be needed. The regions connecting the raised source and drain structures to the gated portion of the fin are known as the extension regions.

The extension regions are part of the fin with same 3D morphology. Doping processes that are normally done to lower the resistance of these regions now have to provide conformal coverage across all three surfaces of the fins. If the doping is non-conformal, electrons tend to accumulate to the highly doped region (path of least resistance) leading to carrier crowding which then results in low on-state current. Current beam-line implantation techniques are non-conformal as the sidewalls of the fins receive a single dose while top surface can receive double the dose in that time. New technologies such as plasma-based doping, vapor phase deposition or atomic layer doping will be needed to provide the desired conformal doping.

Since virtually all advanced planar transistors today employ some form of strain engineering to enhance carrier mobility, there is also ongoing work to apply strain engineering to FinFETs. In FinFETs, strain-inducing capping layers have been attempted using silicon nitride films deposited by chemical vapor deposition (CVD). The magnitude and type of strain (e.g. tensile versus compressive) may be adjusted by modulating the deposition conditions, especially temperature. However, the tight gate and fin pitch dimensions put a limit on the amount of strain that can be induced in this approach. A second method involves the use of a silicon-rich solid solution such as silicon-germanium (PMOS) or silicon-carbon (NMOS) as source drain regions on the two ends of the channel to induce a channel strain. Due to the 3D nature of the fin, this strain transfer from source drain regions to the channel is less efficient than in planar devices. To continue scaling, radical approaches through new materials for channel in place of silicon that provide very high electron and hole mobility such as indium-gallium-arsenide and silicon-germanium solid solution as well as pure germanium are seeing extensive research investment.

Despite these challenges and others not mentioned here, the semiconductor industry, with its history of ingenuity and innovation, is expected to systematically reach solutions to enable the manufacturing of FinFET technologies at the 14nm node and beyond.

Manufacturing UTB-SOI

UTB-SOI also faces its own set of technology challenges for this architecture to be elevated to mainstream production. The primary challenge is in controlling the thickness of the thin silicon channel to within very strict tolerances.

For a 14nm device, the required silicon thickness is approximately 5 nanometers and any variation greater than 0.5 nanometers will negatively impact on-state current (performance) and off-state current (power consumption). A 1 nanometer deviation towards thicker silicon channels can result in as much as 10-time higher power consumption.

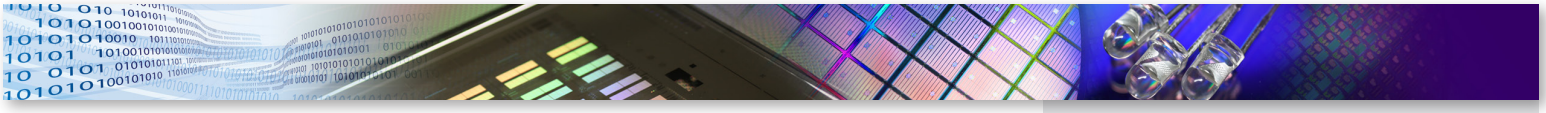
Also, as in the case of FinFETs,given the thin silicon layer design, source drain terminal contacts now have to be in a raised configuration, with the similar challenge that their location in close proximity to the gate creates an unwanted capacitive coupling between the two and causes power drain. New materials that reduce the coupling through usage of a lower dielectric constant layer between them like a low-k spacer or others will be needed.

Yet another challenge is in the formation of extension regions for source-drain structures. The extension regions are small areas at the tips of the channel that are in contact with source and drain terminals. The function of these regions is to extract current from the channel and pass it to source and drain. They need to have low electrical resistance to minimize power losses and to retain a good on-state channel current for high performance. Higher doping can lower the resistance; however, ion beam implantation can cause crystalline damage to these thin regions worsening the resistance problem. Novel doping techniques based on epitaxial growth and controlled diffusion will be enabling solutions for future nodes. The last key challenge is in gate stack deposition. The required gate insulator electrical thickness will be extremely small, around 0.5 nanometers for a 7 nanometer device. Precise control with minimal variability in thickness will be a big challenge to overcome. Atomic layer deposition technology is likely to be required to deliver the needed precision. The metal gate electrodes also need to be precisely manufactured, requiring CVD or ALD technologies in addition to PVD technologies in order to fill small gaps and maintain good transistor performance.

Revolution vs. Evolution in Advanced Transistor Architectures

Two thin channel architectures, FinFET and UTB-SOI, and their associated design and manufacturing aspects have been reviewed. Both were conceived a decade ago and both effectively address the long-term quest for low off-state current. FinFET adoption into manufacturing requires chip makers to integrate complex process technology solutions in the areas of ultra-thin deposition of films, new materials, conformal doping and patterning.

SOI technology has been in production for many years at IBM and its alliance partners. UTB-SOI is an evolution of this technology



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The webinar can be viewed on demand. Please follow the link http://www.synopsys.com/Tools/Manufacturing and select the Webinars tab.

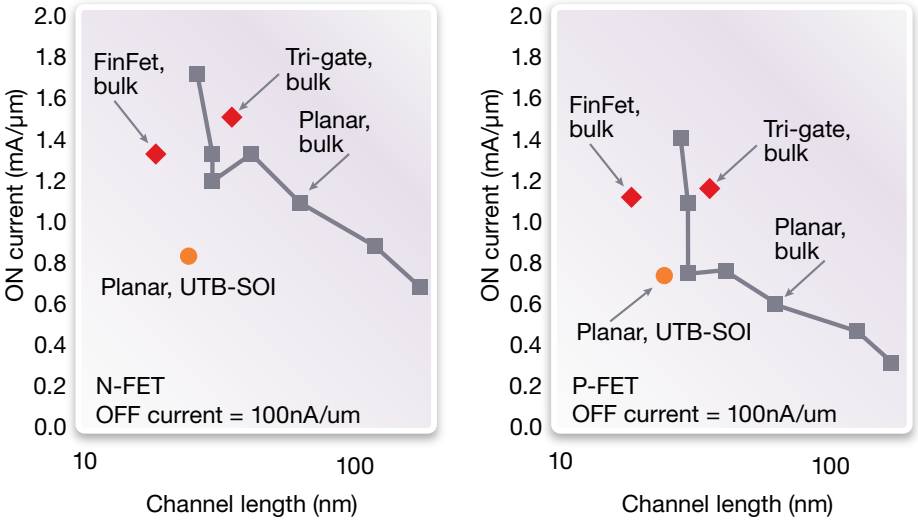


Figure 6: ON-state current for transistors with different architectures based on best research data published in the literature. Transistors with UTB-SOI and FinFET demonstrate the ability to scale down the channel length < 25 nm. FinFET transistor outperforms UTB-SOI so far.

where the silicon body thickness is radically shrunk from 30 nanometers today to a possible 5 nanometers in the future. The UTB-SOI approach continues the planar CMOS architecture with minimal changes to manufacturing flow. A significant challenge, however, is in substrate manufacturability where thickness variation must be in the vanishingly small range of 0.5 nanometers. This is a key reason that the technology is still awaiting adoption into high volume manufacturing.

A key difference between the two designs is in the thickness of thin silicon body. The UTB-SOI requires a silicon body which is two times thinner than that of FinFET, lending FinFET more geometric range to continue scaling. One possible work-around for this issue is that UTB-SOI could employ back gate biasing, where a second gate is built below the buried oxide for greater electrostatic control and reduced off-state current.

The industry debate between FinFET and UTB-SOI approaches boils down to the classic dilemma of choosing revolution or evolution. Both approaches can be excellent strategies. A revolutionary approach requires large-scale investment, with greater risks by radically changing the transistor design and process flow, but it can also yield longer-term yield, performance and extendibility advantages. An evolutionary approach reduces risk, required investment, and time-to-market.

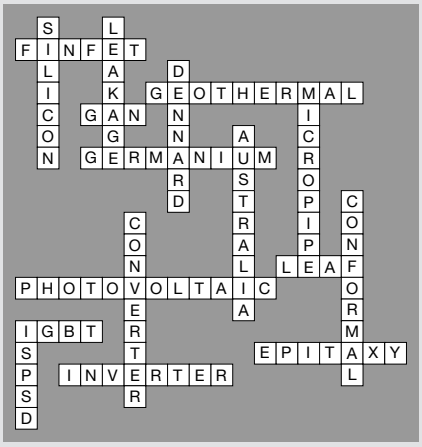
Prof. Hu very aptly summarized the alternative approaches to extending Dennard's scaling for transistors: "Both are real. Both will have a market. For the long-term future, both will be offered, and that is good news, I think. It is exciting to see that there is going to be a choice."

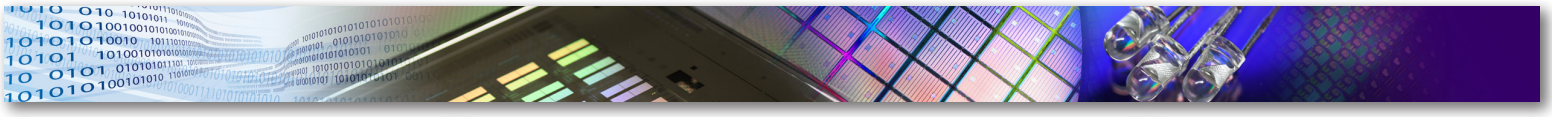
Reference

[1] R. Dennard et al, "Design of Ion-Implanted MOSFETs with Very Small Physical Dimensions," IEEE Journal of Solid-State Circuits, Oct. 1974, pp. 256-268

Crossword Solution

Answer to puzzle on page 10





The Coming Revolution in Power Electronics continued from page 1

photovoltaics, solar thermal and geothermal has achieved an industrial scale in many countries and, though not expected to replace or exceed traditional fossil fuel sources in the near future, continues to drive technological innovations and efficiencies in production and operating costs.

At the heart of many power generation and distribution systems is the power electronics which control and convert power flows in the system. In this article we review the major trends in the evolution of power electronics starting from the system level drivers and ending with the semiconductor technologies for fabricating the power devices.

A Smarter Grid

For over a decade, the need to modernize the power grid has been the subject of much discussion with a general consensus emerging that a new type of grid, eponymously named smart grid, should be developed so as to provide the following benefits and functionality [1]:

- The more cost effective delivery of electricity, including better ways to utilize off-peak electricity production capacity
- Tools to enable consumers to make informed, sometimes real-time, decisions on their usage and purchase of electricity
- The easier incorporation of renewable sources of energy, with consideration to the temporal and variable production capacity characteristic of most such sources
- Improved reliability
- Support for the future growth in plug-in hybrid and electric vehicles

New technologies such as automated sensors and controllers will enable the adjustment of voltage levels to better match real time demand, thereby improving the utilization of generation capacity. These and other enabling technologies are gradually being subjected to the auspices of regulatory bodies who are developing the needed technical standards and protocols.

While the envisioned smart grid will require many years of engineering effort, backed up by private and public funding, the grid modernization process has already begun, notably in the U.S., the European Union, China, Japan, Korea and Australia.

Vehicle Electrification

In 2009, the U.S. accounted for 21.7% of worldwide oil consumption, with most of this oil used for transportation [2]. Around the world, oil is the primarily transportation fuel and a significant contributor to GHG emissions. In view of this, the internal combustion engine, whose initial concept dates back to the middle of the 19th century, is gradually giving way to hybrid electric and eventually fully electric propulsion systems. This trend toward vehicle electrification, when combined with the rising utilization of renewables in electricity production, promises to reduce the consumption of fossil fuels with the attendant benefit of reducing GHG emissions. A Carnegie Mellon study estimates that plug-in hybrid vehicles (PHEV) reduce GHG emissions by 32% relative to conventional IBC vehicles [3]. Full electric vehicles (EV) reduce emissions even further with a recent market entrant, the Nissan Leaf, having won the 2011 World Car of the Year award.

The adoption of PHEV and EV still faces the challenge of consumer behavioral choices, and further improvements in cost, range and duration of charging are seen as key market adoption accelerators. The link between vehicle electrification adoption and smart grid deployment is yet another important factor as it allows for novel concepts such as bidirectional power flow in PHEV and EV. In this scheme, the PHEV and EV vehicle batteries are used as grid storage devices while the vehicles are plugged to the grid, providing an additional monetary incentive to vehicle owners. From the technology point of view, higher efficiency, lighter and cheaper batteries and, closer to the theme of this article, higher efficiency and reduced form factor power converters and inverters, are the focus of much research and development around the world.

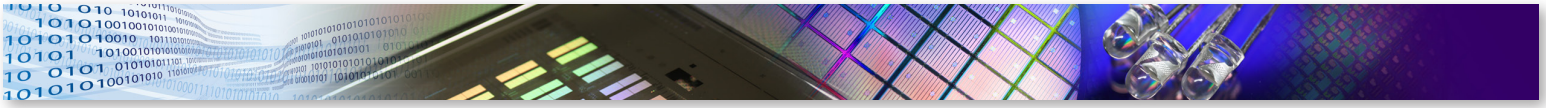
Power Conversion and Inversion

Power converters (DC-DC) and inverters (DC-AC, AC-DC) are fundamental building blocks in power electronics. Well known examples are the devices which transform the wall plug 220V or 110V AC down to the small DC voltages used in portable electronics. In PHEV and EV, the battery bank voltage (typically ~ 300V) must be first converted into a higher voltage (~ 650V) and then inverted into AC to drive the generator in the motor, while other inverters control the charging process [4].

Greater efficiency in the power conversion or inversion process minimizes system losses, and often has a primary impact in the overall system efficiency. Improvements in power converter and inverter efficiency benefit not only PHEV and EV but also a host of other applications such as photovoltaic systems, wind turbines, electric motors, grid transformers and controllers, etc.

Silicon Power Device Technologies

Within the power converters and inverters we find the semiconductor power devices (transistors, diodes, thyristors) which provide the power switching function. Silicon is the mainstay semiconductor used for producing power devices. In its various incarnations, insulated-gate bipolar transistors (IGBT), power MOSFETs, and other silicon power devices account for the majority of the current (2011) $17B a year power device market. The reasons for the prevalence of silicon in power device technologies are no different than in logic or memory: an inexpensive substrate, relative low cost manufacturing process, an excellent insulator (silicon dioxide) and continuously evolving



device structures combine to provide superior overall performance and cost. Indeed, both the IGBT and power MOSFET have experienced a stream of innovations which have helped make them the ubiquitous devices they are today, from the power circuits in laptop computer chargers to the drive system in the Japanese Shinkansen bullet train, and progress is expected to continue (see accompanying article in this issue by Akio Nakagawa)

Given such pervasive usage and the possibility of further improvements in performance and cost, silicon power devices still have a long life ahead of them. Yet, for certain applications where performance is a major driving force, wide bandgap semiconductors (WBG) are beginning to make an impact, and are projected to carve out an increasingly larger portion of the power device market. At a fundamental level, performance in power devices is inextricably linked to the device's blocking voltage when the device is off, and its resistance when the device is on (on-resistance). In particular, the on-resistance plays a major role in determining the switching losses in the device and therefore the overall efficiency of the power circuit where the power device is used.

Further improvements in the voltage blocking and on-resistance capabilities of silicon power devices are intrinsically limited by the material properties of silicon. The silicon energy gap of 1.1 eV (at room temperature) restricts the magnitude of the electric field at which devices breakdown (known as the critical electric field) to about 0.3 MV/cm.

Made for Power: The Superior Material Attributes of WBG Semiconductors

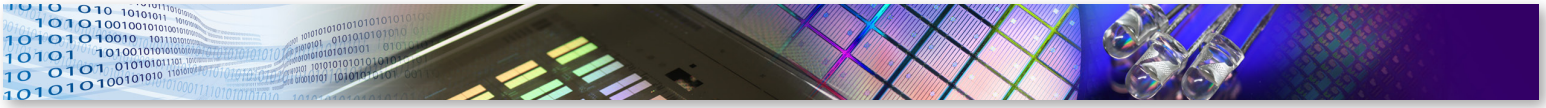
In contrast to silicon, both silicon carbide (SiC) and gallium nitride (GaN), the two principal WBG semiconductors in usage today, are able to support critical electric fields that are about 10 times higher. This means that WBG devices can be made with reduced layout area and thinner layers than silicon devices, enabling a reduction in chip area. The smaller device dimensions resulting from the higher critical electric field also leads to a reduction of the on resistance since conducting regions of the device can be made less resistive (the ρ in the well-known $R = \rho L / A$ equation) and shorter (the L in the same equation). The reduced switching losses resulting from the lower device on-resistance affords the operation of power switching circuits at higher frequency, leading to smaller passive elements like capacitors and inductors. Moreover, WBG devices, owing to their high energy gap (~ 3.3 eV) can be operated at higher temperatures than silicon, with potential additional cost and weight savings from smaller heat sinks.

With such a resume of material advantages, one might indeed wonder why SiC and GaN have not taken over the power device market. The reasons are both financial and technological.

SiC's entry into the power device market occurred over a decade ago with the commercialization of SiC diodes to be used in conjunction with silicon power transistors. This relatively long history has given SiC the opportunity to refine its manufacturing process and reduce its production costs. Notably among these factors is the progress made in the production of SiC substrates. The first commercial SiC devices were produced on wafers 44mm in diameter, often containing large numbers of yield-limiting defects called micropipes. Currently, 150mm diameter wafers are available, the micropipe defect density is no longer a major yield concern, and market forces have gradually lowered wafer prices. SiC transistor technology has also made major strides over the last few years with devices from a number of vendors now available on the market.

GaN's established history in the semiconductor industry is not in power devices but in opto-electronics. At the heart of today's blue light-emitting diodes is a sandwich of GaN and its close relatives indium gallium nitride (InGaN) and aluminum gallium nitride (AlGaN). Even before gaining its current awareness as a material for power switching applications, GaN took a detour as a candidate for radio-frequency power transistors. Much of this circuitous development path is attributable to a fundamental limitation of GaN: the lack of a native substrate. The manufacturing process used to produce silicon substrates (crystal growth from a melt) and SiC substrates (sublimation) do not work for GaN. The only currently viable process for producing GaN substrates is to actually grow it using a more expensive and slower process known as vapor phase epitaxy. This means that for most applications, particularly where cost is major consideration, the GaN device layers must be grown on a foreign substrate, with the available choices being SiC, sapphire and silicon. GaN-on-SiC and GaN-on-sapphire prevailed in the early phases of GaN research and are the workhorses of blue LED production. More recently, GaN-on-Si has emerged as a true contender as the platform of choice for power device applications as if offers the clearest path toward a cost effective production technology. To make GaN-on-Si viable, a number of very challenging obstacles had to addressed, among them the management of the stresses in the GaN/Si layers arising from combining two crystals with different lattice constants and various types of defects present in the GaN which limit performance and reliability. To some extent, these challenges are not been completely surpassed and further validation of the reliability of GaN devices is required before we will see their insertion into high volume commercial applications.

With SiC and GaN poised to growth their footprint in the power device market, competition in overlap applications is heating



up. A traditional way to segment the power device market is by voltage range. Currently, about two thirds of the power electronics market in the 0-900V range. The types of devices that GaN-on-Si supports, a planar structure known as a high electron mobility transistor (HEMT) is well suited for this 'lower' voltage range. At higher voltages, comprising the remaining one third of the power devices market, it becomes challenging to design planar HEMT devices and SiC, with its ability to support vertical device structures, offers some key advantages. Nevertheless, the lines of demarcation are not established and much innovative device engineering in combination with further cost erosion remains.

Conclusion

Power electronics is as active as ever, with a blend of novel device structures and materials aiming to fulfill the promise of emerging application areas in smart grid, vehicle electrification, and energy production from renewables. The power devices community, a critical link in the value chain of power electronics, continues to innovate by optimizing the design of traditional silicon-based devices and by exploring and deploying new devices based on wide bandgap materials such as silicon carbide and gallium nitride.

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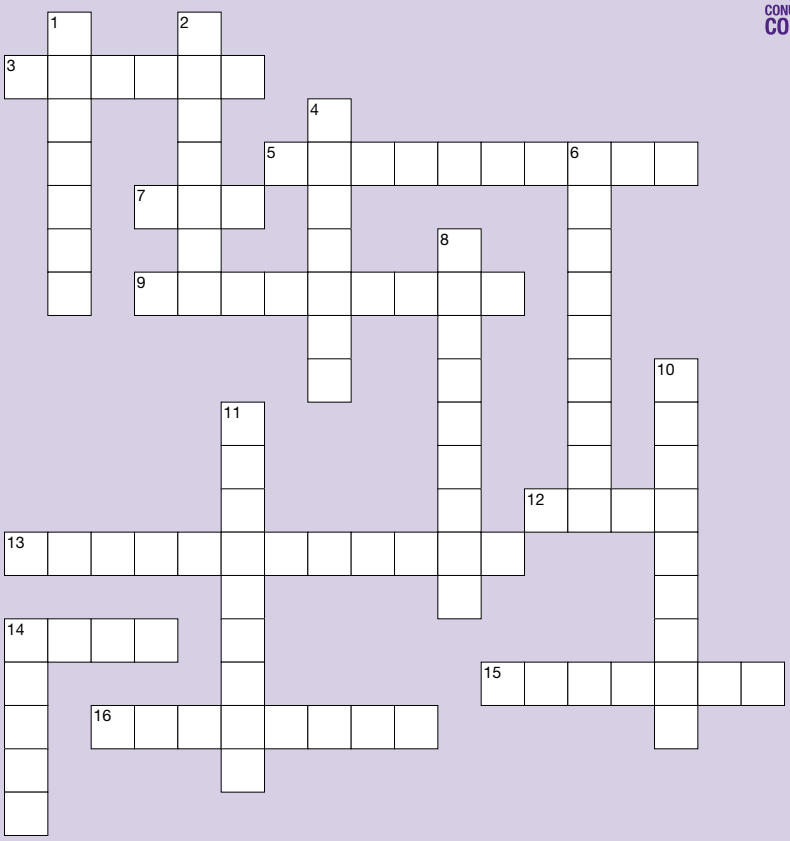
Conundrum Corner

CONUNDRUM CORNER



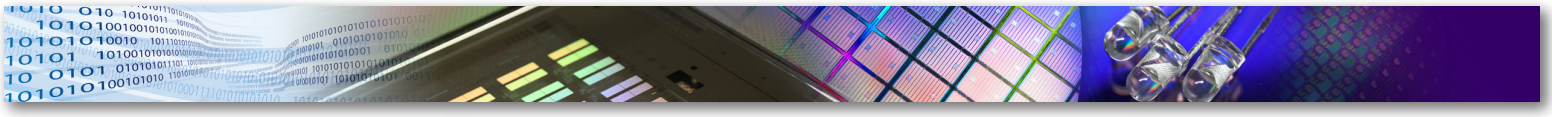
ACROSS

3 New transistor architecture where the channel is surrounded by a gate on three sides
5 Renewable energy source which does not rely on photons
7 Acronym for emerging semiconductor used to fabricate power devices
9 Chemical element used to form a compound with silicon to add stress in FinFET devices
12 2011 World Car of the Year
13 Renewable energy source which relies on photons
14 Acronym for a popular type of silicon power device used in the Shinkansen
15 Process technique which grows a new semiconductor crystal on an existing crystal
16 Power circuit which transforms a DC voltage into an AC voltage

DOWN

1 Common substrate material for fabricating GaN-based power devices
2 Transistor output limiting further scaling of planar device architectures
4 Name of the researcher who first outlined scaling rules for silicon MOSFETs
6 Type of defect which in the past was common in SiC substrates
8 Country south of the equator whereSmart Grid has seen initial deployments
10 Generic designation for process techniques designed to dope the exposed fin sidewalls in FinFET processing
11 Power circuithich transforms a DC voltage into another DC voltage
14 Acronym for an annual conference concerned with power device technologies

See page 7 for solution



1200V IGBT On-Resistance Reduced to SiC MOSFET Level

Akio Nakagawa, Technical Consultant, Nakagawa Consulting Office, LLC.

IGBTs have become one of the indispensable power devices in the field of power electronics, ranging from consumer appliances, industry motors, bullet trains “Shinkansen” and hybrid/electric vehicles. Figure 1 shows the application field of major power devices.

The invention of non-latch-up IGBT [1] in 1984 established today’s IGBT design and its design principle became the global standard. In 1993, the concept of “Injection Enhancement [2]” was proposed, and expanded the voltage capability of IGBTs from 2kV to more than 3.3kV. 3.3kV and 4.5kV. IGBTs are now widely used for the “Shinkansen.” Recently, thin wafer technology [3,4] was introduced to further improve IGBT characteristics. The IGBT silicon thickness has been reduced to 60um for 600V devices and 120um for 1200V devices. The packaging technology has also been improved especially for hybrid/electric vehicle HEV applications. The technology of double sided cooling of IGBT chips has been developed [5] and introduced for the Toyota Lexus Hybrid. The power handling capability of the IGBT chip was increased by 60% by adopting double sided cooling. This reduced the size of the power control unit for HEV by 60%.

The theoretical limit of IGBT was predicted in 2006 [6] and is shown in Figure 2. The on-resistance of IGBT is expected to be still improved in future, and will compete with that of silicon carbide devices and may even supersede it for applications above the 2kV range. The mesa width or the trench to trench distance is required to be reduced to less than 0.1um to approach the IGBT limit. It is considered to be difficult to realize the

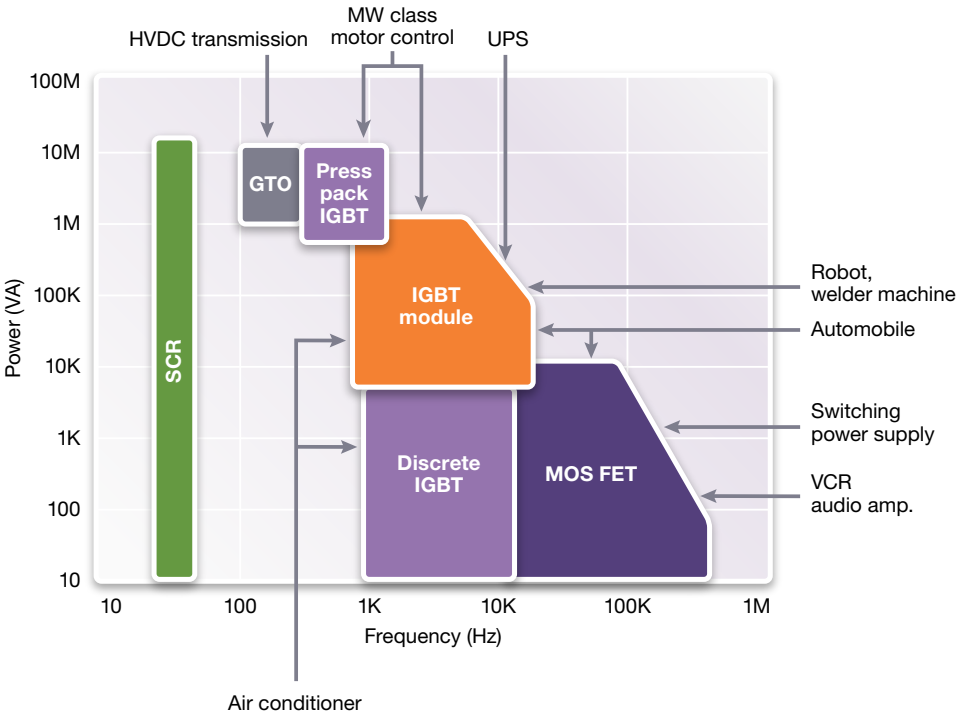


Figure 1: Application fields for power devices

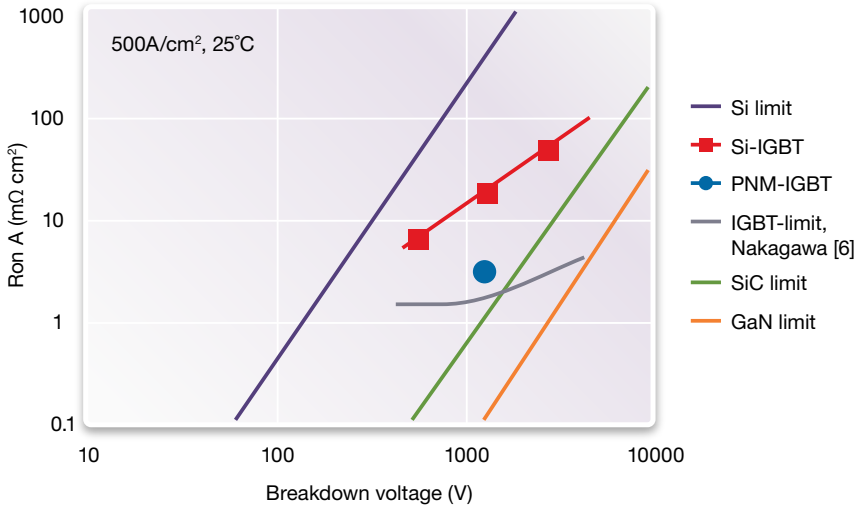


Figure 2: Specific on-resistance vs. breakdown voltage. Partially Narrow Mesa IGBT (PNM-IGBT) have achieved 3.3mΩcm² on-resistance, which is very close to the theoretical limit of IGBT, predicted by A. Nakagawa in Ref. [6]

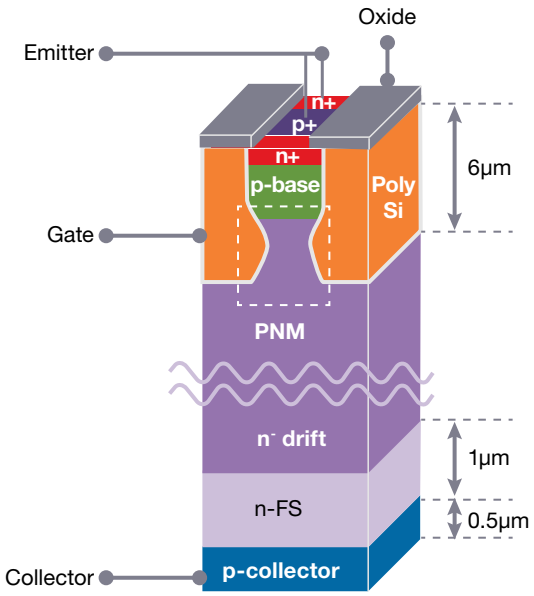


Figure 3: Schematic illustration of Partially Narrow Mesa IGBT

silicon limit IGBT because of the extremely narrow mesa. Thus far, only one IGBT structure called "Dielectric Barrier IGBT [7]" has been proposed to solve the problem. At the recent 2012 International Symposium on Power Semiconductor Devices and ICs (ISPSD), a promising technology "Partially Narrow Mesa IGBT" was proposed by M. Sumitomo et. al. from Denso Corp. and experimentally demonstrated [8]. The unique trench gate structure makes it possible to realize a very narrow mesa region inside the silicon wafer, and provides a practical wide metal contact in the surface. They achieved the on-resistance of 3.3mΩcm^2, which is very close to the silicon limit of 1200V IGBT. This will contribute to further reduce the size and cost of the power electronics system, especially, the power control unit installed inside the HEV.

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Akio Nakagawa, Technical Consultant for Nakagawa Consulting Office, LLC, was born in Atsugi City, Japan, on September 25, 1949. He received the B.Sc. and M.Sc. degrees in physics in 1972 and 1974, respectively, and the Ph.D. degree in electrical engineering in 1984, all from Tokyo University, Tokyo, Japan.

He joined Toshiba R&D center in 1974, where he developed non-latch-up IGBT, 500V SOI 1 chip Inverter ICs, Adaptive Resurf technology for BCD power ICs and other various power devices and ICs. He received Okochi memorial technology prize in 1990 and Toshiba president award in 1997, IEEE Newell Power Electronics Award in 2011, all for the development of non-latch-up IGBTs, and ISPSD Award in 1998, SEMI Leadership Award in 2000.

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