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# Wafer FOCUS

## The Spotlight is on the Photomask

*Anjaneya Thakar, Product Marketing Manager, Synopsys, Inc.*

The semiconductor business is powered by challenging and expensive IC design and manufacturing processes. In this complexity, it is easy to overlook the fact that each design, before it appears on silicon, must squeeze its way in the form of beams of light through slits in plates of glass—the photomask. Photomask manufacturing, while being complex and expensive in its own way, never threatened to slow down the IC manufacturing process. But as we arrive at the threshold of

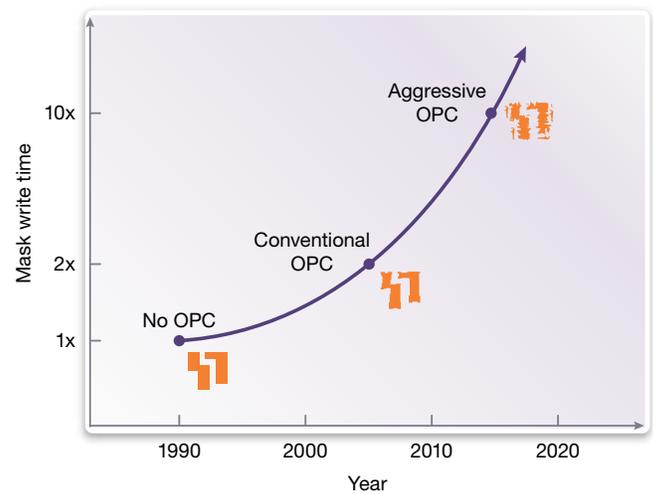


Figure 1: Mask write time increase with aggressive OPC

*Continued on page 2*

*Welcome to the Fall 2011 issue of the Wafer Focus magazine. The feedback from the readers indicates you enjoy this magazine and this provides us the motivation to present topics of interest to the semiconductor manufacturers' community. We look forward to your input and participation in these discussions.*

**Dr. Howard Ko**  
Sr. VP/GM Silicon Engineering Group, Synopsys



## Mask Manufacturing Challenges Cast a Shadow on Semiconductor Technology Scaling

*Naoya Hayashi, Research Fellow, Electronic Device Operations, Dai Nippon Printing Co. Ltd.*



Widespread proliferation of electronic products in business, education and entertainment has made us heavily dependent on semiconductor devices—and

this dependence is expected to get heavier in the future. Advances in semiconductor manufacturing are one reason we have ready supply of affordable solutions and are able to rapidly integrate these devices in our everyday life. These advances took

us from the early g-Line and i-Line steppers to the ArF 193(i) immersion steppers in use today. As we get to the sub-20nm technology nodes, the demands placed on 193i steppers are getting challenging and next

*Continued on page 2*

# Mask Manufacturing Challenges Cast a Shadow



## The Spotlight is on the Photomask continued from page 1

sub-20nm technology nodes, the question “Is the photomask manufacturable?” seems to routinely occupy the minds of IC manufacturers. At the recent SPIE Photomask conference in sunny and scenic Monterey, California, conference attendees spent most of their time locked up in a dimly lit auditorium listening to the growing concern about mask manufacturability and potential solutions. Increasing the use of aggressive techniques to enhance process windows during IC fabrication has led to the mask data patterns becoming highly complex. Since there is no question of

relaxing mask quality, this increase in mask pattern complexity has resulted in increased mask write times (Figure 1) and, eventually, mask cost.

Most vendors of advanced mask lithography equipment are hard at work to determine a practical and timely solution to the problems arising from increasing mask complexity. These solutions include evolutionary techniques which maintain most of the existing manufacturing flow and are, therefore, potentially easy to deploy to revolutionary technologies which hold significant promise.

As in the past, developing a solution to this problem will need collective enterprise from equipment vendors, EDA companies, and semiconductor companies. The good news is that this is already happening.

In this issue of Wafer Focus, we bring you views from a leading merchant maskshop, leaders in the mask lithography tools, and from a unique start-up pursuing new technology. I hope you find these articles informative and I look forward to your feedback.

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## Mask Manufacturing Challenges continued from page 1

generation lithography (NGL) technologies, such as EUVL, NIL, and ML2, are not yet ready to share the burden.

The ITRS roadmap (Figure 1) predicts device scaling to continue its aggressive downward

trend with 14nm devices reaching high volume manufacturing by 2014.

In the absence of NGL tools, this means very aggressive use of computational lithography techniques and the continued use of 193i

lithography for volume manufacturing. In turn, this leads to increasing complexity of mask patterns as source-mask optimization (SMO), inverse lithography techniques (ILT), and multiple-patterning techniques (DPT, TPT, QPT, etc.) are employed to an increasing number of designs in order to maintain acceptable process windows (Figure 2). According to some estimates, this will lead to an order of magnitude increase in mask write times, which is reaching “days”. This is the latest challenge facing the photomask industry upon which the semiconductor industry relies.

The issues facing the photomask industry deriving from aggressive computational lithography are:

- ▶ Insufficient fidelity of mask patterns
- ▶ Long mask write times
- ▶ Lower mask manufacturing throughput and higher mask cost
- ▶ Reduced capability for efficient inspection and repair of masks

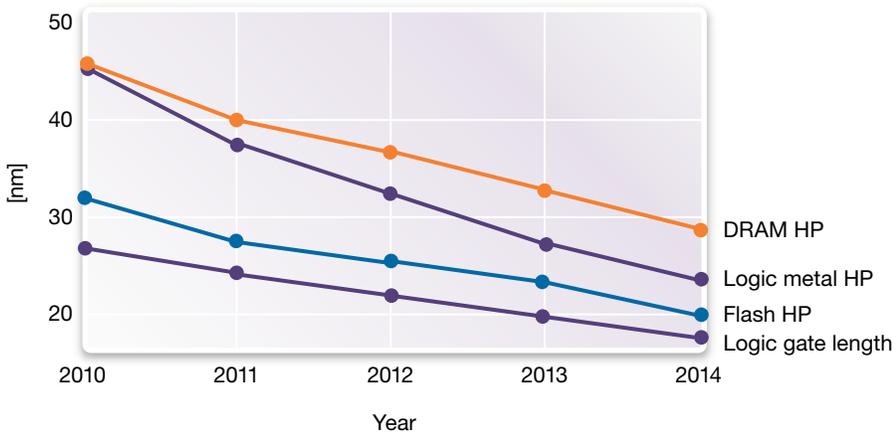


Figure 1: ITRS Roadmap 2010



## What's New

### TCAD

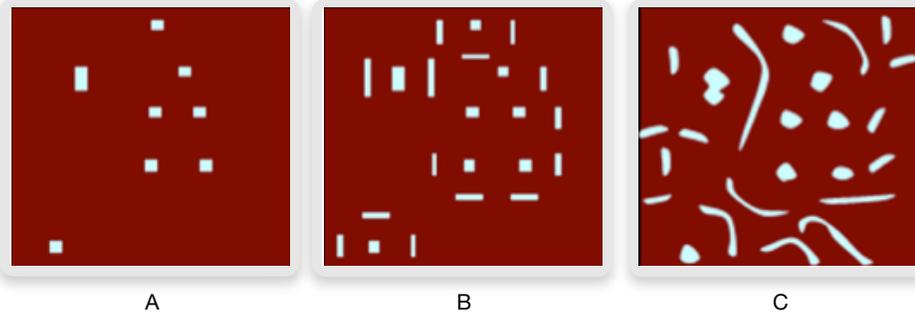
In September, we released TCAD Sentaurus 2011.09, delivering a broad range of new capabilities for FinFET, memory and power device development, and a new, very efficient method for variability analysis. The 2011.09 release is presented in a webinar available for download under the Webinars tab on the Synopsys TCAD website: <http://www.synopsys.com/Tools/TCAD>. Other recent webinars address front-end and back-end reliability modeling and variability analysis in highly scaled devices.

### Yield Management

The upcoming releases of Yield Management products offer significant new areas of value to our customers in product engineering as well as in the fab:

- ▶ Yield Explorer F-2011.12 enables a fully integrated volume diagnostics flow with Synopsys TetraMAX ATPG. The flow is powered by unified single interfaces to standard data formats like LEF DEF as well as STDF, and by a push-button Automated Volume Diagnostics application.
- ▶ Odyssey F-2011.12 provides the means to focus the fab's process control efforts on specific marginal locations within each design. The SmartFlags capability in Odyssey will filter through defect inspection results to identify any defects occurring on known marginal locations, and enable automated response actions for the high value defects captured on wafers in progress.

*Continued on page 5*



**Figure 2: A = No OPC, B = Traditional OPC, C = Aggressive OPC**

Some of these issues are further exacerbated by additional mask manufacturing steps such as: process biasing, mask process correction, and linearization (or Manhattanization) of post-OPC curvilinear shapes. Clearly the lithography process is headed for crisis if these challenges are not addressed quickly and effectively. This will require equipment vendors and EDA vendors to work closely with maskshops (captive and merchant maskshops) and also with the mask users in determining creative solutions that might require a shift in mask manufacturing flow to ensure that integrated circuit manufacturing does not hit a speed-bump. For example, EDA tools and mask writers must expand their capabilities to support overlapped shots, dose modulation per shot, and complex curvilinear patterns.

The good news is that this concern about increasing mask write times is getting due attention from all the relevant parties and there are solutions under consideration to address it. Intelligent biasing maintains post-OPC jog alignment and ensures that shot count does not increase in the mask data prep stage. Several approaches have been presented where e-beam simulation is used to ensure that mask data, optimized for reduced shot count, produces the required features on mask within an

acceptable margin of error. In addition, there is significant development from the mask lithography equipment makers to reduce mask write times. They are working diligently on increasing beam current per shot, reducing settling time per shot, enabling overlapped shots during exposure and, in the future, using multiple e-beams to write one mask — all of which help in reducing mask write times.

Mask manufacturers must work closely with the equipment makers and EDA vendors, and with the mask users in the development and recognition of these solutions. To get the full benefit of the proposed solution, and to ensure that mask manufacturing does not slow down the technology migration of semiconductor devices, we must be open to re-evaluating the overall mask manufacturing flow and making changes as needed. For example, there might be need to modify the post-OPC data during mask date prep to optimize for manufacturing requirements. If so, we must work together in building confidence in this process through thorough evaluation, calibration, and production qualification with the customers. This is similar to the process shift we endured when the post-design data was changed in the OPC process to ensure manufacturability of small features in silicon.



# Mask Writer Data Volume—The Path Forward

Russell Cinque, Applications Manager, JEOL USA Inc.



## Introduction

A little over 10 years ago, the market for electron beam mask writers was dominated by one company,

ETEC. The MEBES (Mask Electron Beam Exposure System) sold by ETEC satisfied industry requirements for accuracy and productivity, and one might forgive them a bit of complacency in thinking their market domination should continue well into the future. But, as we now know, their market domination came to an abrupt end.

The problem was data. Because MEBES writers used a raster exposure system, each pixel of design data was moved through the data path, exposing or blanking the beam. From one technology node to the next, the design grid was halved, and the number of pixels increased by a factor of four. Write times increased with the same geometric progression: 1, 4, 16, 64, and so on. Overwhelmed by data, write times grew beyond the mask maker's tolerance.

Fortunately, the mask industry had a viable alternative. VSB mask writers produced by JEOL, Toshiba, and Hitachi used variable shapes and vector placement to fundamentally break the linkage between design grid and write time. Around 2001–2002, the mask industry moved en masse to adopt VSB systems, and the issue of mask write times was resolved.

Now, 10 years after the migration to VSB, the future of electron beam writers is again unsettled. And once again, the problem is the data.

## VSB write time

VSB write time is given by equation (1), where  $N$  is the number of shots,  $d$  is the resist sensitivity,  $j$  is the current density,  $p$  is the number of passes,  $t_s$  is the shot settling time, and  $t_o$  is overhead time—primarily stage movement:

$$T = N \times \left( \frac{d}{j} + p \times t_s \right) + t_o \quad (1)$$

There is no explicit dependence on the design grid. However, VSB systems are not immune to design changes. Consider a simple line-space pattern. As the pitch is halved, the number of features and the shot count double.

Shot counts also increase with data complexity. With EUV delayed, the need to enhance resolution is driving us toward design techniques, such as Inverse Lithography, that cause extreme increases in data complexity, shot counts, and write times. The challenge for mask makers is to allow complete freedom of design, while keeping the mask write time at an acceptable level.

We will examine 3 possible solutions to the write time dilemma. The first and simplest is evolutionary improvement of VSB. The second scenario, Multi-Beam (MB), requires a revolutionary change from the established VSB. Finally, we will discuss a hybrid approach that modifies both the VSB writer and the input data.

## Solution 1

### Evolutionary improvement of VSB

As the number of shots ( $N$ ) increases, stage movement writing overhead becomes negligible, and the equation VSB throughput is simplified:

$$T = N \times \left( \frac{d}{j} + p \times t_s \right) \quad (2)$$

Let us consider the various ways that increasing shot count can be offset by changes to the terms in brackets. We could adopt a resist with lower dose requirements ( $d$ ), but we are constrained by shot noise. When we shorten the dwell time, there are fewer events per shot, and CD variation increases. We can reduce the number of passes ( $p$ ). However, this would increase CD variation due to resist heating and remove the placement benefits of deflection field averaging. When weighing these tradeoffs, the industry has opted not to use dose or the number of passes to reduce write time.

This leaves us with current density ( $j$ ) and settling time ( $t_s$ ). Over the past 10 years, both terms have improved by an order of magnitude, largely offsetting increased shot counts. Looking ahead, however, it is unlikely that tool vendors will be able to maintain this pace. Moreover, plausible improvements to VSB writers will certainly be overwhelmed by the massive data volume required by resolution-driven mask designs.



## Solution 2

### Multi-Beam

MB writing, as proposed by Mapper, IMS, and many others, would provide a breakthrough solution to the problem of mask write time. Assuming the other quality requirements could be met, a multi-beam system would soon dominate the market for mask writers, displacing the conventional VSB.

MB seems to be the obvious path forward. In recent years, the field has become increasingly active, as more companies announce plans to enter the market, and published results look ever more promising. And yet, the market waits for the first successful tool. The challenges of creating and calibrating thousands of beams are not trivial. MB is perhaps like EUV, an inevitable solution. Unfortunately, again like EUV, a solution that is still somewhere in the future.

## Solution 3

### Writer & Data Hybrid

VSB evolution and MB required modification of the mask writer only; data preparation remained unchanged. In the third approach, the hybrid, we modify both the writer and the incoming data. We will briefly discuss three variants of the hybrid approach: L-shots, Multi-Block Printing (MBP), and Model Based Fracture with Dose Assignment (MBDA).

#### L-shots

The addition of a third shaping aperture enables the formation of “L” s. Data preparation is then modified to identify and create rectangular shots that share a common vertex. These can be exposed as L-shots, giving a 2 for 1 reduction in the shot count for each L that is created. However, because JEOL allows figures to overlap, it is possible to achieve greater savings. As shown in Figure 1, pattern overlap allows the number of shots to be reduced from 5 to 2.

*What's New continued from page 3*

## Mask Synthesis

Proteus LRC (lithography rule check) was launched at SPIE Advanced Lithography 2011. Proteus LRC offers the lowest cost of ownership and the highest accuracy with embedded Sentaurus Lithography rigorous simulation. Anthony Krauth, R&D Advanced Mask Development Manager at Micron, cited the reason for their adoption of Proteus LRC was the “robust checking algorithms and predictable models.” A free Proteus LRC webinar is available for more information.

## Mask Data Prep

In spring 2011 the latest release of CATS (2011.03) went out to our customers. In addition to ongoing improvements in areas such as turn-around time, output file-size reduction and DP scalability, this release offers the following new capabilities:

- ▶ Manufacturing Rules Check & Correct (MRCC): in addition to performing dimensional checks for manufacturability (width, space etc.) CATS users can now perform data manipulation, creation and filtering tasks to get higher quality masks.
- ▶ Support for PROVE, the next-generation registration metrology tool from Carl Zeiss SMS GmbH, for in-die metrology solutions for the 32-nanometer (nm) technology node and below.

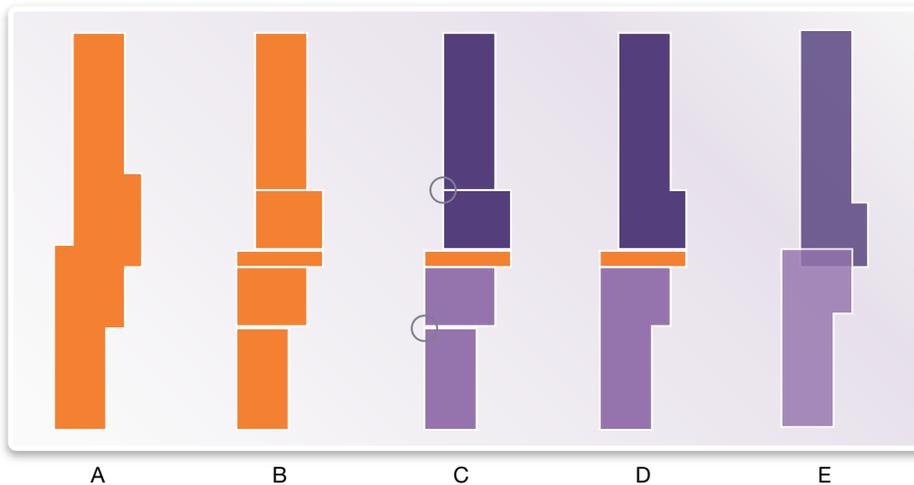


Figure 1: A = Desired shape, B = Conventional fracture, C = Identify optimal Ls, D = Non-overlap Ls, and E = Overlap Ls



## Multi-Block Printing (MBP)

The standard VSB aperture is modified to include multiple shapes or blocks. In this system, a group of figures can be exposed with a single shot cycle, greatly increasing the efficiency of the writer. The design of the aperture would, of course, be optimized for the customer. For example, if a customer's patterns contained a large number of off-angled lines, the aperture would be designed to expose arbitrary off-angle lines with the same efficiency and fidelity as a Manhattan geometry. In the case of MBP, data preparation would be modified to designate which element of the aperture is used to optimize exposure.

## Model Based Fracture with Dose Assignment (MBDA)

In standard data prep, rectangular figures are used to faithfully replicate a target geometry—without overlap and without gaps. When the target geometry is complex, the result is a very high number of small shots. In model based fracture, one makes use of the fact that the mask process (bake, develop, and etch) will smooth the latent image. If the mask process is understood, the desired target geometry can be produced from pattern data, composed of relatively large shots, that only roughly approximates the original outline. A schematic of this technique is shown in Figure 3.

Because there are several degrees of freedom, this approach is powerful and has generated a great deal of interest in the mask industry. The JEOL platform is particularly well suited to model based fracture. JEOL writers properly account for pattern overlap, and the JEOL data format has, for many years, allowed individual dose assignment for each figure.

## Conclusion

The complexity of mask data is pushing write times beyond acceptable limits. Evolutionary improvements to VSB throughput are insufficient to keep pace, and the ultimate solution, Multi-Beam, is not yet available. For today, the best approach to offset increasing data complexity is a writer-data hybrid.

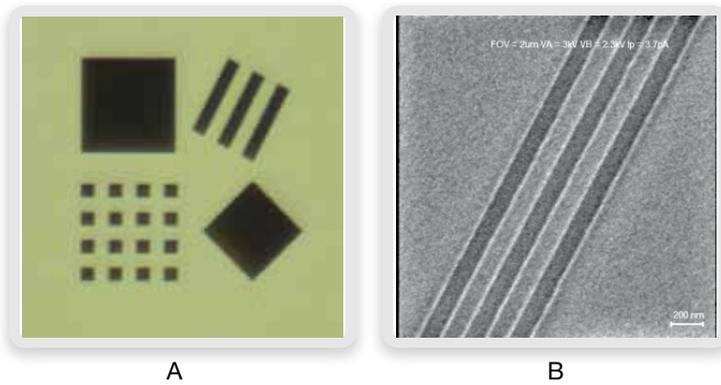


Figure 2: A = Multi-Block Printing test aperture, B = Resist image off-angle lines

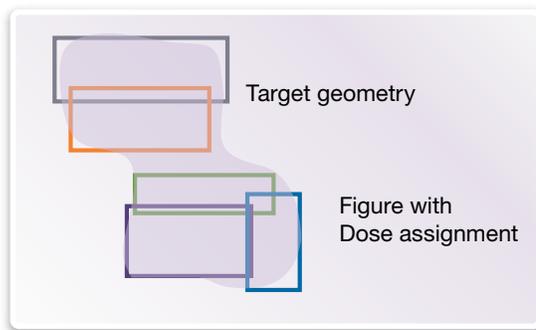


Figure 3: Model Based Fracture with Dose Assignment



# A Study of Factors Influencing Mask Write Times on E-Beam Writers

Shuichi Tamamushi, Technology Executive, Mask Lithography Division NuFlare Technology Inc.



## Introduction

The pace of geometry scaling (shrinkage) of semiconductor devices has been about 2x every 2 years and it is expected

that the same, or even higher, pace will continue for the foreseeable future.

While various alternative NGL (Next Generation Lithography) technologies are being fervently studied, practical viability of any of them in the near future is still questionable with a host of technical barriers to be overcome. Therefore, ArF Immersion lithography with high NA (Numerical Aperture) optical systems is the most likely technology to be used for lithography of subsequent generations of process nodes. This means OPC (Optical Proximity Correction) will continue to be one of the key techniques for achieving acceptable manufacturing yields on future process technologies.

There is a clear trend that mask pattern complexity has increased due to the use of aggressive OPC at increased due to the use of aggressive OPC at advanced process technology nodes. In fact, the increase in shot count for mask lithography is higher than the increase in the number of transistors. If this trend continues, the ratio between shot count and the number of transistors will expand significantly and essentially jeopardize the mask manufacturing process itself. Thus the discussion here is made on the reasonable assumption that the ratio between shot count and the number of transistors is

maintained constant as process technology transitions to smaller geometries.

Our study on throughput issue below is based on the above assumption that the shot count increase is in proportion to the increase of the number of transistors, i.e. 2x every generation.

At present, E-Beam writers with VSB (Variable Shaped Beam) technology are used for the most advanced mask pattern writing. This is primarily because the VSB machines offer higher accuracy and throughput during mask lithography.

Adopting 50KV acceleration voltage for mask writing offers high resolution because of reduced forward scattering of electrons in resist enabling good CD (critical dimension) controllability. However, this high acceleration voltage is accompanied by proximity effects in several tens of micron range resulting in CD errors, which need to be corrected by controlling dose for each shot. VSB approach, with the capability to control flash time for each shot, is well suited for such correction. This ability to control dose and pattern sizes with high resolution is the main enabling feature of NuFlare's EBM writers.

One issue we have to address is the possibility of deteriorated writing efficiency due to large density variations (large spread of dense and sparse patterns) in a mask pattern. Total writing time is not simply proportional to the shot count. In fact, mask write time has not increased in proportion to shot count increase for last 20 years during which time the shot count has increased almost 1000X. Shot size spread and maximum shot size are the key factors that determine the writing time.

## Simple Model of Mask Writing Time

Even though pattern density, resolution, and accuracy requirements vary (get tighter) from one generation to next, the mask plate size has been maintained to be 6-inch square and it is assumed the writing area will continue to remain the same. The relation between total beam flash time "T", average beam current "I", average dose "D" and writing area "S" is expressed in the following formula, where "Q" is the total charge projected:

$$Q = I * T = D * S$$

Therefore, the total beam flash time "T" is expressed by:

$$T = D * S / I$$

Average beam current "I" is expressed by:

$$I = a * J, \text{ where "a" is average shot area and "J" is the current density.}$$

If writing area "S" is constant:

$$a \propto 1/N \text{ where, "N" is total shot count and therefore,}$$

$$I \propto J/N \text{ and,}$$

$$T \propto D * S * N / J$$

In other words as "N" increases, "T" can be maintained constant by increasing "J".

## Estimation of Data Processing Time on the E-beam Mask Writer

Data processing time is independent from the flash time and therefore overall time required for completing writing a mask is determined by the longer of data processing time or total exposure time (actual writing time). Simplified explanation to cover all the

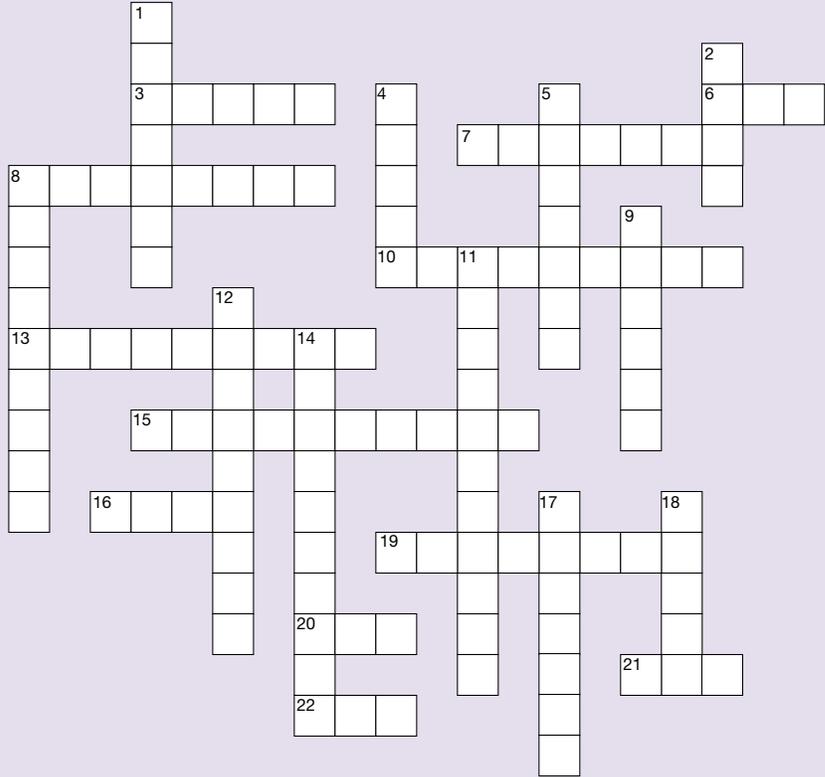


possible cases is difficult, however, writing function of NuFlare's EB Mask writer can be modeled as it uses multiple commercially available CPUs in that the data processing speed is proportional to each CPU speed multiplied by the number of CPUs. Empirical data shows that the relation between data volume given and data processing time is perfectly linear.

## Conclusions

1. While the shot count (number of shapes including OPCs) increase is in the same range as increase in number of transistors per each generation, the same or slightly longer mask write time can be practically realized within controllable range by keeping the total exposure time (the sum of accumulated flash time and settling time) constant by increasing current density. This is a reasonable solution for next generation of process technology.
2. In the event the shot count increases more than 2x in each generation, both total data processing time and actual total exposure time can increase exponentially to eventually become impractical. Even if total exposure time can be reduced by use of such new technology as "multi-beam, multi-column" methodology, data processing time can be a bottleneck unless the data processing speed increases more than 2x each generation. This means the ratio of data processing cost increases each generation.
3. Improving mask writing technology and data processing capacity to keep pace with more than 2X increase in shot count is going to be technically a formidable challenge and economically a very expensive solution. Thus the desirable and practical solution for foreseeable future seems to be to suppress shot count increase by optimizing OPC algorithms.

## Conundrum Corner



### ACROSS

- 3 Annual photomask technology conference in California
- 6 Techniques used to improve printability of features on silicon
- 7 Undesirable small shapes in mask data
- 8 Technique used in data processing to minimize input/output to slow devices
- 10 One of the techniques proposed to reduce mask write time
- 13 An industry standard format for mask data
- 15 Cause of blurring of the image produced by an optical system
- 16 Industry's most widely used mask data prep solution
- 19 Decompose design data for mask writing
- 20 This computational technique uses inverse imaging
- 21 Types of mask writers most commonly used for advanced technology nodes
- 22 Enables lithography to continue down to 15 nm and beyond

### DOWN

- 1 Set of instructions for mask writing
- 2 Amount of energy supplied in one shot during the writing process
- 4 This is a stream of electrons used in writing of photomasks
- 5 Sizing of mask data to compensate for manufacturing effects
- 8 Glass plate reproduction of an IC design
- 9 God of wisdom and moon
- 11 Method of printing a pattern on a substrate
- 12 This technique extends the use of ArF steppers for silicon manufacturing
- 14 Space between die on a wafer
- 17 Chemically removing layers from a surface
- 18 Early format for mask data

See page 11 for solution





# Electron Multi-beam Mask Writer for the 11nm HP node and below

Hans Loeschner (CSO / Technical Marketing), Christof Klein (Director Strategic Programmes), and Elmar Platzgummer (General Manager / CTO) of IMS Nanofabrication AG, Vienna, Austria



The increase in complexity of mask patterns at technology nodes below 20nm is of great concern to the mask manufacturing community. Mask

lithography techniques currently being used are inadequate to meet the economic and quality requirements of future advanced masks. IMS offers a solution which meets this challenge using breakthrough technology. The benefit of a multi-beam mask writing tool is significant reduction in write times while maintaining high mask quality at nodes below 20nm. This article describes IMS' unique technology for mask lithography and describes the benefits in more details with actual data.

## Introduction

The mask writer is of key strategic importance for the semiconductor industry. At present, electron VSB (variable shaped beam) tools are used to write the patterns on resist coated 6" mask blanks. In order to push 193nm immersion and EUV optical lithography to smaller technology nodes, the mask patterns are getting very complex, with RET (resolution enhancement techniques) like OPC (optical proximity correction), ILT (inverse lithography techniques) and SMO (Source – Mask – Optimization) becoming mandatory. Due to increasing pattern density and complexity, the number of shots to be exposed on a mask for VSB is rising exponentially from node to node. So far, the mask writer equipment companies have

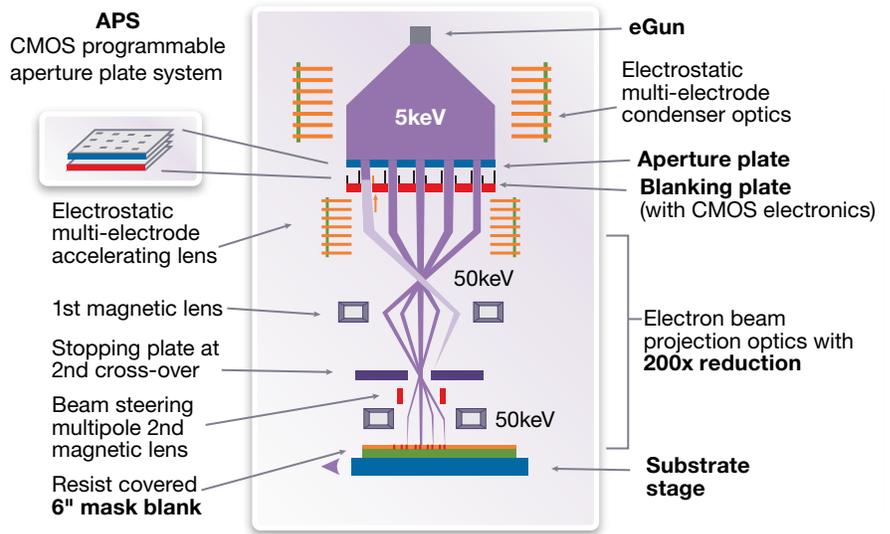


Figure 1: eMET (electron Mask Exposure Tool) principles and realized proof-of-concept tool (eMET POC)

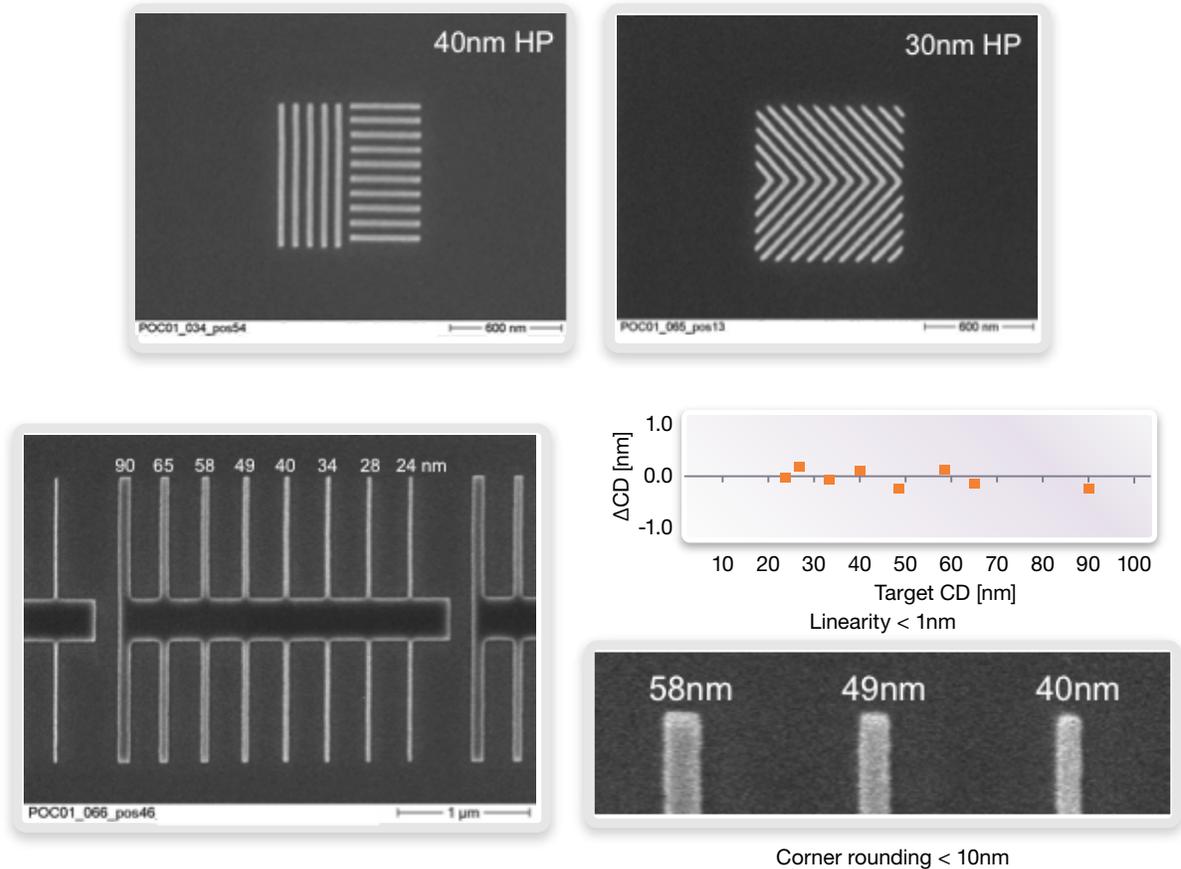


Figure 2: eMET POC exposure results

been successful coping with this complexity by raising the electron beam current density to 400 A/cm<sup>2</sup> while concurrently, significantly increasing deflection speeds. But for  $\leq$  16nm HP technology nodes, there is a brick wall for VSB tools to achieve mask writing times below one day for leading-edge complex masks because...

### 50 keV Electron Multi-beam Maskwriter Development

IMS Nanofabrication AG ("IMS"), a venture capital funded company in Vienna/Austria, developed multi-beam projection techniques to overcome these obstacles. The IMS techniques implement a novel electron-optical column, consisting of an eGun, condenser optics, a blanking device

(aperture plate system) and a projection optics providing 200x reduction. The aperture plate system, operated at low energy (5keV), consists of an "aperture plate" and a "blanking plate" with integrated CMOS electronics, providing 256k ( $k = 1024$ ) programmable beams. The projection optics is a unique combination of an accelerating electrostatic multi-electrode lens and of two magnetic lenses. The beam array field at the substrate is 82 $\mu$ m x 82 $\mu$ m so that the resist covered 6" mask blank can be exposed with constant stage speed in stripes of 82 $\mu$ m width. In 2010 IMS demonstrated redundancy exposure techniques, proving that a reasonable number of "always on" and "always off" beam defects can be tolerated in the blanking device. The electron beam

energy at the substrate is 50keV ensuring very small forward scattering in the resist layer. Figure 1 shows the principles of the multi-beam projection tool, coined "eMET" (electron Mask Exposure Tool), and the proof-of-concept tool realized 2011 (eMET POC).

In order to characterize the novel eMET POC column a stationary stencil plate was used, with 200x reduction providing ca. 780 beams of 20nm beam size at resist coated substrates (150mm Si monitor wafers and 6" mask blanks). With multipole X/Y beam steering 40nm HP and 30nm HP line patterns and iso-lines down to 24nm line width were realized (Figure 2). From detailed evaluations of line width vs dose the column blur was determined within the 82 $\mu$ m x 82 $\mu$ m beam array field. The experimental results were in



	2011–2012	2013–2016	2017–2018	2019–2020
Technology node	Test: 11nm HP (8nm Logic)	11nm HP (8nm Logic)	8nm HP (6nm Logic)	6nm HP (4nm Logic)
50keV electron multibeam tool	POC	Beta and 1 <sup>st</sup> gen HVM	2 <sup>nd</sup> gen HVM	3 <sup>rd</sup> gen HVM
Beam array size	82µm x 82µm	82µm x 82µm	82µm x 82µm	82µm x 82µm
Max. current density	1 A/cm <sup>2</sup>	4 A/cm <sup>2</sup>	4 A/cm <sup>2</sup>	4 A/cm <sup>2</sup>
# beams (1k = 1024)	256k	256k	512k	1024k
Min. beam size	20nm → 10nm	10nm	7nm	5nm
Current (all beams “on”)	1µA	1µA	1µA	1µA
Data path speed to APS	12.8 Gbit/s	≥120 Gbit/s	≥240 Gbit/s	≥480 Gbit/s
Throughput	1-4 cm <sup>2</sup> /h	10h/mask	10h/mask	10h/mask

Figure 3: eMET roadmap

agreement with the 5.3nm (1sigma) blur as predicted by simulations.

In parallel to building up the eMET POC system, blanking plates providing 256k (k=1024) programmable beams were realized by the Fraunhofer Institute for Silicon Technology (ISIT), Germany. Several units are already fully tested at IMS and characterized with 12.8 Gbit/s data path speed. A 256k-APS unit will be inserted to the eMET POC column in Q4/11 for tool acceptance and demos in 2012.

### Electron Multi-beam Maskwriter Roadmap, Extendibility and Productivity

The eMET mask writing time is governed by the speed of blanking plate CMOS electronics and the Data Path capabilities to be enhanced to ≥ 120 Gbit/s for Beta and 1<sup>st</sup> generation HVM tools. This enables a mask write time of < 10 hours, using 10nm beam size and a resist exposure dose of 100µC/cm<sup>2</sup>. The use of such insensitive resist meets the ITRS requirements on low line edge/width roughness (LER/LWR).

An important topic of the eMET Beta and 1<sup>st</sup> generation HVM tool developments

for the 11nm HP mask technology node is the realization of the advanced Data Path. For this essential part of the multi-beam mask writer IMS has started a technical collaboration with Synopsys.

The eMET roadmap is shown in Figure 3. Using the novel column, the eMET technology is multi-generational, within the 82µm x 82µm beam array field doubling the number of beams to 512k for the 8nm HP, and to 1024k for the 6nm HP technology node, and concurrently, by lowering the smallest beam size to 7nm and 5nm, respectively.

For eMET the required electron beam current density at the substrate is as low as 4 A/cm<sup>2</sup> (100-times smaller compared to VSB) which is an important advantage to avoid detrimental resist heating and outgassing. The total beam current is 1µA (with all beams “on”). This current level gives rise to very small global and stochastic Coulomb interactions, not limiting tool performance.

Summarizing, the IMS electron multi-beam technology surpasses the productivity of VSB tools by a factor of 5 to 20, providing < 10 hours mask write time for the 11nm HP (8nm logic), 8nm HP (6nm logic) and 6nm HP (4nm logic) mask technology nodes.

### Crossword Solution

Answer to puzzle on page 8



Please send questions or comments to [waferfocus@synopsys.com](mailto:waferfocus@synopsys.com)

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