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Newsletter for semiconductor process and device engineers

December 2011

TCAD news

Latest Edition

Welcome to the IEDM 2011 edition of the TCAD News. IEDM is always a good forum to reflect on recent developments in the semiconductor industry, and this year there is indeed much to be excited about. We've seen the 22nm node initiating production along with the introduction of 3-D tri-gate devices, which promises further CMOS scaling and represents another inflection point in the semiconductor industry. We've also seen tremendous progress in the development of novel memories and more efficient and capable power devices, fabricated in silicon, SiC, and GaN. TCAD has no doubt played an increasing role in the development of these technologies as R&D becomes more complex and experiments on wafers more costly.

In this edition of TCAD News we present two topics which are highly relevant to advanced logic and memory technologies. With feature sizes down to the sub-20nm range, device variability has become an important requirement for device engineers to analyze and control in order to achieve optimal operation. The first article discusses a recently developed Impedance Field Methodology (IFM) for analyzing the impact of random variability on device performance. This methodology is much more efficient in terms of simulation speed without compromising accuracy. An added benefit of IFM is that it can be extended to the variability analysis of small circuits such as SRAM cells, generating static noise margin statistics to assess device yield. While FinFET is becoming the primary option for the 14nm node, the second article covers the 3-D simulation of FinFET devices, including the analysis of doping and stress proximity effects. Both articles should provide a glimpse of how TCAD can help in evaluating the complex device engineering options while you are listening to the interesting papers at IEDM.

With the approaching holiday season, I would also like to take this opportunity to wish you happy holidays and a prosperous New Year.

With warm regards,

Terry Ma
Vice President of Engineering, TCAD

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Modeling Statistical Variability with the Impedance Field Method

Introduction

As transistor scaling continues, self-averaging of device properties for individual devices becomes less effective and thus the statistical variability of device properties become more prominent. The conventional numerical approach to investigating statistical variability is to run a large number of simulations on randomized realizations of a reference device. A severe shortcoming of this so-called "atomistic" method is the huge numerical expense, caused by the necessity to run many 3-D TCAD simulations.

The impedance field method (IFM) in Sentaurus Device provides a fast, convenient and accurate alternative for statistical variability analysis.

What is the Impedance Field Method?

The basic idea behind the IFM is to treat the randomness as a perturbation of a reference device. Rather than solving the full, nonlinear Poisson and drift-diffusion equations for a large number of random device realizations, we obtain the 3-D TCAD solution only once for the reference device. Then we compute the current fluctuations at the device terminals caused by these random perturbations. This computation is based on linear response theory using a Green function technique [1], [2].

For modeling statistical variability Sentaurus Device supports three different variants of the IFM: The noise-like IFM, the statistical IFM and the deterministic IFM.

To get a better feel for IFM we will now discuss these IFM variants for the example of random doping fluctuations. Note, however, that the IFM can also be applied to geometric fluctuations.

Once we obtain the 3-D TCAD solution for the reference device with the doping profiles $N^s_{\mathrm{ref}}(\vec{\mathrm{r}})$, we compute the deviation of the current at a contact c in linear response to the perturbations:

$$\delta I_{v,c} = \sum_s \int d^3r\, G^s_c(\vec{\mathrm{r}})\ \delta N^s_v(\vec{\mathrm{r}}) \qquad (1)$$

$$\delta N^s_v(\vec{\mathrm{r}}) = N^s_v(\vec{\mathrm{r}}) - N^s_{\mathrm{ref}}(\vec{\mathrm{r}})$$

where $N^s_v(\vec{\mathrm{r}})$ is one particular random doping realization for the doping species s.

The Green function $G^s_c(\vec{\mathrm{r}})$, which is also called the "impedance field", does not depend on the random doping realization. It is computed from the full 3-D TCAD solution of the reference device and therefore the Green function must be computed only once, no matter how many random doping realizations are considered.

In This Edition

Noise-like Impedance Field Method

The IFM has long been known from noise analysis [1] and the noise-like IFM variant discussed here models the random fluctuations in a manner very similar to noise analysis [2]. For random doping fluctuation (RDF), the statistical average of the doping fluctuation vanishes $\langle \delta N_v^s(\vec{r}) \rangle = 0$ and thus, in our linear approximation, the statistical average of the terminal current fluctuation vanishes $\langle \delta I_c \rangle = 0$.

Therefore information about the statistical effects of the RDF on the terminal currents is contained only in higher order statistical moments. The second moment is given by:

$$S_{c_1,\,c_2} = \langle \delta I_{c_1}\, \delta I_{c_2} \rangle \qquad , (2)$$
$$= \sum_s \iint d^3r_1 d^3r_2\, G_{c_1}^s(\vec{r}_1) K^s(\vec{r}_1,\vec{r}_2) G_{c_2}^s(\vec{r}_2)$$

Assuming that the random doping fluctuations are spatially uncorrelated the second-order moment of the random doping fluctuation is given by:

$$K^s(\vec{r}_1,\vec{r}_2) = \langle \delta N^s(\vec{r}_1)\ \delta N^s(\vec{r}_2) \rangle \qquad , (3)$$
$$= N_{\mathrm{ref}}^s(\vec{r}_1)\, \delta(\vec{r}_1 - \vec{r}_2)$$

Note that contributions for different doping species s, such as acceptor and donors, add up, rather than compensate for one another. Also note that there are no adjustable parameters in the second-order moment of the random doping fluctuation. Therefore using this model does not require any calibration. The second moment is directly related to the standard deviation of the terminal current or voltage. For example for a single transistor the standard deviation of the drain d current and the gate g voltage is given by:

$$\sigma(I_d) = \sqrt{S_{d,d}} \qquad , (4)$$
$$\sigma(V_g) = \frac{\sqrt{S_{d,d}}}{y_{d,g}}$$

The standard deviation for the gate voltage fluctuation is obtained by dividing the drain current standard deviation by the small signal transconductance $y_{d,g}$.

The noise-like IFM is fast, easy to use and efficient when it is sufficient to know the random fluctuation induced standard deviation of terminal current and voltages.

Statistical Impedance Field Method

Within the statistical IFM we use Equation (1) directly, and to perform a statistical sampling using a large number of random doping realizations $N_v^s(\vec{r})$. To obtain statistical samples, we assume that doping is spatially uncorrelated, and that the number of dopants in a given volume follows a Poisson distribution, with an average given by the average number of dopants in the volume. With this assumption, based on the average doping concentrations, for each vertex in the device, we pick random numbers for acceptor and donor atoms in the Voronoï volume for the vertex, and convert these numbers back to concentrations by dividing by the Voronoï volume. This approach is equivalent to the approach introduced in Ref. [3]. We then use Equation (1) to compute the small-signal current responses δI_c at each contact c, for a sufficiently large number of random samples. From δI_c we then compute the full IV curves of the randomized devices. IFM approximates the generally non-linear system by a linear, small-signal equivalent one. We find that the accuracy of this inherent approximation can be considerably improved by leveraging all otherwise available information about the system. For example, the IFM gives the user a certain degree of freedom in selecting which linearized quantities to consider. For example, for a MOS transistor one can consider either the random fluctuation induced linear gate voltage response or the linear drain current response of the system, or even a combination of both. For a transistor in saturation the gate voltage only weakly controls the drain current and thus considering the linear drain current response is more appropriate. In the sub-threshold regime, on the other hand, random fluctuation effects are very well described by threshold voltage fluctuations, which are intuitively liked to the linear gate voltage response. This additional information is incorporated into the IV computation algorithm by formulation of a set of boundary conditions specific for the devices and biasing schemes at hand. Table 1 summarizes the steps involved in the statistical IFM.

Step	Task
1	Start from reference device with doping profile $N_{\mathrm{ref}}^s(\vec{r})$
2	Generate randomized doping data field samples: $N_v^s(\vec{r})$; $v=0,1,2,\ldots,\sim 1000\text{-}5000$
3	Compute linear current response of the TCAD solution to the random doping perturbation $\delta I_{v,c}$ from Equation (1)
4	Compute IV characteristics from $\delta I_{v,c}$
5	Compute statistics of all relevant quantities from IV characteristics.

Table 1: Summary of steps in the statistical IFM.

This approach is therefore also applicable when the standard deviations of contact currents are insufficient to characterize the statistical behavior of interest. For example, we can use the statistical IFM to plot individual voltage transfer characteristics (VTC) of an SRAM cell inverter and use them to extract the static noise margin (SNM).

Deterministic Impedance Field Method

For deterministic IFM, we specify the variations directly. For example, for deterministic doping variations we replace in Equation (1) the random doping realization $N_v^s(\vec{r})$ by a user defined actual modified doping profile. Sentaurus Device computes the effect of the variations on the observation terminal voltages and currents. Compared to random fluctuations, deterministic variations

give the user more control over the variation and are easier to understand, because no statistical interpretation is required and no second-order moments appear. This method is particularly useful for screening and corner analysis.

Comparison of noise-like IFM to an "atomistic" approach for single transistors

To better illustrate the advantages of the IFM let us compare this method to another widely used approach for the investigation of variability in single transistors: the so-called "atomistic" approach (see for example [4],[5]). This method relies on 3-D TCAD simulations of a large number (200 up to 100,000 [6]) of independent randomized 3-D realizations of the device structure. The computational resources needed for the "atomistic" approach are directly proportional to the number of randomized device structures in the statistical sample. Such an approach is therefore naturally limited to smaller devices with simplified geometries [4]-[7]. For "atomistic" methods one also has to carefully select transport models which are compatible with the "atomistic" approach and re-calibrate the transport parameters to recover the calibrated reference TCAD results [4],[7].

The IFM method on the other hand is applicable even to large device structures and can also readily handle realistic geometries. The computational resource requirements depend only weakly on the number of randomized devices included in the statistical sample. Further IFM is fully compatible with standard TCAD. Consequently, all well-established TCAD transport models as well as all calibrated transport model parameters can be used directly for IFM.

To illustrate the speed advantage of IFM compared to the "atomistic" approach, which is also fully supported by Sentaurus Device, we compare the simulations results between the "atomistic" method and the noise-like IFM. Figure 1 shows one of the 200 randomized 3-D NMOS structures used for the comparison.

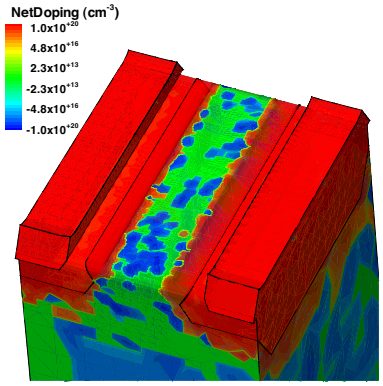

Figure 1: Randomized doping profile for one of 200 3-D NMOS devices used with the "atomized" method. For better viewing only silicon regions are shown.

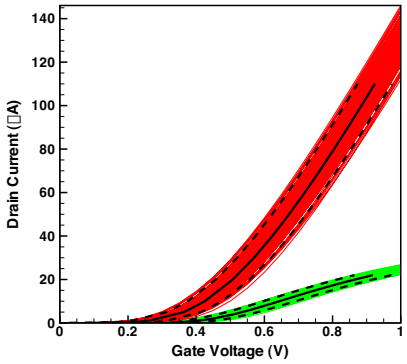

Figure 2: I_dV_g for V_d=50mV (green) and 1V (red) obtained from 200 3-D TCAD simulations of individually randomized realization of the NMOS device. The solid black line shows the average I_dV_g and the dashed line the average I_dV_g $\pm 2\sigma(V_g)$.

Figure 2 shows the resulting 200 I_dV_g curves for V_d=50mV and V_d=1V. From these curves then the standard deviations for quantities such as the threshold voltage V_{th} and the on-state current I_{on} are computed.

Within the noise-like IFM method, a single 3-D TCAD simulation is sufficient to compute the standard deviations of the gate voltage $\sigma(V_g)$ and the drain current $\sigma(I_d)$ as function of the gate bias as shown in Figure 3 and Figure 4.

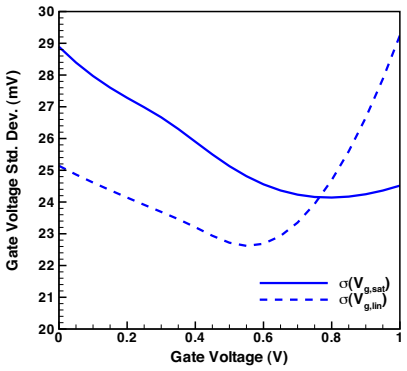

Figure 3: Standard deviation of the gate voltage fluctuations $\sigma(V_g)$ for the 3-D NMOS device as computed with the noise-like IFM.

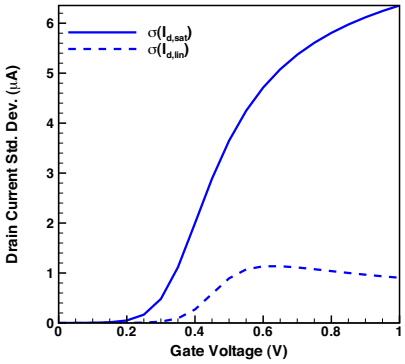

Figure 4: Standard deviation of the drain current fluctuations $\sigma(I_d)$ for the 3D NMOS device as computed with the noise-like IFM.

From these curves we extract threshold voltage standard deviation as $\sigma(V_{th})=\sigma(V_g)|_{V_g=V_{th}}$ and the on-state current standard deviation as $\sigma(I_{on})=\sigma(I_d)|_{V_g=1V}$. Table 2 shows that the accuracy of the standard deviation obtained by the two different approaches is equivalent (See also Ref. [8]). Table 3 gives the single-computer run time using 4 CPUs. The computation of the impedance field during the gate bias sweep doubles the run time for 3-D TCAD simulation of a single device structure. However, this computation has to be done only once. For the "atomistic"

method however a full 3-D TCAD simulation is required for each of the 200 randomized device structures. This results in an overall 100x speed advantage of IFM over the "atomistic" approach. The speed advantage increases even more if a larger sample of randomized device structures is considered.

	"Atomistic"	Noise-like IFM
$\sigma(V_{th})$ (lin)	23.8 mV	23.5 mV
$\sigma(V_{th})$ (sat)	27.5 mV	27.2 mV
$\sigma(I_{on})$	6.63x10^{-6} A	6.33x10^{-6} A

Table 2: Comparison of standard deviations computed with the "atomistic" method and the noise-like IFM.

Method	# of Runs	Total
"Atomistic"	200	400h
IFM	1	4h

Table 3: Run-time comparison between the "atomistic" method and the noise-like IFM. All simulations were performed on Linux PC using 4 threads.

Static noise margins variability of SRAM Cells

It is possible to use the statistical IFM for single transistors and generate IV curves similar to the ones shown in Figure 2. However, using the statistical IFM for the computation of quantities like the standard deviations of the threshold voltage or the on-state current of a single transistor does not result in any advantages over the noise-like IFM. Further, like the "atomistic" approach for the statistical IFM the user has to manage and analyze the large amount of IV data that both methods produce.

However, the statistical IFM is fully applicable in application areas which are not suitable for the noise-like IFM. A highly relevant example is the variability of the static noise margin (SNM) of an SRAM cell.

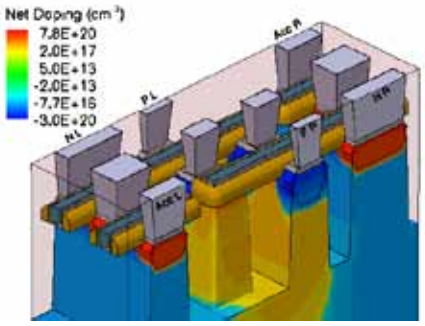

Figure 5: Device structure of the 6T SRAM cell. For better viewing the display of the dielectrics are shown as transparent.

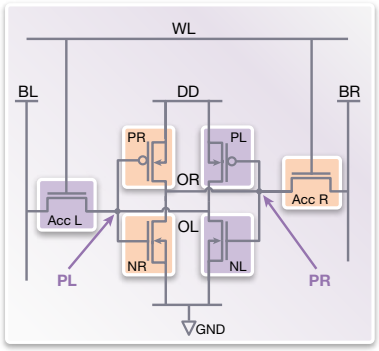

Figure 6: Circuit diagram equivalent to the 3-D TCAD device structure shown in Figure 5. The diagram also shows the node labels and circuit element names for reference. For the measurement of the voltage transfer characteristics (VTC) of the "left" (violet highlights) or the "right" (tan highlights) inverter the probes PL and PR are added to the SRAM circuit. The probes are activated or deactivated as needed.

Figure 5 shows a 6T CMOS SRAM cell which is created by 3-D TCAD using Sentaurus Process [9], and Figure 6 shows the equivalent circuit of the SRAM cell. The 3-D TCAD model which represents the 6 transistors as a single simulation domain contains 1 million grid points. The large run-time for obtaining a single voltage transfer characteristic of about 25h makes the use of "atomistic" approaches prohibitive. The noise-like IFM is not applicable either because there is no direct correlation between the standard deviations of current or voltage fluctuations at the respective "left" and "right" output nodes OL and OR and the standard deviation of the SNM.

The statistical IFM, however, uniquely combines the flexibility of the "atomistic" approach, while fully retaining the speed advantage of the IFM.

Figure 7 shows the "left" and "right" VTC curves for 1000 randomizations of the reference SRAM cell obtained by computing the individual VTC curves from the linear current response at the output terminal of the respective "left" and "right" inverters of the SRAM cell. For each of these 1000 "butterfly" curves the "left" and "right" static noise margins (SNM) are extracted by fitting the largest possible square into the "left" and "right" wings of the butterfly. The "left" and "right" SNM are defined as the length of the sides of the respective square. The effective SNM is defined as the smaller of the two values.

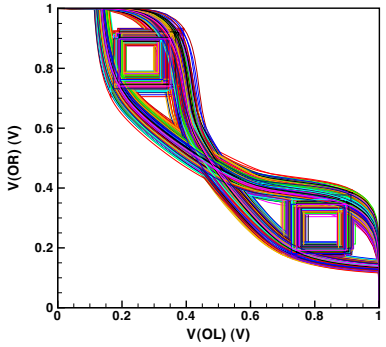

Figure 7: SRAM butterfly curves:"Left" and "right" voltage transfer characteristics (VTC) obtained from simulating 1000 randomizations of the 6T SRAM cell shown in Figure 5 using the statistical IFM. The corresponding "fitted squares" represent the "left" and "right" static noise margin. The data is shown for the "Read" operation.

Figure 8 shows the quantile-quantile (Q-Q) plots for the "left" and "right" SNM as well as the effective SNM as extracted from the data shown in Figure 7. In the Q-Q plot the quantiles of observed SNM distributions are compared to the quantiles of a Gaussian distribution with the same average and standard deviation. The straight Q-Q plot for "left" and "right" SNM distributions shown in Figure 8 are consistent with the assumption

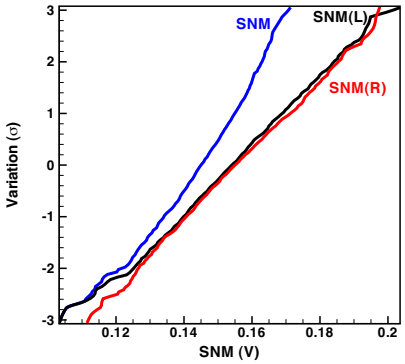

Figure 8: Quantile-quantile plots of the "left" (black), "right" (red) SNM as well as the effective (blue) SNM as extracted from the data shown in Figure 7.

that both quantities follow the same, Gaussian distribution.

The distribution of effective SNM is, however, clearly not consistent with the assumption of a Gaussian distribution. The Q-Q plots of the effective SNM instead show curvature. These findings are consistent with experimental results [10].

Resource Requirements

# of Nodes	~ 1,000,000
RAM used	~ 50 GB
Run Time per VTC	~ 50 h
DC bias sweep time	~ 50% of run time
Impedance Field comp.	~ 46% of run time
$\delta I_{v,c}$ computation time	~ 4% of run time

Table 4: Computational Resource requirements for the 6T CMOS SRAM Cell simulations using the statistical IFM.

To ensure accurate TCAD simulation results the 3-D 6T SRAM cells is represented by a TCAD model containing about 1 million grid nodes. The 3-D TCAD device simulation which computes the statistical IFM response for 1000 randomization during one VTC sweep took less than 50h (including initialization). We used 4 CPUs on a standard large RAM Linux computer.

The peak RAM consumption was about 50GB. The DC bias sweep consumed about 50% of the total runtime. The computation of the Green functions for each bias point consumed about 46% of the total runtime. The computation the linear responses for all of the 1000 individual randomizations accounted for the remaining 4% of the total runtime. This analysis shows that the statistical IFM is particular efficient for large number of randomizations as the incremental runtime for an additional randomization is very small. Also, although the statistical IFM approach applied to a 3-D 6T SRAM cell requires considerable computational resources, these resource requirements can easily be met by a standard modern computer with sufficient RAM. Note also that the entire statistical IFM analysis for a randomization sample size of 1000 (or more) takes roughly the same time than it would take to compute just two DC sweeps for an "atomistic" approach.

Summary

The impedance field method in Sentaurus Device provides a fast, convenient and accurate method for statistical variability analysis. Sentaurus Device supports three variations of the method to optimally fit the specific requirements of the task at hand. For applications for which it is sufficient to consider the standard deviation of the terminal current or voltage response the noise-like IFM provides the easiest to use, as it does involve explicit statistical sampling. The deterministic IFM gives the user perfect control for screening and corner analysis. For more complex device responses the statistical IFM combines the flexibility of the "atomistic" approach, while fully retaining the speed advantage of the IFM.

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Simulation of 6T-FinFET SRAM with Sentaurus TCAD

Introduction

Logic technologies have been successfully developed down to the 32/28nm process node by relying on novel processes to boost performance and mitigate short channel effects. The introduction of stress engineering at the 90nm node and, more recently, high-k dielectrics with metal gates, are notable examples. However, at the 22nm node and beyond, scaling becomes increasingly difficult without fundamental changes to the device architecture, with research and development focusing on three-dimensional (3-D) transistors and thin-body silicon on insulator (SOI). This year's announcement by Intel of a 22nm process node featuring tri-gate transistors [1] marks a significant milestone on the road to replacing the traditional planar MOSFET. In tri-gate transistors, the gate wraps around the channel on three sides, forming a 3-D structure known generically as a FinFET. FinFETs are expected to play a larger role in future technologies, motivating their simulation with TCAD.

Building on extensive research and development spanning several years and releases, Sentaurus TCAD now includes a comprehensive set of 3-D tools to address the rising interest in the industry to design and optimize FinFETs [2]. The most challenging task in 3-D TCAD is meshing and geometry generation. Mesh generation is handled by Sentaurus Mesh, which features advanced algorithms to generate high quality meshes suitable for highly accurate process, device, and backend reliability simulations. MGOALS3D is a geometry generation library that is used in the simulation of process-oriented geometric steps. An alternative way to generate 3-D structures is with Sentaurus Structure Editor, a solid modeler that has the capabilities to create complex structures from geometry primitives. The process simulators, Sentaurus Process and Sentaurus Topography, have consistent models for 1-D/2-D/3-D operation. The device simulator, Sentaurus Device, has the longest history in 3-D simulation, with a full set of 3-D models and widespread utilization since the inception of Sentaurus. In parallel with the 3-D development of mesh generation, structure generation and the core simulators, parallel solvers have been developed and substantially improved over the last several years in order to make 3-D simulation practical. Release F-2011.09 further extends 3-D simulation capabilities with numerous improvements in speed, robustness, as well as new features [3].

Simulation results

The introduction of 3-D FinFET structures into manufacturing requires reliable 3-D TCAD simulation capabilities in order to study, optimize and improve these structures. In this and the subsequent section of the article presents a full 3-D simulation of a 6 transistor FinFET SRAM cell. An overall view of the structure is presented in Figure 1.

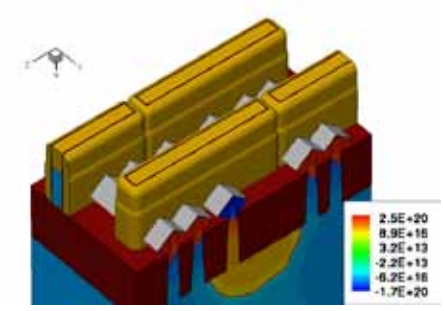

Fig 1: Doping distribution in 6T-FinFET SRAM cell.

The process flow and geometry details are based on recent gate-first 25 nm gate length processes published by leading manufacturers [4,5]. The size of the simulated cell is 260 nm X 487 nm. The layout information is based on scanning electron microscope (SEM) images and features 2 driver P-FinFETs and 4 N-FinFETs (2 used as drivers and 2 access ones). In order to boost the performance of the N-FinFET drivers, each of the transistors consists of two fins connected in parallel (or effectively 2 transistors working together). This is accomplished by merging the source/drain pockets [5]. Connecting the fins in parallel corresponds to increasing the device width in planar CMOS technology. The physical gate length of the high-performance transistors for this technology is 25 nm. The transistors feature epitaxial pockets with process faceting typical of these processes. Stress is applied to the P-FinFETs and N-FinFETs via SiGe pockets and Si:C source/drain areas, respectively. The fin pitch for the N-FinFET is smaller than the one for the P-FinFET in order to merge the source/drain areas during epitaxial growth. Since information about the doping process and conditions for this structure is not available in the literature, we chose implantation and annealing conditions that correspond to a typical device performance for this node. Simulations of such complex structures require a large amount of computing resources. On a state-of-art multi-core machine, the FinFET process simulation takes about 56 hours, while device simulation requires 60 hours to simulate the Id-Vgs characteristics for low and high biases, and the HOLD, and READ butterfly curves.

The geometry was generated with MGOALS3D and includes 40 different operations. Some of the important geometries are presented in Figure 2.

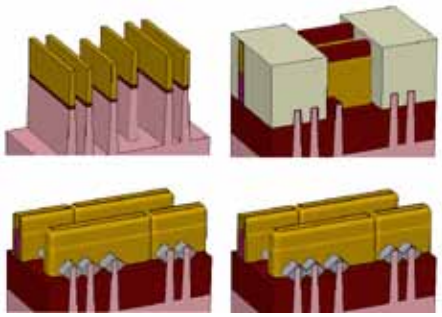

Figure 2: Geometry operations in 6T-SRAM structure: a) fin pattern, b) structure for source/drain extension implantation, c) structure with pockets and in source/drain, and d) final geometry.

There are four geometry snapshots represented in this figure. The first shows the patterning of the fin area, which is essentially the first 3-D mask in the simulation. Protective Oxide and Nitride hard mask is used for this step. The second snapshot is the SRAM structure geometry just before source/drain extension implantation—it includes the Polysilicon gate, extension Nitride spacer, sacrificial oxide for the implantation, and the resist to protect the N-FinFET during the implantations for P-FinFETs. The third structure shows the pockets. And the final geometry includes the silicides in the pockets. The pocket shapes in this simulation are created by polyhedron insertion. The other operations utilize Sentaurus Process etching and deposition capabilities.

Next, we discuss and interpret the simulation results. In a previous study, proximity effects in planar CMOS SRAM cell were simulated leading to the observation that both stress and doping profiles can be altered due to the close proximity of the transistors in the SRAM cell [6]. We apply the same approach to this 6T-FinFET SRAM cell: compare the transistors performance simulated stand-alone with the ones in SRAM cell. Differences in the device performance are attributed to proximity effects, or deterministic variations. In order to show the doping proximity effects due to implantation we present the implantation profiles after P-FinFET halo in Figure 3.

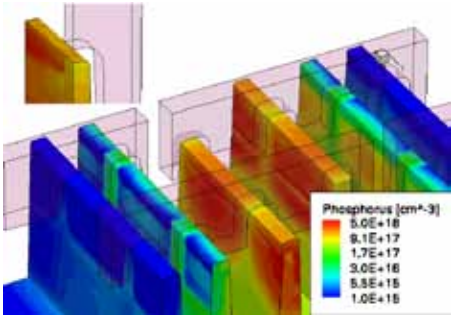

Figure 3: Phosphorus distribution in stand-alone P-FinFET (upper left corner) and 6T-FinFET SRAM cell after halo implantation.

Close examination reveals two discernible differences in the doping profiles: channel doping is lower in the SRAM cell due to resist shadowing, and there is contamination on the N-FinFET sidewalls, closest to the P-FinFET domains. The last effect is due to the implantation through the resist covering the sidewalls. These doping proximity effects are much more pronounced in the FinFET SRAM than the planar CMOS SRAM due to the closer spacing between different polarity transistors, as well as the three-dimensional nature of this technology. We anticipate large efforts for the optimization of such technologies, including the optimization of doping profiles for transistor performance and the doping uniformity in the 3-D channel. Possibly there will be alternative solutions to minimize doping proximity effects such as un-doped channel or alternative doping techniques plasma doping (PLAD). But there are some drawbacks to these approaches as well. In any case 3-D TCAD is very valuable tool for the development and optimization of FinFET doping.

Stresses are also well known to show some layout dependence. Comparison of the stress distribution in the SRAM cell and stand-alone FinFET devices are illustrated in Figure 4.

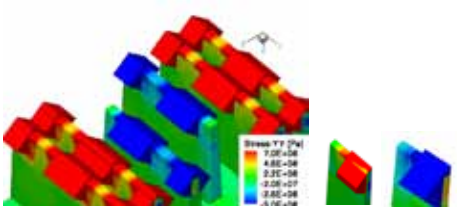

Figure 4: Stress distribution in 6T-FinFET SRAM cell as compared to stand-alone simulations.

In this simulation, the lattice mismatch between the silicon and the pockets are the main source of stresses. One can notice the differences in stresses between the stand-alone transistors and the ones in the SRAM cell. The channel stresses in the SRAM cell are actually larger than the ones in the discrete devices. And if the P-FinFET differences are relatively small, the stresses are visibly higher in the SRAM N-FinFETs compared to the discrete devices. The increased stresses in P-FinFET are attributed to the larger pocket in the middle of the SRAM as being a larger source. In P-FinFET, in addition to the larger stress pockets, the transistor's source/drain pockets are connected, restricting the degrees of freedom for stress relaxation. These results are somewhat counter-intuitive and opposite to the ones observed in planar CMOS SRAM technology, which underscores the importance of full SRAM simulation for obtaining trustworthy results.

The proximity effects discussed above have an effect on the device performance. In Figure 5 we present the electrical characteristics for the devices discussed in this article.

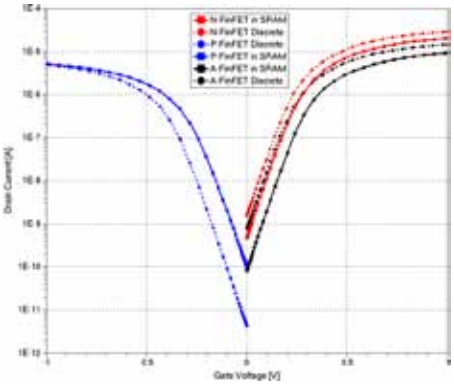

Figure 5: IdVg curves at low drain bias 0.05 V for N-, P-, A-(access) FinFET transistors. The results for discrete devices are shown with dashed curves and the ones for the SRAM transistors with solid ones.

N-, and P- devices show different behavior due to the previously discussed proximity effects. There is significant increase in leakage, decreased threshold voltage for the P-FinFET. This is primarily due to the reduced doping in the channel. The N-FinFETs show higher current levels, especially at high bias (higher I_{on} currents). This is primarily due to the stress proximity effects.

A figure of merit for the SRAM cell is the static noise margin (SNM). Examples that illustrate 6T-FinFET SRAM cell operation are shown in Figure 6.

The cell shows reasonably high static noise margin. TCAD was extensively used to optimize the doping and stress of the cell in order to obtain reasonable results.

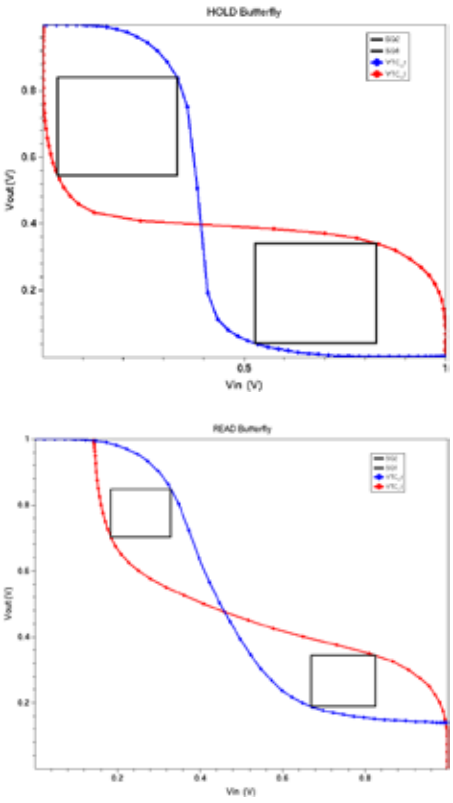

Figure 6: 6T-FinFET SRAM cell butterfly curves and static noise margin (SNM) for different states: HOLD (top) and READ (bottom).

Conclusions

We have demonstrated the Sentaurus TCAD capabilities for simulating next-generation logic devices using as an example a 6T-FinFET SRAM cell. Some interesting 3-D proximity effects were highlighted. This further illustrates the value of TCAD for the development of "More Moore" devices and their optimization.

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