

Latest Edition

As this June edition of *TCAD News* goes to press, power device technologists from the world over are gathering at the 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD) in San Diego, California.

In the run up to ISPSD 2011, several market studies project significant growth for the power management sector to service traditional and emerging applications such as hybrid and electric vehicles, and smart grid.

Our customers are actively developing new silicon and wide-bandgap power device technologies to address these applications.

While TCAD Sentaurus has been widely deployed for modeling power devices, we continue to enhance its capabilities for analyzing and characterizing conventional as well as novel types of power devices.

This edition reports on the use of TCAD Sentaurus for modeling two wide-bandgap power devices: a p-gate GaN HEMT and a SiC IGBT, which are some of the latest innovations in the power device community to push the envelope for higher voltage and frequency, while maintaining low on-resistance.

I trust you will enjoy reading *TCAD News* and, as always, we welcome your feedback and suggestions for future topics.

With warm regards,

Terry Ma

Vice President of Engineering, TCAD

TCAD news

Recent Progress in the Simulation of GaN Devices with TCAD Sentaurus

Introduction

For over a decade, gallium nitride (GaN) high-electron mobility transistors (HEMTs) have attracted considerable attention as high-power and high-frequency devices for radar, avionics, and wireless base-station transmitters. More recently, GaN HEMTs have been considered for power-switching applications, with many established and emerging companies reporting device results. Much of the market promise for these devices stems from the unique physical properties of the III-nitride (III-N) material system, which comprises GaN and associated ternaries such as AlGaIn and InGaIn. The wide energy gap of GaN supports a large breakdown electric field, while a very high two-dimensional (2D) electron gas density, resulting from its strong polarization effects, supports large currents. The combination of these two characteristics, high current and high voltage capability, promises devices with superior power-handling and low on-resistance.

Simulating GaN Devices: From Reliability to Product Design

Early efforts to develop GaN HEMT technology centered largely on characterization, physical understanding, and process development to mitigate the trapping effects that hampered the commercialization of these devices for many years. Naturally, earlier TCAD simulations focused on providing insights into the bulk

and surface trapping behavior to guide process improvements, for example, by limiting carbon impurities in buffer layers, and to optimize the device structure to reduce operational conditions conducive to trapping. An important illustration of these early efforts was the simulation study of the impact of field plates on the electron temperature in the channel. Field plates were shown to reduce the electric field at the drain edge of the gate, contributing to a reduction of the electron temperature and trapping [1]. Without a field plate, hot electrons diffused into the bulk where they became trapped. When a field plate is inserted into the structure, the lower electron temperature limits the spillover of electrons from the channel into the bulk, thereby reducing trapping. Gate-lag transient simulations revealed key insights into the so-called current collapse phenomena. It was shown that field plates yield an almost complete recovery of the drain current following a gate off-on switching pulse.

With improvements to epitaxial material and processing, devices with nearly ideal characteristics have been demonstrated. Although extensive reliability studies of GaN devices continue, a new phase has been entered where simulation of GaN devices is used in a more conventional way, as a tool for designing and optimizing

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device structures for specific application scenarios. In this article, one such scenario is discussed: the design of a normally off device for power-switching applications.

Model Requirements

Before discussing the design of a normally off GaN HEMT, the model requirements for GaN simulation are reviewed briefly. The simulation of GaN HEMTs presents several challenges and needs to account for the polarized wurtzite crystal structures of AlGa_{0.23}Ga_{0.77}N, InGa_{0.23}Ga_{0.77}N, and GaN, which have dipoles across the crystal in the [0001] direction. These dipoles can cause spontaneous (pyroelectric) polarization, while pseudomorphic heterostructures fabricated from these III–Ns also exhibit strain-induced (piezoelectric) polarization. The primary effect of the polarization is an interface charge due to abrupt variations in the polarization at the AlGa_{0.23}Ga_{0.77}N–GaN heterointerface and at the AlGa_{0.23}Ga_{0.77}N surface [2]. The resulting values are computed automatically using the built-in strain piezoelectric polarization model in Sentaurus Device [3]. Quantization effects at the AlGa_{0.23}Ga_{0.77}N–(In)Ga_{0.23}Ga_{0.77}N heterointerface create a 2D electron gas channel. A quantum-mechanical solution is needed to properly account for the electron spatial distribution in this channel. Sentaurus Device uses a quantum potential correction to the continuity equation, known as the density gradient. This closely matches the solution to the full Schrödinger equation, while improving the robustness of the simulation and providing a five-fold to ten-fold reduction in computation time. When simulating hot-carrier effects and dynamic trapping/detrapping, hydrodynamic transport models should be used to properly account for the influence of the carrier energy on trapping/detrapping phenomena.

Normally Off p-Gate GaN HEMT

Device Structure

The simulation project, described in detail in an application note [4], provides a device

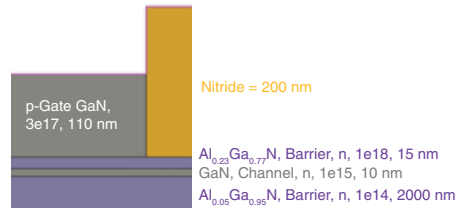


Figure 1: Cross section of simulated device structure (gate region).

simulation setup for a normally off p-gate GaN HEMT based on a structure reported in the literature [5]. Since the publication does not report key structural parameters, reasonable assumptions are made to create a structure consistent with the device performance results. It includes a 2 μm Al_{0.05}Ga_{0.95}N buffer layer, a 10 nm GaN channel layer, and a 15 nm Al_{0.23}Ga_{0.77}N barrier layer. The gate is an 110 nm p-type GaN layer. The source–gate separation is 1 μm and the gate length is 1.4 μm . Figure 1 shows the cross section of the layers at the gate region. Highly doped regions are created under the source–drain electrodes down to the GaN channel to emulate metal spikes and to control contact resistance. Mg-doped GaN is used as the p⁺ gate to deplete the channel at $V_g = 0$, yielding a normally off transistor and satisfying a key requirement for operation in power-switching applications, as mentioned in the introduction. The AlGa_{0.23}Ga_{0.77}N buffer is used to increase the threshold voltage (V_{th}), while reducing the R_{on} with a higher Al content barrier. The AlGa_{0.23}Ga_{0.77}N buffer also suppresses punch-through [5]. The built-in strain piezoelectric polarization model in Sentaurus Device computes the polarization-induced charges at the heterointerfaces.

Simulation Setup

Sentaurus Structure Editor defines the device structure, and Sentaurus Workbench parameters define the structural variables for optimization:

- ▶ Length of the field plate (FP)
- ▶ Gate–drain distance (Lgd)
- ▶ Doping level of the top AlGa_{0.23}Ga_{0.77}N barrier layer (AlGa_{0.23}Ga_{0.77}N_Doping)

Two device structures are simulated. Structure 1 has FP = 1.8 and Lgd = 6 μm . Structure 2 has a longer field plate with FP = 8 and Lgd = 18 μm . Both structures have AlGa_{0.23}Ga_{0.77}N_Doping = $1e18\text{ cm}^{-3}$.

Device Simulations

To assess the device performance for power-switching applications, I_d – V_g , I_d – V_d , and off-state breakdown voltage sweeps are performed. In the device simulations, the spontaneous and piezoelectric polarization is simulated automatically by including Piezoelectric_Polarization(strain) in the Physics section of the command file.

The Al_{0.05}Ga_{0.95}N buffer is assumed to be completely relaxed, and the subsequent layers (channel and barrier) are strained to match the lattice constant of Al_{0.05}Ga_{0.95}N but with 20% of relaxation. The large polarization divergence at the AlGa_{0.23}Ga_{0.77}N barrier surface (barrier–nitride interface) produces a huge sheet of negative polarization charge. This would accumulate holes at that interface and completely deplete the channel of electrons. In reality, it is still unclear whether the polarization charge is compensated by fixed charges or interface trap states. In this example, accumulated holes at the surface of the AlGa_{0.23}Ga_{0.77}N barrier are completely compensated by deep, single-level trap states.

To match the subthreshold slope of the I_d – V_g curve in [5], traps are added to the AlGa_{0.23}Ga_{0.77}N barrier–GaN channel interface. As expected, the simulations reveal that the passivation nitride thickness and field-plate length impact the off-state leakage current and the breakdown voltage. Moreover, traps in the buffer affect both the subthreshold slope and the off-state leakage current.

In large bandgap semiconductors, the intrinsic carrier density is extremely small. For this reason, it is recommended to adjust some of the default settings of the numeric solvers to improve robustness and accuracy. Recommended settings for GaN device simulations are discussed in the application note [4]. In the simulations, Schottky

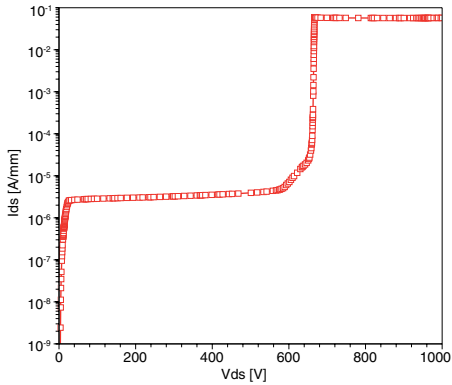


Figure 2: Off-state leakage curve of FP = 8 and Lgd = 18 structure.

contacts are used in the source and drain. Electron tunneling is switched on, and the electron tunneling mass is made to be arbitrarily small, so the contact is essentially Ohmic. This method improves convergence and avoids abrupt band bending near the contacts. Users also can tune the tunneling mass to model contact resistance.

Figure 2 shows the off-state breakdown voltage characteristics for a structure with an 8 μm field plate and gate-drain distance of 18 μm . The high breakdown voltage observed (>600 V) is indicative of the potential applications for these devices.

Figure 3 shows the I_d-V_g and I_g-V_g characteristics. The gate current is more than four orders of magnitude below the drain current, indicating good gate control

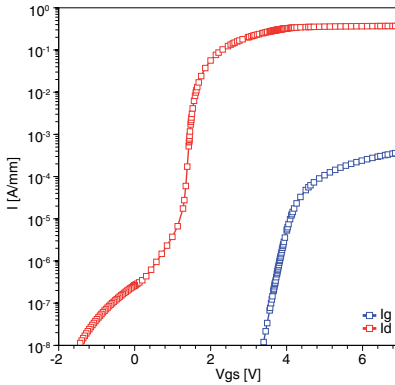


Figure 3: I_d-V_g and I_g-V_g curves of FP = 1.8 and Lgd = 6 structure with $V_d = 15$ V.

at $V_d = 15$ V. Finally, Figure 4 shows the I_d-V_d curves. The negative output conductance exhibited by the $V_g = 5$ V curve is due to self-heating effects.

Conclusion

The unique material attributes of GaN and its related materials are being exploited to produce new power devices with higher power density, lower on-resistance, and higher efficiency. TCAD Sentaurus has extensive capabilities to simulate GaN-based devices and is used increasingly to develop and optimize this promising technology.

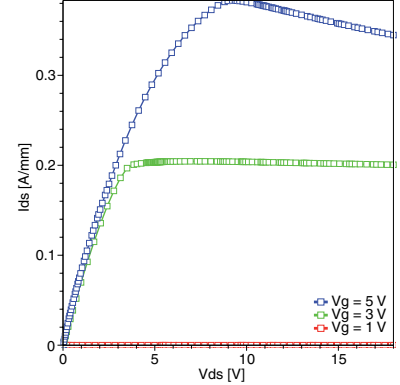


Figure 4: I_d-V_d curves of FP = 1.8 and Lgd = 6 structure.

References

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Simulation of SiC p-IGBT in Sentaurus Device

Introduction

Silicon carbide (SiC) is well recognized as a superior semiconductor for power device applications. Compared to silicon, its breakdown electric field is an order of magnitude higher, and its thermal conductivity is approximately three times as high, enabling devices with higher power ratings and improved thermal dissipation. Although SiC power devices have been

commercially available for several years, the pace of device development has increased recently due to improvements in substrate technology – 100 mm substrates with low micropipe density are readily available and 150 mm substrates have been demonstrated – and to market pull for new applications. One key emerging application for SiC power devices is hybrid and electric vehicles where higher efficiency converters promise to

increase fuel efficiency [1]. As SiC device design and optimization progress, the role of TCAD simulation has grown, as a way to guide structural design to fully realize superior material attributes and to reduce the number of experimental wafers.

Simulation of SiC devices presents unique technical challenges in view of the very low intrinsic carrier concentrations due to the wide energy gap and anisotropic material

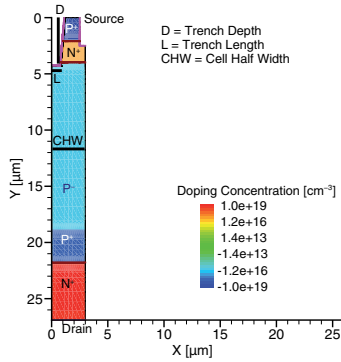


Figure 1: p-IGBT device structure created with Sentaurus Structure Editor.

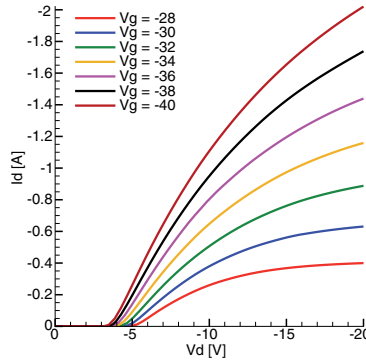


Figure 2: I_d - V_d characteristics for various gate voltages.

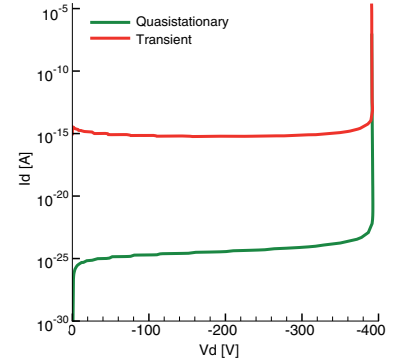


Figure 3: Breakdown voltage characteristics simulated using transient and quasistationary methods.

properties such as carrier mobility, thermal conductivity, electrical permittivity, and impact ionization, which result from the hexagonal crystal structure. In the June 2010 edition of *TCAD News*, there was a report on the calibration of SiC physical models in Sentaurus Device, and a 4H-SiC VJFET example was discussed.

6H-SiC p-IGBT Example

In this article, a 6H-SiC p-IGBT example is presented. An associated application note will become available from SolvNet®. The device structure is shown in Figure 1 and is based on the structure reported by Singh *et al.* [2].

The physical models used in the simulation include:

- ▶ Incomplete dopant ionization
- ▶ Interface charge traps at SiC/SiO₂ interface
- ▶ Doping- and temperature-dependent Shockley-Read-Hall recombination
- ▶ Mobility model with degradation due to doping, surface roughness, acoustic phonon scattering, and high electric field saturation
- ▶ Bandgap narrowing
- ▶ Okuto-Crowell avalanche model

Due to the wide band gap of SiC, the intrinsic carrier concentration is very small relative to other semiconductors such as gallium

arsenide. This leads to numeric challenges that can be addressed with SiC-specific settings for the matrix solvers and by using extended precision floating-point arithmetic. Details about extended precision arithmetic can be found in the associated application note.

Device Simulation Results

Sentaurus Device is used for device simulation. The I_d - V_d characteristics are simulated with the *transient method*, which applies a slowly varying ramp signal to the device terminal instead of sweeping the terminal voltage in quasistationary mode. This technique improves simulation robustness. Figure 2 shows the I_d - V_d characteristics with gate voltages ranging from -28 V to -40 V in steps of -2 V, and the drain voltage is swept from 0 to -20 V. The drain current at $V_g = -40$ V and $V_d = -12$ V is -1.4 A, and the knee voltage is -2.7 V. Both closely match the published data [2].

The breakdown voltage characteristics are simulated with the Okuto-Crowell model and special numeric settings for handling the extremely small leakage present in the device in the off-state. Both the transient method and the quasistationary method are used to simulate the breakdown voltage. When using the quasistationary method, extended precision (128) is used as the

off-current values are in the range of 10⁻²⁵ A. However, for the transient method, extended precision (80) can be used to speed up the computation time.

Figure 3 shows the breakdown voltage characteristics obtained from the transient and quasistationary methods. As expected, both curves show the same breakdown voltage values. However, the quasistationary method predicts less off-current than the transient method. The higher off-current seen with the transient method is due to displacement current because the ramp signal is applied at the drain terminal.

Conclusion

SiC devices are being investigated to improve the power switching and conversion efficiency of key systems such as hybrid and electric vehicles. TCAD Sentaurus offers comprehensive capabilities for simulating this emerging technology and supports the 4H and 6H polytypes.

References

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