SYNOPSYS®
Predictable Success

Newsletter for semiconductor process and device engineers March 2011

TCAD news

Latest Edition

The trends in semiconductor technology towards smaller feature sizes and higher integration, along with extensions in the safe-operation area of power devices, lead to a number of reliability issues whose characterization and mitigation are fundamental parts of technology development and product design. TCAD simulation of reliability phenomena is increasingly important in semiconductor technology development as a way to provide insight into the physics of the underlying degradation mechanisms and to guide process changes to improve reliability.

We dedicate this edition of *TCAD News* to device reliability, as its relevance and importance continue to grow.

The first article discusses the latest TCAD models for simulating negative bias temperature instability, which impacts PMOS device reliability.

In the second article, we review the effect of hot carriers in semiconductor device operation and reliability, and illustrate the combination of hot-carrier energy and degradation models in simulating channel-initiated secondary-electron (CHISEL) current in flash memory cells.

I trust you will find these articles informative and, as always, I encourage you to send us your feedback.

With warm regards,

Terry Ma
Vice President of Engineering, TCAD

Contact TCAD
For further information and inquiries:
tcad_team@synopsys.com

Simulation of NBTI Degradation with Two-Stage Model

Introduction

Negative bias temperature instability (NBTI) is a major reliability issue in CMOS technology. NBTI degrades the threshold voltage on PMOS transistors, leading to an increase in the drain current over time in both the DC and AC operations of circuits. Despite considerable research, the chemical and physical mechanisms underlying NBTI degradation are not fully understood and remain an active research topic. In past releases, Sentaurus Device implemented models for the reaction–diffusion mechanism that, when coupled with the multistate configuration framework, could be used to treat the interactions of hydrogen with dangling bonds. However, reaction–diffusion theory has been unable to account for the full dynamic behavior of NBTI recovery and, at best, has provided an intermediate modeling solution before a complete theory is formulated.

Recently, Grasser and coworkers proposed a two-stage NBTI degradation model and demonstrated its applicability to different technologies (high-k metal gate, SiO_2, SiON) over a wide range of stress voltages, times, and temperatures [1]. Since the model can reproduce both the degradation and the recovery phases of NBTI, it is particularly useful in the AC stress regime. The model was implemented in Version E-2010.12 of Sentaurus Device.

This article describes the major features of this two-stage model and its use for a 32-nm technology node PMOS transistor.

Model Description

The two-stage NBTI model is built around the concept of E′ centers and their behavior as a switching trap in a multistate model. The model assumes that a certain initial concentration of precursors, which are oxygen–vacancy structures containing a Si–Si bond. This is state 1 of the model. When voltage stress is applied, holes tunnel from the channel into the precursor structures near the interface. When a hole is trapped in a precursor, it breaks up the Si–Si bond and creates a positively charged E′ center. This is state 2. The E′ center can become neutral as a result of hole emission (electron capture), corresponding to state 3. The neutral E′ center can over time repair the Si–Si bond and revert to the original precursor, or state 1. The occupancies and kinetics among these three states constitute the first stage of the model.

The second stage of the model accounts for the creation of poorly recoverable defects. In a positively charged E′ center (state 2), the trapped hole ties up one of the Si bonds, while the other Si bond is unpassivated. However, the bond inside the E′ center can become passivated by acquiring a hydrogen dislodged from a passivated Si dangling bond at the interface. When the hydrogen

In This Edition

moves to the E′ center, it locks in the positive charge, effectively preventing or delaying the recovery of the E′ center defect, and leaves behind an unpassivated dangling bond at the interface known as a P_b center. In oxynitrides, so-called K_n centers are created, and the formulation is similar. This process of hydrogen migration to the dangling bonds inside E′ centers has been shown to be energetically favorable. To handle this coupling between E′ centers and P_b centers, the model introduces a fourth state to represent the E′/P_b hydrogen complex.

The dynamics of the transitions among the four states are treated with the following rate equations:

$$\dot{s}_1 = -s_1 k_{12} + s_3 k_{31}$$

$$\dot{s}_2 = s_1 k_{12} - s_2 (k_{23} + k_{24}) + s_3 k_{32} + s_4 k_{42}$$

$$\dot{s}_3 = s_2 k_{23} - s_3 (k_{32} + k_{31})$$

$$\dot{s}_4 = s_2 k_{24} - s_4 k_{42}$$

Here, s_i are the state occupancy probabilities that satisfy the normalization condition:

$$\sum_{i=1}^{4} s_i = 1$$

The transition rates are given by:

$$k_{12} = e_C^{n,1} + c_V^{p,1}$$

$$k_{23} = c_C^{n,2} + e_V^{p,2}$$

$$k_{32} = e_C^{n,2} + c_V^{p,2}$$

$$k_{31} = \nu_1 \exp(-E_A / kT)$$

$$k_{24} = \nu_2 \exp[-(E_D - \gamma F)/kT]\Theta(C - r)$$

$$k_{42} = \nu_2 \exp[-(E_D + \gamma F)/kT]\Theta(C - r)$$

where:

- ν_i are the attempt frequencies.
- γ is the prefactor for the field-dependent barrier energy.
- $e_C^{n,i}$ and $c_C^{n,i}$ are the electron emission and capture rates.
- $e_C^{p,i}$ and $c_C^{p,i}$ are the hole emission and capture rates.

A salient feature of the model, due to the amorphous characteristics of dielectric materials, is the treatment of the trap levels for the precursor, the E′ center, and the P_b center as random variables. Similarly, the barrier energies for the state transitions from s_3 to s_1, s_1 to s_2, and s_2 to s_4 are treated as random variables as well. Compared to previous models, the two-stage NBTI model accounts for asymmetry in the degradation. As seen in Figure 1, a rapid increase in interface charge density (corresponding to an increase in V_{th}) during the stress phase is followed by a much more gradual relaxation when the stress is removed.

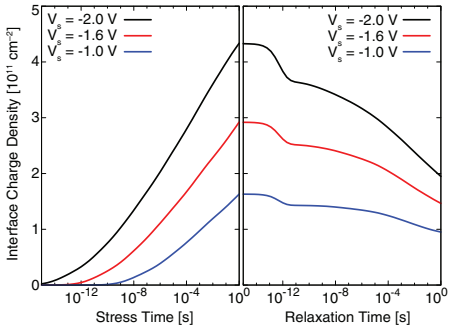


Figure 1: Calculated interface charge density of a PMOSFET as a function of stress and relaxation times for three different stress voltages. The simulated PMOSFET has a p-type polysilicon gate, a SiON dielectric with an effective oxide thickness of 1.4 nm, and a substrate with n-type doping of 2×10^{18} cm^{-3}. The relaxation voltage is –0.3 V, and the lattice temperature is 323 K. It is assumed that each sample is in the precursor state at the beginning.

Simulation Example

In the following example, the two-stage NBTI model is applied to a two-dimensional 32-nm node PMOS structure. The threshold voltage degradation is simulated during the electric stress (high gate voltage) and the recovery (low gate voltage) stages.

As discussed in [1], various experimental methods are used to evaluate the threshold voltage degradation due to NBTI. Depending on the method used, you can further model the effects of the trapped charge on the threshold voltage degradation. TCAD simulation allows for a direct calculation of the experimentally measured quantities of a particular experimental procedure and eliminates the need for additional assumptions in the modeling of the results.

Following [1], the so-called on-the-fly (OTF) technique is applied to the test structure. To reproduce typical experimental conditions, a small 50 mV bias is applied to the drain. The drain current is monitored for different gate voltages (electrical stress) as a function of time. In the OTF method, the threshold voltage is obtained from the relationship for the transconductance ($g_m = dI/dV$) as $\Delta V_{th} = (I(t) - I(t_{ref}))/g_m$.

Here, I(t) is the measured (or calculated) current at the time t and $I(t_{ref})$ is the measured current at the delay time t_{ref}. Therefore, calculating the time dependency of the current under the stress and transconductance g_m allows the calculation of the threshold voltage shift.

Figure 2 shows the change of the threshold voltage for three different gate stresses. Figure 3 shows the recovery of the threshold voltage after the stress has been lifted. These results demonstrate that, in agreement with [1], the relaxation happens

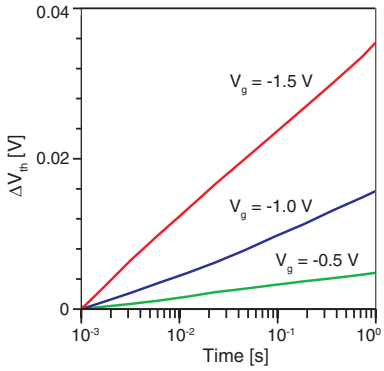


Figure 2: Dependency of threshold voltage shift during the stress phase and relaxation phase for three stress voltages on gate V_g.

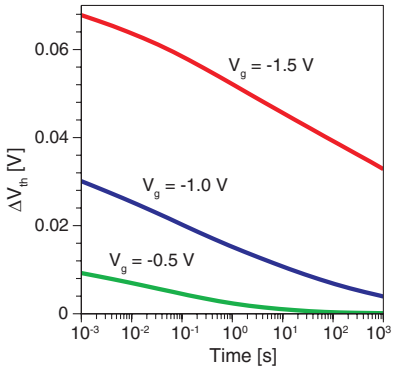


Figure 3: Dependency of threshold voltage shift during the recovery phase for three stress voltages on gate V_g.

on a longer timescale, particularly for a higher stress voltage.

Conclusion

NBTI is a significant degradation mechanism in PMOS transistors. With the addition of the two-stage NBTI model to the family of Sentaurus Device degradation models, users now have access to a comprehensive model framework for simulating and researching this important effect.

References

[1] T. Grasser *et al.*, "A Two-Stage Model for Negative Bias Temperature Instability," in *International Reliability Physics Symposium (IRPS)*, Montréal, Québec, Canada, pp. 33–44, April 2009.

Simulation of Hot-Carrier Effects with TCAD Sentaurus

Motivation for Simulating Hot-Carrier Effects

An electron enters a region of high electric field, and it quickly begins to gain energy. The usual processes by which it loses energy to the lattice, for example carrier–phonon interactions, are not sufficiently frequent to restrain the rise in energy that is no longer in equilibrium with the lattice; the electron becomes a *hot electron*. Along with its counterpart, a *hot hole*, the hot electron and the hot hole are loosely designated as *hot carriers*. While some devices rely on hot carriers for their operation – Gunn-effect diodes and NOR flash devices are prominent examples – others avoid the conditions leading to their generation altogether so as to maintain reliable operation.

Whether they aid or impede device operation, hot-carrier effects are an important component of many device simulations, and their relevance continues to grow as the regions of high electric fields in devices are more readily established due to the trends to shrink dimensions (logic devices) or to operate at higher voltages (power devices).

Among the hot-carrier effects, hot-carrier injection (HCI) demands considerable attention since it often leads to degradation in device operation. In general, TCAD simulation has shown to be an effective tool for seeing inside devices in ways that are not convenient or are plainly impossible with experimental characterization alone, and HCI simulation should be no exception. However, simulating HCI-induced degradation is challenging as it must account for many physical phenomena: generation and transport of hot carriers, carrier injection or tunneling across interfaces, breaking of passivating bonds and trap generation, and so on.

The physical models underlying these phenomena range from 'well-known and requiring more extensive computational resources' for hot-carrier generation and transport, to 'phenomenological and requiring calibration to the process' for the breaking of bonds, trap profiles, and trap energies.

Despite these challenges, recent simulation studies have opened new vistas into the value that TCAD provides in characterizing HCI-induced degradation and in optimizing device structures to mitigate its impact [1][2].

Simulation of CHISEL in Flash Memory

To illustrate the application of Sentaurus Device to HCI-induced degradation, a simulation project based on channel-initiated secondary-electron (CHISEL) injection in flash memory is discussed. CHISEL injection aims to generate higher gate currents than the traditional channel hot-electron (CHE) mechanism, thereby boosting programming speed. The CHISEL technique is a two-step process. Under a large parallel electric field (along the channel), holes are generated by impact ionization. Subsequently, these holes flow towards the substrate under a high substrate bias and, in turn, they initiate secondary electron–hole pairs. The electrons so created gain energy as they flow towards the surface, generating a gate current. The CHISEL-generated gate current is approximately an order of magnitude higher than the CHE-generated current, and it has a distinct signature [3].

The simulation project contrasts CHISEL and CHE operations, and studies CHISEL-induced device electrical degradation. It is based on the standard 130 nm NMOSFET provided in the Applications Library of TCAD Sentaurus Version E-2010.12. The device structure is shown in Figure 1. Noteworthy physical models used in the simulation include the Philips mobility model with high field saturation and transverse field dependency, Shockley–Read–Hall and Auger recombination, and the spherical harmonics expansion (SHE) hot-carrier injection model. The SHE model estimates the hot-electron injection current flowing into the gate electrode. Figure 2 shows the drain and substrate currents as a function of gate voltages for a range of substrate applied voltages.

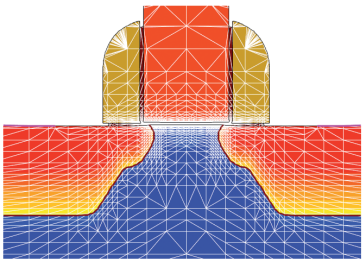


Figure 1: MOSFET structure used in CHISEL simulation project.

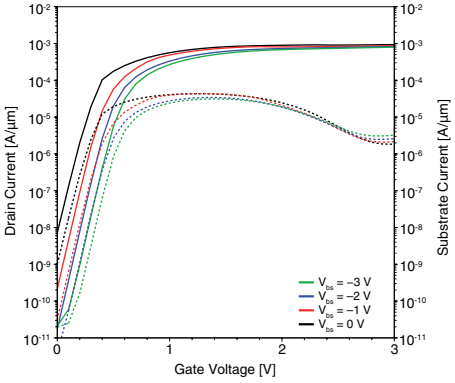


Figure 2: Simulated MOSFET I_d–V_{gs} and I_b–V_{gs} curves for different substrate biases.

The expected order-of-magnitude difference in the gate current, when the device is biased in CHE and CHISEL conditions, is clearly seen in Figure 3. For higher substrate bias voltages used in CHISEL (–2 V and –3 V), a significantly higher gate current is observed. To simulate the MOSFET degradation under CHISEL electrical stress conditions, the interface trap degradation model is used. The kinetic reaction constant enhancement in the trap formation equation is switched on with an enhancement term that takes SHE HCI into account:

$$\nu = \nu_0 \exp\left(\frac{\varepsilon_A^0}{kT_0} - \frac{\varepsilon_A^0 + \Delta\varepsilon_A}{\varepsilon_T}\right) k_{\mathrm{SHE}}$$

where $\varepsilon_A{}^0$ is an activation energy, ε_T is the Si–H bond energy, and k_{SHE} is expressed as:

$$k_{\mathrm{SHE}} = 1 - \delta_{\mathrm{SHE}} \frac{q g_\nu}{2} \int_{\varepsilon_{\mathrm{th}}}^{\infty} \left(m(\varepsilon)\, g(\varepsilon)\, f(\varepsilon)\, \nu(\varepsilon) \right) d\varepsilon$$

where:

- $m(\varepsilon) = \min\left[\exp\left(\frac{\varepsilon - \varepsilon_a + \delta_\perp |F_\perp / F_0|^{\rho_\perp}}{kT}\right), 1\right]$
- δ_{SHE} is a prefactor.
- $\varepsilon_{\mathrm{th}}$ is a threshold energy.
- ε_a is an activation energy.
- $\delta_\perp$ is a normal field–induced activation energy–lowering factor.
- $\rho_\perp$ is a normal field–induced activation energy–lowering exponent.
- F_0 = 1 V/cm.
- g_ν is the valley degeneracy.
- g is the density-of-states.

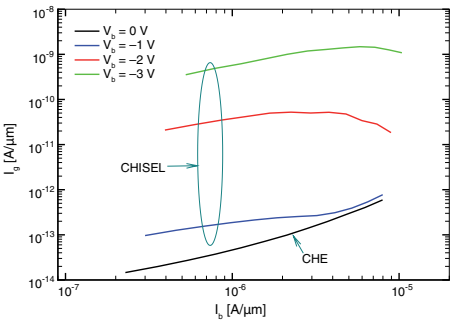


Figure 3: Gate current versus substrate current for bias conditions corresponding to CHE (V_b = 0 V) and CHISEL (V_b = –1 V, –2 V, –3 V) conditions.

The interface trap profile distributions resulting from CHE and CHISEL electrical stress conditions are shown in Figure 4.

The interface trap profile is subsequently loaded into a new device simulation to estimate device performance after the degradation. Users can define their own metric of device degradation. In the project, the difference in the threshold voltage before and after the degradation is used as a metric, as shown in Figure 5.

The simulations indicate that the CHISEL operation effectively increases the gate HCI, thereby providing a mechanism to shorten program/erase time. However, the CHISEL operation may lead to faster degradation, motivating the use of simulation to study

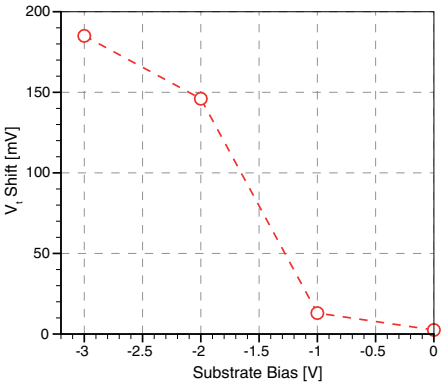
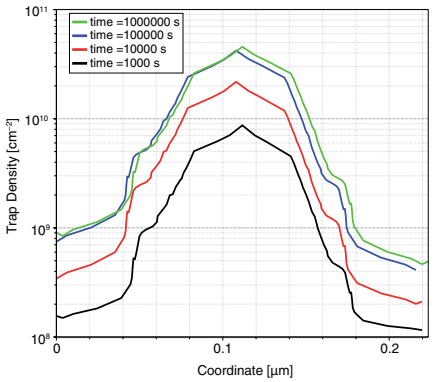


Figure 5: Threshold voltage shift after device degradation as a function of applied substrate bias, with the device subjected to CHE/CHISEL electrical stress conditions at $t_{\mathrm{stress}} = 10^6$ s.

specific CHISEL operation regimes to ensure adequate device reliability.



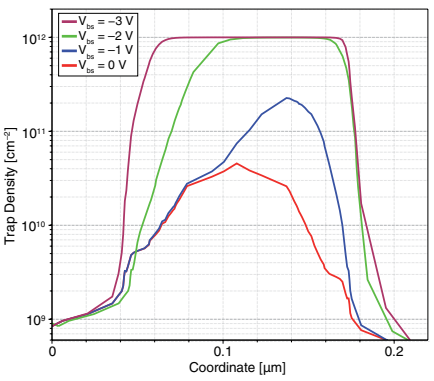


Figure 4: (*Left*) Interface trap profile distributions along the channel obtained for different stress times under CHE bias conditions. (*Right*) Comparison of interface trap profile distributions along the channel for CHE and CHISEL bias conditions at $t_{\mathrm{stress}} = 10^6$ s.

References

[1] S. Reggiani *et al.*, "Analysis of HCS in STI-based LDMOS transistors," in *International Reliability Physics Symposium (IRPS)*, Anaheim, CA, USA, pp. 881–886, May 2010.

[2] S. Bach *et al.*, "Simulation of Off-State degradation at high temperature in High Voltage NMOS transistor with STI architecture," in *22nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Hiroshima, Japan, pp. 189–192, June 2010.

[3] F. Driussi, D. Esseni, and L. Selmi, "Performance, Degradation Monitors, and Reliability of the CHISEL Injection Regime," *IEEE Transactions on Device and Materials Reliability*, vol. 4, no. 3, pp. 327–334, 2004.

SYNOPSYS®

Predictable Success

Synopsys, Inc. • 700 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

03/11.DP.CS424.