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Newsletter for semiconductor process and device engineers

September 2011

TCAD news

New Features and Enhancements in TCAD Sentaurus F-2011.09

This issue of TCAD News is dedicated entirely to the F-2011.09 release of TCAD Sentaurus, sequentially describing the new features and enhancements in Sentaurus Process, Sentaurus Device, Sentaurus Interconnect and Sentaurus Structure Editor.

Sentaurus Process

The F-2011.09 release of Sentaurus Process encompasses a broad range of new capabilities. In the implant module, we have worked with a leading equipment vendor to improve plasma doping (PLAD) accuracy, a process technique of growing relevance in leading-edge silicon processing. Mesh refinement based on layout masks has been improved. In this release we target implant lateral scattering and lateral diffusion with a new mask edge-based refinement. This enhancement, coupled with a new way to retrieve implant moments, allows the user to identify areas for mesh refinement. Another convenient new feature is the introduction of a 3D shape library. In this first implementation, the library has shapes which allow the creation of STI regions with straight, inner and outer corners, diamond shapes for convenient formation of SiGe S/D regions, among others. We have added 3D crystallographic deposition and improved 3D crystallographic etch. Also introduced are a new method for generating structures with line edge roughness (LER) and a convenient and efficient way to transfer kinetic Monte Carlo (KMC) simulation results to a structure for device simulation. In keeping with our continued effort to improve simulation performance, improved scaling of process simulation parallelization is reported.

PLAD Model

Plasma immersion ion implantation is a promising technology for semiconductor processing due to its relative equipment simplicity, compatibility with cluster tools, high throughput (especially at very low energy), and conformal doping. Due to these advantages, plasma implant is suitable for ultra-shallow junction formation, high dose source-drain doping, and sidewall doping in deep trenches.

During plasma immersion ion implantation, ionized species present in the plasma are extracted and implanted into the wafer, while other processes such as deposition, etching and sputtering, occur in parallel. All these mechanisms contribute to the resultant dopant profile in the silicon. The new plasma doping (PLAD) module in Sentaurus Process accurately reflects both the hardware and process signatures as well as the physical properties of the associated deposition, etching, sputtering, implantation, knock-on, defect creation and annihilation processes.

The key features of the PLAD model include the simultaneous implantation of multiple species and the deposition of doped material during implantation. Due to the lack of ion mass separation, PLAD doping usually involves multiple implanted species consisting of multiply-charged components with a range of energies. Users can specify multiple species in the implant command by using parameter `plasma.source=`

Latest Edition

Despite the current economic challenges, the semiconductor industry continues to strive to develop innovative processes and devices to fuel the growth in smart technologies. While the development of leading-edge Tri-gate transistors takes center stage recently, the pace of research in silicon and wide bandgap power devices targeting emerging high-efficiency applications in solar inverters, hybrid and electric vehicles, and smart grid also accelerates. These technology trends provide the backdrop for development of the newly released TCAD Sentaurus version F-2011.09. This edition of TCAD News reports the new features and enhancements available for supporting the latest processes (for example plasma implantation, silicon stress and orientation-dependent mobility), modeling 3D structures (shapes library, crystallographic etch and deposition, line-edge roughness, Sentaurus Topography 3D interface), and simulating device variability with the Impedance Field Method. We also report on the improvements in device modeling of III-Nitride and SiC devices, application of Sentaurus Interconnect to solder joint reliability analysis, and introduce a new link between Sentaurus Interconnect and Raphael which enables RC extraction in complex interconnect structures.

I trust you will enjoy reading about these and other enhancements in the F-2011.09 release of TCAD Sentaurus. As always, I welcome your feedback and suggestions.

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{<species1>=<n> <species2=<n> …}, where the numbers after the species specify the fraction of the total dose for the given species. The existence of neutral species in PLAD doping may also involve the deposition of thin film containing the dopants. Users can specify the deposition of the material by specifying the parameter `plasma.deposit= {material=<c> thickness=<n> steps=<n>}`. Deposition of material on the surface is performed isotropically, that is, with a constant growth rate over the surface. The collisions among the ions and the neutrals in the plasma provide a spread in energy and angular distribution of the implanted ions. These can be taken into account by using the parameters `en.stdev` and `tilt.stdev`. Sentaurus Process then performs alternating steps of deposition and Monte Carlo (MC) implantation by using the number of steps specified by the user. In order to simulate the dopant knock-on or knock-off effect, users need to specify the `recoils` parameter in the `implant` command and provide information about the recoil species and material composition.

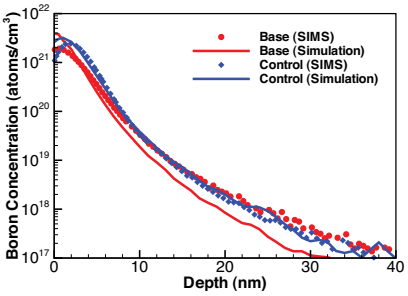


Figure 1: Simulation and SIMS measurement of plasma doped profiles. The PLAD energy is 1kV.

Figure 1 compares simulated and measured plasma doped profiles. In the profiles labeled 'control,' the plasma composition and properties were modulated using the advanced process control features in the PLAD equipment. The 'baseline' case corresponds to non-optimized conditions. The simulation dose is chosen to match the 'control' SIMS profile. All other implant conditions were extracted from the equipment data sheet. As can be seen, the simulation matches the SIMS profile very well in case of "control". In case of "baseline", the agreement is less ideal, which we attribute to the presence of a higher fraction of multiply-charged ions not accounted for in the simulation.

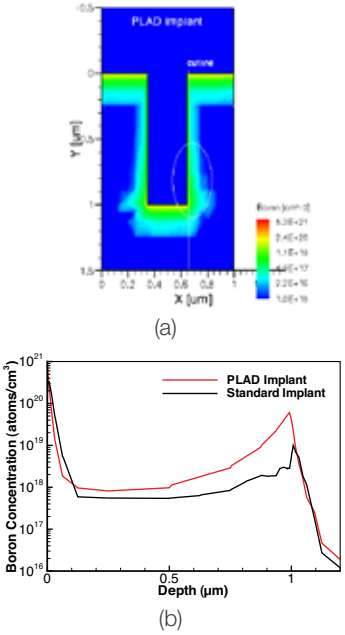


Figure 2: (a) Boron PLAD in a trench structure and (b) doping profile for a cutline 1µm deep, contrasting the PLAD profile with that obtained with standard implantation.

Figure 2 (a) illustrates boron PLAD in a trench structure. With PLAD, substantially higher doping is incorporated in the sidewall near the trench bottom due to the fact that the spread in angular ion distribution favors two processes: (a) more dopants can be knocked out of the deposit layer and either directly enter into the silicon substrate or (b) dopants are scattered into the ambient and then re-implanted into the sidewall. This can be more clearly seen in Figure 2 (b) which shows the concentration profile along the cutline at depth of 1µm into the surface. However, even though the current PLAD model predicts higher concentration near the bottom, it has less effect on the sidewall doping in the upper part of the trench. Possibly, diffusion from the deposit layer is necessary in order to achieve full conformal doping around the trench.

Mask Edge-driven Refinement Enhancements

Refinement Along Mask Edges

Previous releases already supported the definition of refinement areas from masks. The user can, for example, define a refinement area as the extrusion of the mask footprint into the depth from a given starting point to a given end point, and then define the bulk mesh refinement in this area.

In F-2011.09 the user can also request refinement along the edges of a mask. This is useful to automatically resolve the lateral straggle and diffusions of an implant. This feature is available for 2-D and 3-D. Figure 3 illustrates this new capability for a curved mask. To highlight the function only the mask edge refinement is activated. It can be seen that the tighter mesh refinement is applied only around the edges of the curved doughnut shaped mask (shows as a transparent resist block).

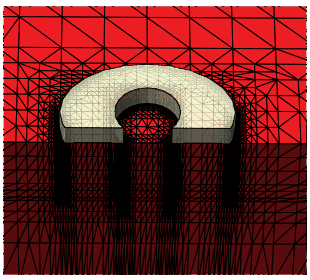


Figure 3: Mask-edge driven refinement: The extruded edges of a mask are used to define a refinement area. For reference, a resist region deposited using the same mask is shown as a transparent body.

Boolean Operations

To make full use of mask-driven refinement it is often necessary to operate on mask shapes. For example to restrict the refinement to a particular area of interest, it may be necessary to AND two or more masks. Similarly, to fully capture the lateral straggle the size of the mask may need to be increased (biasing). Also, it may be useful to eliminate or merge certain small features (under/over or over/under sizing). Sentaurus Process F-2011.09 now supports such Boolean operations on 2-D and 3-D masks.

Create a Mask from a 2-D Region

Modern semiconductor processing techniques such as spacer formation often result in regions of interest which are not directly related to a mask. While it may be possible to derive these regions of interest by applying Boolean operations – for example, biasing and transposing – to the original mask, it is often more precise and user friendly to extract directly the region of interest. As an example, with this release the user can now refine the area under a spacer by first creating an auxiliary mask from the cross-section of a 2-D region and then use this auxiliary mask with the mask-driven mesh refinement. Conversely, it is now also possible to retrieve the coordinates of all segments in a 2-D mask. These features are available in 2-D only.

Range-driven Refinement

Adaptive meshing is a good and user-friendly way to ensure that all doping profiles are adequately resolved at all times. However, in some circumstances a user may want to exert more control over the meshing. For example, a user may wish to minimize the number of times the mesh is recreated in order to speed up the simulations or to reduce interpolation noise. Sentaurus Process F-2011.09 offers support for a more "manual" adaptive meshing strategy. The new utility `RangeRefinebox` allows the user to define with a single command a set of standard refinement boxes. The depth of all of these refinement boxes are defined with respect to a common "range" parameter. The set of refinement boxes can include staggered Russian-doll type refinement boxes, which start off with a tight refinement near the peak of the implant profile and gradually relax the refinement towards the tails. The `RangeRefinebox` utility also supports the new mask-edge-driven refinement and is available for 2-D as well as for 3-D.

To fully leverage this new capability the `implant` command was also enhanced. It is now possible to retrieve all moments for given set of implant conditions, and then, for example, use the primary range and the standard deviation as arguments of the `RangeRefinebox` utility. Figure 4 shows an example of this new capability, which showcases several of the mask-driven meshing enhancements in F-2011.09.

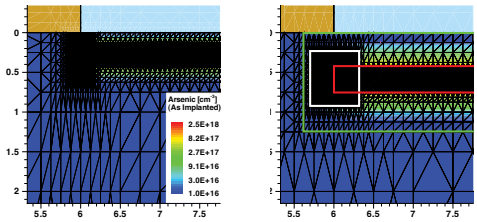
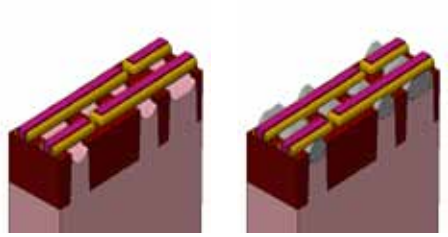


Figure 4: The RangeRefinebox utility allows defining a set of refinement boxes with respect to a "range" parameter. Here, a tight bulk refinement is requested near the depth of the primary range of the implant (red box) and a coarser refinement in the tail area (green box). At the edges of the mask opening a tight mesh resolves the lateral straggle (white box).

Crystallographic Etch and Deposition

A new crystallographic deposition capability and a greatly improved crystallographic etch capability is introduced in Sentaurus Process F-2011.09. To illustrate these capabilities we simulate the formation of sigma-shaped SiGe pockets in a 6T CMOS SRAM cell. In figure 5a shows the geometry after etching the source/drain (S/D) areas of the CMOS transistors. This shape is generated using a single crystallographic etching step with different rates for the different crystallographic orientations. The etch rate of <111> planes is slower than that of the <100> and <110> planes, which is why the <111> planes are exposed as seen in the picture. The tip depth of the sigma etched profile can be created by a simple anisotropic etch. In Figure 5b displays the result of crystallographic deposition. The pockets were generated using a single deposition command. The typical hexagonal shape of the SiGe pockets in Figure 5a arises from the lower rates in the <111> direction.



(a) (b)

Figure 5: Crystallographic etch (a) and crystallographic deposit (b) provide a convenient and physical way to create SiGe source/drain pocket structures. The etch and deposit rates can be set for the following families of directions: <001>, <110>, and <111>.

Levelset Etching Improvements

The Levelset etching capability has been expanded. Improved results can be expected in both 2-D and 3-D for levelset-based etches such as Fourier and Crystallographic. The support for etch beam shadowing has now been expanded into 3-D etching. This calculates etching based on the visibility of the surface to the incoming etch beam. Surfaces shadowed from the etch beam are not etched. In addition, there is now the option to choose a levelset etch calculation even in simpler cases when levelset would not necessarily be used by default.

Line Edge Roughness (LER)

The handling of masks in Sentaurus Process has been expanded to take into account line edge roughness (LER). LER is the result of random variations in photolithography that produce mask edges deviating from straight lines. The roughness along the edge affects device electrical characteristics. These variations can be characterized by how much the mask deviates from the straight edge and by the frequency spectrum of the deviations.

LER in Sentaurus Process allows the user to apply a root-mean-square (RMS) amplitude and a correlation length to a straight mask along an axis direction. It produces randomized results from run to run, always within the envelope of these two parameters.

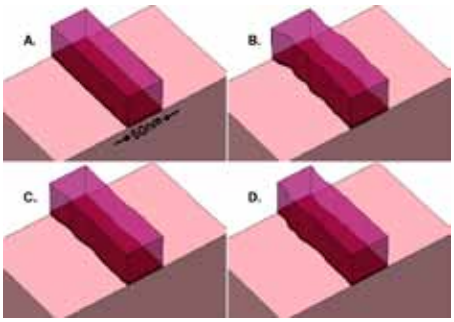


Figure 6: Example of 3D mask with line edge roughness (LER) using different values of amplitude and correlation length. The applied LER is characterized for each case as follows (a) no LER applied, (b) correlation length = 20nm, amplitude = 5nm, (c) correlation length = 20nm, amplitude = 2nm, and (d) correlation length = 12nm, normal amplitude = 2nm.

Sano Smoothing and Sano Adaptive Meshing

Transferring from KMC output to device simulation has been greatly streamlined in Sentaurus Process F-2011.09. Now it is possible to perform the following tasks from within a single Sentaurus Process input file:

1. Apply the Sano method to convert from KMC particles to appropriate finite element fields [1]
2. Select a meshing strategy appropriate for device simulation, including adaptive refinement on smoothed finite element fields such as NetActive
3. Create contacts
4. Save the final TDR file ready for device simulation

Steps 1 through 4 can be performed in 2-D or 3-D, and will normally generate only one call to Sentaurus Mesh, making it efficient and user friendly.

The same implementation of the Sano method in Sentaurus Mesh has been made available in Sentaurus Process. This, coupled with the standard calls to Sentaurus Mesh library for mesh generation, is designed to produce similar (though not identical) high quality results as obtained when performing the Sano smooth and remesh operation in stand-alone Sentaurus Mesh.

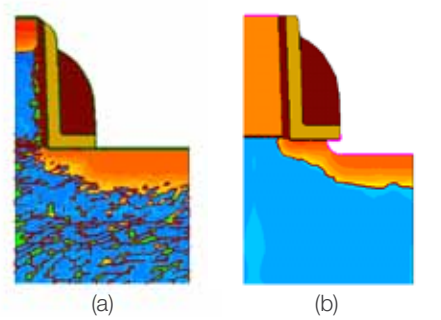


Figure 7: (a) A typical KMC result where the particles have been transferred to the finite element mesh using the default (nearest grid point) method; (b) the same KMC simulation after using Sentaurus Process to prepare the structure for device simulation. The Sano method has been used to obtain a smooth doping profile; the source, drain and gate contacts have been prepared after emulating silicidation with an etch.

MGOALS3D Becomes Default Geometric Engine

Over the past several releases there have been numerous improvements made to the MGOALS3D geometry engine. Customer feedback and internal testing indicate the capabilities and robustness of MGOALS3D greatly surpasses the older PROCEM module in Sentaurus Structure Editor. Accordingly, in this release the default geometry engine is now MGOALS3D.

Sentaurus Topography 3D Interface

A direct interface to Sentaurus Topography 3D has been created to make combined Sentaurus Process/Sentaurus Topography 3D simulations more convenient. Due to US export control regulations, this feature is not available everywhere. Structures are automatically passed to and from Sentaurus Topography 3D, and meshing is delayed until it is necessary. This first version is limited to simple deposition or etching fronts, with the requirement that no thin regions are present in the structure after Sentaurus Topography 3D operations. These limitations will be gradually lifted in future releases.

Shape Library

The shape library provides users with an easy and convenient way to generate common shapes such as STI structures and Sigma shaped SiGe source/drain. The size and location of the shapes are specified in the function call to generate the shape.

Currently, there are six commands available in the shape library: `PolyHedronSTI` creates a shallow trench isolation (STI)-shaped straight section; `PolyHedronSTIaccc` creates a STI concave active corner-shaped polyhedron; `PolyHedronSTIaccv` creates a STI convex active corner-shaped polyhedron; `PolyHedronCylinder` creates a cylinder-shaped polyhedron; `PolygonWaferMask` creates a wafer mask polygon and `PolyHedronEpiDiamond` creates an epitaxial diamond-shaped polyhedron. As new applications come to our attention, the number of shapes offered is expected to grow.

To illustrate, Figure 8 shows three STI shaped polyhedrons, and Figure 9 shows a structure created by combining the three types of STI shaped polyhedrons.

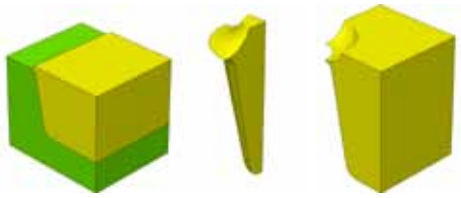


Figure 8: (a) STI-shaped polyhedrons (b) STI concave corner-shaped polyhedrons (c) STI convex corner-shaped polyhedrons

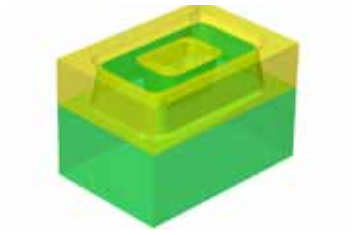


Figure 9: STI structure created by combining three STI-shaped polyhedrons.

Release	Serial, 1 thread	4 thread	8 threads	16 threads
F-2011.09	116h 00m	35h 27m	26h 20m	22h 14m
Speed up	1x	3.25x	4.40x	5.22x

Table 1: Speed-up of 3D 6T SRAM process simulation test case.

Performance Improvements

The simulation of dopant diffusion and mechanical stress in Sentaurus Process involves the solution of many large linear systems produced by the discretization of differential equations. In the case of large 3-D structures and long-duration diffusion, linear solvers might occupy up to 80% of the total time of the diffusion step. The Sentaurus Process F-2011.09 release offers improved parallel iterative solvers for diffusion and mechanics for multi-core computers. The parallel scalability of the new solver algorithm is shown in the table below for the case of an RTP step for a full six-transistor 6T-SRAM cell in three dimensions [2-4]. For dopant diffusion, the three-stream pair diffusion and dopant defect cluster model are used. The mesh contains 981,563 grid points, with 1512 linear systems assembled on this mesh and is solved in the course of a RTP step. Of these, diffusion generated 1345 sparse linear systems with 11.4M unknowns and 202M non-zero entries in the matrix. The remaining 167 linear systems (which were also sparse with 2.83M unknowns and 124.5M non-zero entries) were generated in order to solve for the stress distribution. The benchmark data presented below is for a Nehalem-EX (32 core, 2.66GHz X5650, 256 GB RAM) machine. The table shows the wall-clock time in hours and minutes.

Enhancements in Sentaurus Process Kinetic Monte Carlo (KMC)

Diffusivity in Clusters

The importance of impurity clusters in the activation and deactivation of dopants during annealing is silicon is well established. These impurity clusters, comprising one dopant with vacancies or interstitials (As_nV_m, B_nI_m clusters), or several dopants with vacancies or interstitials ($As_nP_oV_m$), are already modeled by Sentaurus Process KMC. Nevertheless, these clusters have been assumed to be immobile. However, several studies in the literature suggest that the mobility of these clusters cannot be neglected, as in the cases of As_2V and possibly BI_2 [5][6][7]. In particular, reference [5] states that "fast As diffusion at high doping levels is mediated by mobile As_2V complexes".

Starting with Sentaurus Process KMC F-2011.09, a new model to allow diffusion of clusters has been implemented. This model allows simple diffusion for every impurity cluster as:

$$D(cluster) = D_0(cluster) \times \exp\left(-\frac{E_m(cluster)}{k_B T}\right),$$

where the parameters for diffusion, prefactor (D_0) and energy (E_m) are defined as

pdbSet KMC <material> <dopant> Dm_Complex <cluster> <value>

pdbSet KMC <material> <dopant> Em_Complex <cluster> <value>

respectively. For instance, As_2V diffusion could be defined as:

pdbSet KMC Si As Dm_Complex As_2V 1e-1

pdbSet KMC Si As Em_Complex As_2V 2.0

In its current implementation, this model presents some limitations:

- No SiGe, stress/strain or Fermi-level dependencies are included
- Interaction with interfaces are not allowed. Interfaces are treated as "mirrors"
- Interactions with point defects are not fully accounted during cluster migration
- Mirror or periodic boundary conditions are accepted, but "sink" boundary conditions are not

Figure 10 shows different Sentaurus Process KMC simulations with and without As_2V mobility compared with experimental results taken from reference [5]. The improvement obtained by allowing As_2V to diffuse is clear and confirms the necessity of this model.

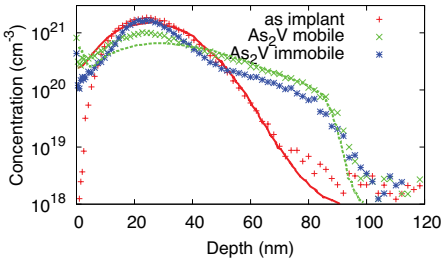


Figure 10: Comparison between experimental results (reference [5]) and KMC simulations of As implanted at 35 keV, dose 5x10^{15} cm^{-2}, annealed at 1030°C for 15 s.

Improved Lattice Kinetic Monte Carlo (LKMC) Model for Epitaxy

Several experimental results are available in the literature regarding the development of facets during selective epitaxial growth of Si and SiGe. In the previous release E-2010.12, the most common facets, {100}, {110} and {111}, could be simulated using a native lattice KMC (LKMC) model. However, {311} facets have also been observed [8]. The formation of {100} terraces in {100} substrates with an off-axis of a few degrees, have also been reported [9].

Sentaurus Process KMC F-2011.09 extends the previous model to account for these new phenomena. The frequency of atoms to attach to the sample is simulated as:

$$v_{SEG}^{LKMC} = K_{SEG}^{LKMC}(site) \times \exp\left(-\frac{E_{SEG}^{LKMC} + \Delta E(site)}{k_B T}\right),$$

K_{SEG}^{LKMC} (site) is a prefactor that accounts for the local microscopic growth for each configuration. This prefactor depends on 2 variables, 'n' and 'm'. 'n' can be 100, 110 or 111 defined similarly to K(1), K(2) and K(3) in the previous model. 'm' is new, and it is used to distinguish between configurations with the same 'n' but different second neighbor coordination numbers. In our model we have split 100 configurations only, into three different ones: 100, 100.7 and 100.8 for 100

configurations with 6 or less, 7, and 8 or more second neighbor coordination numbers.

ΔE(site) is a correction energy applied to special sites. It is a new parameter used to simulate the formation of {311} facets during selective epitaxial growth (SEG). As such, only 1 site is defined to have a non null correction: the {311} local configuration. This configuration occurs in two different situations: (a) a (100) generic site that lacks half of its third neighbors and (b) a (110) site where the second atom in the chain needed to define the place as 110 would have first coordination number equal to 2. Assigning a slower rate to configuration (a) prevents the {311} facet from becoming a {111} facet. The slower rate for configuration (b) assures that the local {311} configuration is not broken by lateral (110) regrowth. The presence of this activation energy can be understood as the energy needed to break the bonds created by surface reconstruction in free Si interfaces.

In contrast with E-2010.12, where the parameters for SEG and solid-phase epitaxial regrowth (SPER) where shared, in F-2011.09 the parameters needed for this model are defined in the parameter database under KMC Si Epitaxy and are not shared with SPER parameters. The parameters for the site prefactors are:

prefactor.SEG.100.8	For (100) sites with 8 or more second neighbor coordination number
prefactor.SEG.100.7	For (100) sites with 7 second neighbor coordination number
prefactor.SEG.100	For (100) sites with 6 or less second neighbor coordination number
prefactor.SEG.110	For (110) sites
prefactor.SEG.111	For (111) sites

And for the activation energies:

energy.SEG	Overall activation energy for SEG
energy.SEG.311	Correction for 311 planar SEG

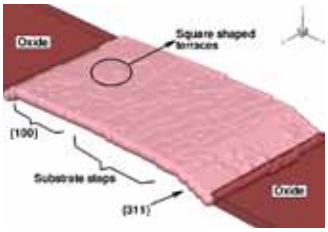


Figure 11: Monolayers grown on a {100} substrate with a 4° miscut angle

Figure 11 shows a detailed 3-D view of a strip of Si(100) surface with a 4° degree miscut limited by SiO_2 strips after a few monolayers have been epitaxially grown. The formation of initial {311} facets can be seen on both sides. The flat surface is starting to show the formation of terraces with square shaped islands on top of them. The original substrate steps formed by the miscut structure can also be seen, although they have been overridden by the perfect {100} terrace formation on the left.

Sink Boundary Conditions.

New sink boundary conditions have been included for the y and z cell boundaries. These new conditions are similar to sinkProbBottom and are called: sinkProbLeft and sinkProbRight for y and sinkProbFront and sinkProbBack for z.

SiGe Bandgap Narrowing Interpolation

When Ge is present, bandgap narrowing is computed as a linear interpolation between the narrowing produced by strain for purẽ Si ΔE_{gs}^{Si}, and the narrowing for pure Ge ΔE_{gs}^{Ge} This way, the total narrowing for $Si_{1-x}Ge_x$ is

$$\Delta E_{gs} = \Delta E_{gs}^{Si} + x(\Delta E_{gs}^{Ge} - \Delta E_{gs}^{Ge})$$

where x is the relative Ge concentration specified in $Si_{1-x}Ge_x$. The parameters used for pure Ge are similar to the ones for pure Si, but with the "Ge." prefix.

Sentaurus Device

The F-2011.09 release of Sentaurus Device adds significant new capabilities to address the many applications Sentaurus Device has acquired over the years. The 'More Moore' applications are targeted with a new stress- and orientation-dependent hole model, the application of the Impedance Field Method (IFM) to variability analysis, and a novel method for solving the Boltzmann Equation (BE) deterministically, whereas the 'More than Moore' applications are covered with new models for widebandgap materials and optoelectronic devices. The new BE deterministic solver is a research-oriented capability which complements the traditional Monte Carlo (MC) method of solving the BE.

Low-Field Hole Mobility Model for Stress and Surface/Channel Orientation

A new low-field channel mobility model for holes has been developed which accounts for strain and orientation effects on the hole band structure, scattering processes, and quantization. The total mobility tensor is constructed from the heavy, light, and split-off bands by explicitly modeling the quantized carrier density-of-states (DOS) in the channel, the group velocities, and the microscopic momentum relaxation time (MRT). Hole quantization effects are modeled by the 6-band **k·p** MLDA model [11] and the group velocities are computed by averaging over the 6-band **k·p** band structure. It is important to note that such averaging breaks the bulk symmetry of the velocity product in the mobility calculation and brings anisotropy to the channel mobility for the (110) surface, while the mobility for (100) remains isotropic. The hole MRT is based on standard bulk scattering expressions, but modifies them to account for quantization in the channel via the position-dependent DOS from the 6-band **k·p** MLDA model. This modification also introduces implicit electric field dependence to the scattering model.

The new model computes an anisotropic correction to the macroscopic TCAD mobility. This correction is defined as the ratio of the total valence band hole mobility tensor for the actual strain/surface configuration to the total hole mobility along the channel direction of some reference MOSFET configuration, for instance relaxed (100)/<110>.

The validity of the mobility model was checked in both stressed and relaxed conditions; several major surface/channel orientations were considered. Figure 12 shows the normal electric field dependence of the new hole mobility for various substrate and channel orientations together with experimental data. There is good agreement with experimental data for high electric field and relatively good agreement for moderate fields. Also the model correctly captures the very different effective field dependence of (100) and (110) substrate orientations. Figure 13 shows stress-related hole mobility enhancements computed according to the new model and compares them to Kubo-Greenwood mobility calculations based on 6-band **k·p** subbands [12] and to MC data [13] for (100) and (110) substrate orientations.

These comparisons confirm that the model is capable of giving predictive results for stress and orientations effects. Calculating a correction factor rather than an absolute mobility allows retaining previously calibrated TCAD macroscopic models and still obtaining a correct stress and orientation response. On the other hand, there will be some impact on computation time: to compute the carrier density and mobility the model needs to perform multiple numerical integrations over the energy. Though minor when compared with full subband-based mobility calculation, the computational cost of the new model is still considerably higher than that of conventional TCAD mobility models.

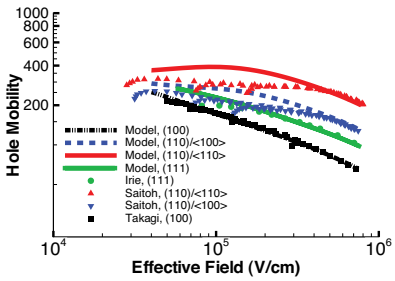


Figure 12: Comparison of measured mobility with the new model computed as a correction to (100) MOSFET mobility in the absence of stress for four surface/channel configurations: (100)/<110>, (110)/<100>, (110)/<110>, (111)/<110>.

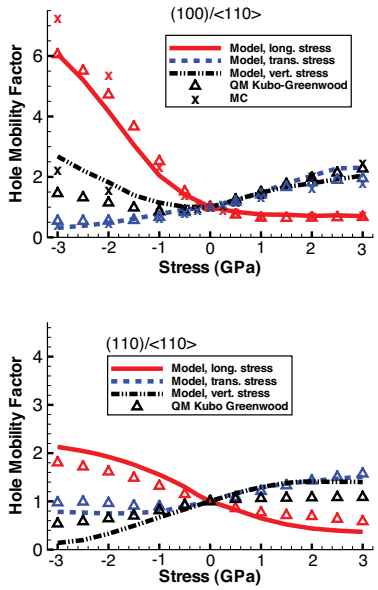


Figure 13: Comparison of stress-related hole channel mobility enhancement computed by the new model with QM Kubo-Greenwood calculations and MC results for (100) and (110) substrate orientations.

Deterministic Boltzmann Equation Solver

Introduction

With the continued scaling in device dimensions, quasi-ballistic transport becomes increasingly important and conventional macroscopic transport models such as the drift-diffusion (DD) and hydrodynamic models become less predictive and require more calibration. For example, the DD model tends to overestimate linear currents [15] while underestimating saturation currents. In addition, the macroscopic transport models do not solve for microscopic carrier distribution function which is needed for the physics-based modeling of hot carrier injection and device degradation.

To overcome the limitations of the macroscopic transport models, Sentaurus Device F-2011.09 now provides a deterministic Boltzmann equation (BE) solver [16] based on the high-order spherical harmonics expansion (SHE) method [17]-[19]. The BE is a balance equation for the microscopic carrier distribution function defined in the phase space which includes the wave vector as well as the spatial coordinate. As the phase space has a large degree-of-freedom, the Monte-Carlo (MC) method has been widely used to solve the BE, and a MC-based BE solver is available as part of Sentaurus tools suite [20]. While the MC method randomly samples the phase-space trajectory to solve the BE, the SHE method reduces the phase space dimension by expanding the distribution function and the BE with spherical harmonics up to a certain order with an appropriate coordinate transform. The resulting system of equations is solved deterministically to obtain the distribution function. Obviously, the number of unknowns obtained after the discretization of the BE is much larger than those of the macroscopic transport models. The number of unknowns in the deterministic BE solver is proportional to the number of mesh points, the number of required energy intervals, the number of considered band-valleys, and the number of spherical harmonics used in the expansion. Therefore, the deterministic approach typically requires considerable computational resources. On the other hand, it can provide a fully converged self-consistent solution which is not affected by stochastic noise as in the case of MC methods.

Typically the deterministic BE solver requires only a few Newton iterations to obtain a sufficiently converged solution because it employs the coupled Newton scheme with quadratic convergence.

In order to solve the BE, the band-structure and scattering models are needed. The deterministic BE solver provides various band-structure and scattering models. Among the available band-structure models, the multi-valley band model for electrons and the anisotropic band model for holes can capture stress and orientation dependences as well as the full-band-structure-related effects. The supported microscopic scattering models include phonon scattering, ionized impurity scattering, impact ionization, and surface roughness scattering. Each scattering model provides variable options

and adjustable model parameters. In order to ensure consistency between the macroscopic transport model and the BE, the strength of the impurity scattering and the surface roughness scattering at each position can be automatically adjusted to reproduce the macroscopic low-field mobility specified in the Physics section. In addition, generation-recombination processes and a quantum correction based on the modified local-density approximation model [21] can be taken into account.

Simulation Example

For hot carrier injection, the first-order SHE method without the self-consistent potential can provide reasonable results. As the application of the first-order SHE method to the hot carrier injection problem was already introduced in Sentaurus Device C-2009.06 and discussed in [22], here we focus on the self-consistent simulation of the Poisson and BE in order to study quasi-ballistic transport in short-channel MOSFETs. We compare simulation results obtained from the BE solver and from the DD model for bulk MOSFETs with gate lengths from 80 nm to 250 nm as shown in Figure 14. The spherical harmonics up to order 3 and 7 are used for electrons and holes, respectively. The device structures as well as simulation conditions are similar to those reported in [23] which compares the DD model with the solution of the BE obtained from the Monte Carlo method. To be consistent with [23], quantum effects are not taken into account. Typical CPU time to obtain one bias point is about 40 min for the nMOSFET and 140 min for the pMOSFET, respectively. With the DD simulation result as an initial guess, each bias point can be efficiently obtained in parallel within the Sentaurus Workbench (SWB).

Figure 15 shows I_D-V_G curves of the 80 nm MOSFETs. The BE and DD give similar subthreshold currents as the subthreshold characteristics are mainly determined by the electrostatics. Note that the deterministic BE solver can compute the subthreshold currents without problems as it does not involve stochastic noise unavoidable in the Monte Carlo method. Figure 16 shows I_D-V_D curves of the 80 and 250 nm MOSFETs. Even though the scattering rate of the BE solver is consistent with the low-field mobility of the DD model, the linear currents from the BE are slightly smaller than the linear currents from the DD model because of the built-in electric field [15], especially for the nMOSFETs. In addition, the BE gives larger saturation currents than the DD model because of the velocity overshoot effects. Figure 17 shows the on-current (I_D at V_G=V_D=±1.5 V) as a function of the gate length, which clearly shows that the on-current differences increase with decreasing gate length. Figure 18 shows the average electron velocity and electron sheet density along the channel of the 80 nm nMOSFET for V_D=V_G=1.5 V. Although the BE gives about two times larger peak velocity compared with the saturation velocity, the actual enhancement of the on-current is about 30% as the BE also gives smaller electron density in the channel. In fact, the enhancement of the on-current is proportional to the velocity enhancement at the beginning of the channel because the two models give similar electron density at the beginning of the channel. Figure 19 shows the microscopic electron energy distribution functions as a function of the total energy at different channel positions. The quasi-ballistic transport gives the pronounced tail distribution at the drain side of the channel (at x=40nm), which cannot be characterized by the macroscopic variables such as the electron density and energy. Note that such a tail distribution can be responsible for hot carrier degradation and hot carrier injection.

The present deterministic BE solver based on the high-order SHE method is a useful tool for studying quasi-ballistic transport in nanoscale MOSFETs as well as various reliability issues which requires information about the microscopic carrier distribution function.

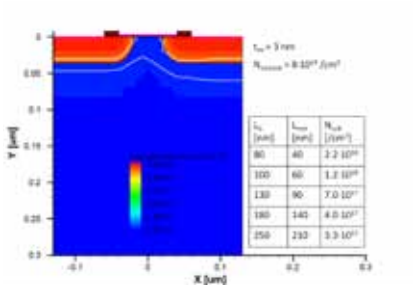


Figure 14: Simulated 80 nm MOSFET structure.

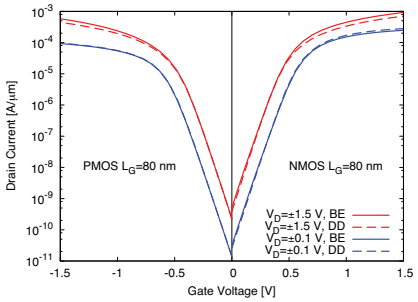


Figure 15: Simulated I_D-V_G curves of the 80 nm MOSFETs for $|V_D|$ = 0.1 and 1.5 V.

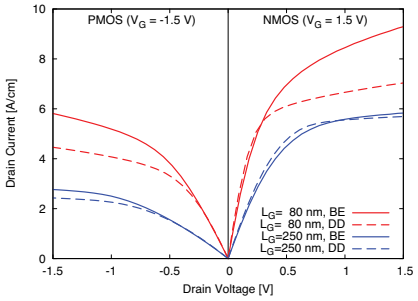


Figure 16: Simulated I_D-V_D curves of the 80 and 250 nm MOSFETs for $|V_G|$ = 1.5 V.

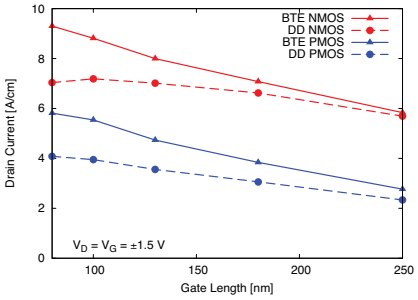


Figure 17: Simulated on-current (I_D at V_G = V_D = ±1.5 V) as a function of the gate length.

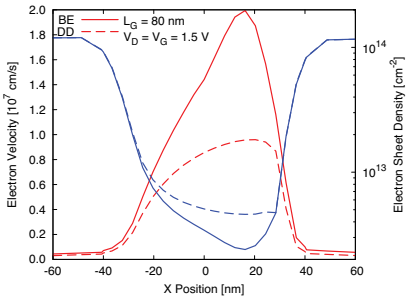


Figure 18: Average electron velocity and electron sheet density along the channel of the 80 nm nMOSFET for $V_D = V_G = 1.5$ V.

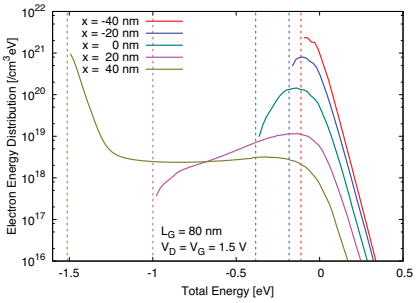


Figure 19: Electron energy distribution functions as a function of the total energy (kinetic energy + potential energy) at different x positions along the Si/SiO_2 interface (y = 0 nm) of the 80 nm nMOSFET for $V_D = V_G = 1.5$ V from the source (x = - 40nm) to the drain (x = 40nm). The dotted line represents the potential energy at each position.

Metal Workfunction Variability

Sentaurus Device now allows the workfunction in metal regions to have a positional dependency. This can be used, for example, to account for local workfunction variations in metal gates used in scaled technologies.

Specifying the positional dependency of metal workfunction can be accomplished in two ways. In one method, the workfunction is specified as a mole-fraction dependent parameter for the metal, if the metal is treated as mole-fraction dependent material. This could be used, for example, to modify the workfunction in metal gates based on the composition of one of the constituent elements, such as aluminum in TiAlN.

The second method allows the positional dependency of the workfunction in the metal to be specified directly in the Sentaurus Device command file, or alternatively through a physical model interface (PMI) model written by the user. The PMI capability is especially powerful since it enables the user to provide a detailed description of the workfunction in metal regions.

One possible application of this capability is to use a PMI model to provide a grain-level description of metal gate workfunction. This is useful for analyzing the device-to-device variations of threshold voltage due to the random distribution of grains in metal gates. Depending on processing conditions, metal grains can range from a few to several nanometers in size. Due to the small gate size in advanced technologies, this means that the gate will consist of a relatively small number of grains. In addition, these grains may vary in size, shape, and orientation. It is important to note that the workfunction of each grain depends on its orientation, giving rise to a metal gate with a spatially varying workfunction. Device-to-device variations of gate grains will result in device-to-device variations of effective workfunction and device threshold voltage.

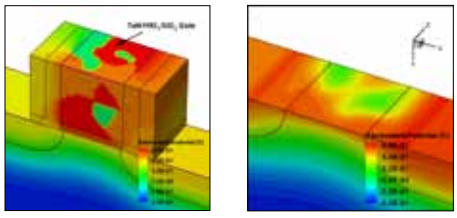


Figure 20: Device structure and electrostatic potential in a L/W = 16 nm/16 nm device utilizing a $TaN/HfO_2/SiO_2$ gate stack with an average metal grain size of 4 nm.

As an example, a PMI model has been written to account for the random variation of metal grains in a L/W = 16 nm/16 nm n-channel MOSFET. The simulated structure utilizes a $TaN/HfO_2/SiO_2$ gate stack with an effective oxide thickness of 8 nm. The metal gate is treated as a $(16\text{ nm})^3$ conductor region. The PMI will assign the workfunction in this region based on a random distribution of grains with a specified average grain size. The workfunction for each grain will take on one of three possible values based on probabilities for TaN given in [24] (wf_1=4.0 eV, P_1=0.50; wf_2=4.15 eV, P_2=0.30; wf_3=4.8 eV, P_3=0.20). Figure 20 shows the electrostatic potential in the gate resulting from the varying workfunction for one possible configuration of grains with an average size of 4 nm.

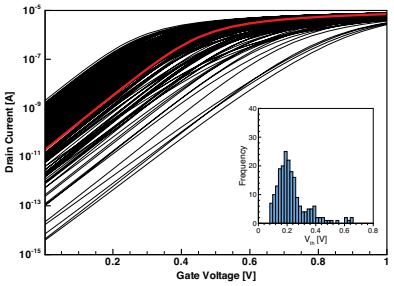


Figure 21: I_d-V_g curves from 200 simulations of a device with randomized grains of average grain size of 4 nm. The red curve is for a device with a fixed workfunction of 4.205 V. The inset shows the corresponding threshold voltage distribution.

Since the distribution of grains is a random consequence of the process conditions, the threshold voltage may vary from device to device. To study such variations, 200 simulations of I_d-V_g characteristics were performed for a device where the average grain size was assumed to be 4 nm. For the $(16\text{ nm})^3$ gate considered here, on the average, each gate cross-section will have only about 16 grains. The results are shown in Figure 21. The large observed spread in the I_d-V_g curves, and in the threshold voltage distribution shown in the inset, is due to the combination of a small number of grains and the spread of possible workfunction values (from 4.0 to 4.8 eV). The red curve shows the result from a simulation with a fixed workfunction value of 4.205 (obtained from $wf_1*P_1 + wf_2*P_2 + wf_3*P_3$).

Figure 22 shows cross-sections of the randomly oriented grains (with average grain size = 4 nm) at the metal/HfO_2 interface for two different cases, and the corresponding electrostatic potential at the silicon/oxide interface when V_g = 0.24 V. The left plot show a case which resulted in a V_{th} close

to the average. The right plot show a case that resulted in a V_{th} well above average. In the left plot, the distribution of wf_1=4.0 eV grains along the Z=0 border have resulted in an electrostatic potential that is favorable to electron flow through the channel. In contrast, the grain distribution in the right plot shows wf_3=4.8 eV grains spreading across the entire channel, creating a potential barrier for electron flow and resulting in a larger threshold voltage.

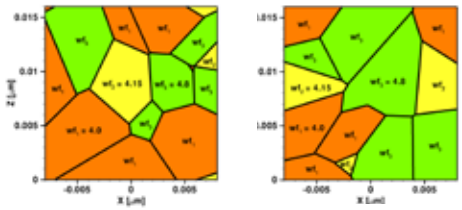


Figure 22: Metal grain cross-section at the metal/HfO_2 interface and corresponding electrostatic potential at the silicon/oxide interface for two cases with an average grain size of 4 nm.

It is instructive to repeat the analysis, but with a smaller average grain size. Figure 23 shows the results of another 200 I_d-V_g simulations, but this time with an average grain size of 2 nm. In this case, the spread of the results has been reduced considerably compared to Figure 21.

This is because the smaller average grain size results in an increased number of favorable potential paths through the channel, and statistically this results in devices that behave closer to average.

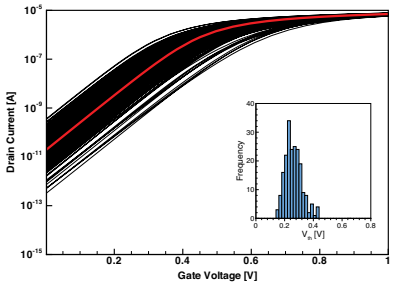


Figure 23: I_d-V_g curves from 200 simulations of a device with randomized grains of average grain size of 2 nm. The red curve is for a device with a fixed workfunction of 4.205 V. The inset shows the corresponding threshold voltage distribution.

Note: Please contact TCAD Support to obtain the PMI module discussed in this section.

Variability Analysis with Impedance Field Method

Scaling in advanced logic and memory devices has reached a state where process-induced electrical variability must be considered as an integral part of process optimization and device design. The process variation—the statistical location of discrete dopants in the silicon lattice, geometrical fluctuations along material boundaries, spatially inhomogeneous gate metallization, etc.—is well modeled by TCAD and its impact, the electrical characteristics of devices and circuits, is conducive to simulation.

A common approach for TCAD-based variability analysis is the so-called "atomistic method" whereby many direct simulations of devices with individually randomized doping profiles and other process effects are carried out, with the electrical output analyzed statistically. While this method is intuitively easy to grasp, it has the drawback of requiring significant computational effort to accumulate the necessary statistics. With the "atomistic method" even single transistor variability analysis may require multiple days of CPU time. A computationally efficient alternative is the impedance field method (IFM) which relies on a single simulation of a continuum device and computes the electrical variability as a linear response to fluctuation noise sources.

Description of IFM Method

In the impedance field or Green's function method the local fluctuation is treated like a noise source and the fluctuation of the terminal electrical characteristics is calculated based on this noise source. The method incorporates noise sources due to doping, interface geometry, and metal workfunction (see associated section in this newsletter), and is in principle extensible to other fluctuations. The underlying assumption is that the response of the contact voltage to local fluctuations is linear. For each contact, Green's functions are computed that describe this linear relationship. The calculation of the noise influence on the terminal characteristics is purely numeric, as the Green's functions are completely specified by the transport model. Green's function G and noise source K together give the correlation of the variations of the terminal characteristics via:

$$\langle \delta V_k \delta V_l \rangle = \int_S d^2 r_1 d^2 r_2 \cdot G_k(\mathbf{r}_1) \cdot K(\mathbf{r}_1, \mathbf{r}_2) \cdot G_l(\mathbf{r}_2)$$

As an illustration, the correlation coefficients for doping and interface geometry are described by the following equations:

Geometrical noise :

$$K = \mathbf{n}(\mathbf{r}_1) \cdot \mathbf{n}(\mathbf{r}_2) \cdot \left[a_{iso} + |\mathbf{n}(\mathbf{r}_1) \cdot \mathbf{a}(\mathbf{r}_1)|\right] \cdot \left[a_{iso} + |\mathbf{n}(\mathbf{r}_2) \cdot \mathbf{a}(\mathbf{r}_2)|\right] \cdot e^{\frac{(\mathbf{r}_2 - \mathbf{r}_1)^2}{\lambda^2}}$$

RDD:

$$K = \mathbf{N}(\mathbf{r}_1) \cdot \delta(\mathbf{r}_1 - \mathbf{r}_2)$$

where $n(r_1)$ is the normal at r_1, $\delta s(r_1)$ is the displacement of the interface at r_1, λ is the correlation length, and N is the doping concentration. Vectors are drawn in bold.

The geometrical correlation coefficient defines the probability with which a certain perturbation of the geometry at two different points occurs at an interface. Reducing the correlation length λ results finally in the uncorrelated case. Increasing this parameter to a value much larger than the device dimensions gives a simple shift of the whole interface.

The IFM computes the variability in a single calculation and has the added advantage of greatly reducing mesh noise since it uses a single numerical mesh.

The IFM has been shown to produce similar results to the "atomistic" method. Table 2 shows a comparison of standard deviations for $V_t$lin, $V_t$sat and Ion simulated with the "atomistic" and IFM methods for a 3D NMOS transistor typical of 32nm technology. The data for the "atomistic" methods has been obtained by performing 200 I-V simulations of individually randomized instances of the 3D NMOS transistor and averaging the results. For IFM, a single I-V sweep of the original continuum device structure is sufficient.

	"Atomistic"	IFM
σ V_t (lin)	23.8 mV	23.5 mV
σ V_t (sat)	27.5 mV	27.2 mV
σ I_{on}	6.63x10^{-6} A	6.33x10^{-6} A

Table 2: Comparison of variability results obtained from IFM and "atomistic" method.

Yet the IFM analysis was completed in 4 hours of CPU time in a single simulation whereas the "atomistic" method required 200 simulations and 400 hours of CPU time, representing about a 100X improvement in simulation efficiency for the IFM.

Extension to Statistical Impedance Field Method

The F-2011.09 release also features the possibility to simulate the linear response of a set of on-the-fly randomized realizations of a device structure. This approach combines the speed and accuracy of the IFM with the ability to reconstruct the I-V curves of individual randomized realizations of a device structure. The statistical Impedance Field Method is particularly attractive for applications for which the standard deviation of currents and voltages are not sufficient. An example of such an application is the static noise margin variability in SRAM cells.

Sensitivity Analysis

Usually, device parameters, such as parameters which define the mobility model, are calibrated by running multiple simulations with different (mobility) parameters. Then the resulting terminal currents are compared to measurements, and accordingly adjustments are made to the (mobility) parameters. Typically, this procedure must be repeated several times to arrive at a calibrated set of (mobility) parameters. In the following we'll refer to this approach as the "direct method".

A disadvantage of the "direct method" is that it becomes successively more difficult to manage as the number of parameters increases. Also, some combination of parameters may result in degraded convergence or even simulation failure resulting in a noisy or even incomplete data set.

In release F-2011.09, Sentaurus Device introduces a new feature to simplify calibration of parameters. The feature, called sensitivity analysis, is based on the impedance field method (IFM).

Within this approach Sentaurus Device first computes the solution of the reference device. Based on this solution it computes the linear response to a change of a user-selected set of parameters via the impedance field. As a result, it predicts how a change in a given parameter affects the observed terminal currents.

This approach guarantees that all requested data points are available for subsequent analysis since no re-computing of solutions is needed.

Furthermore, sensitivity analysis computes the impedance fields only once. The same impedance fields can be used to compute the linear response for all parameters. Therefore, sensitivity analysis is much faster than the direct method. In particular, the total run time for the direct method is proportional to the number of varied parameters, while for the sensitivity analysis the computation of additional parameter variations is very fast once the impedance fields are calculated.

In conclusion, sensitivity analysis addresses the two main issues of the direct method: large computation time and numeric robustness. It therefore is a powerful tool to keep up with the increased variety in modern device technology.

New Models for the Simulation of III-Nitride Devices

While silicon power devices are dominant in today's power electronics, and will continue to evolve, more and more III-nitrides, notably GaN, AlGaN, and InGaN, long viewed as promising semiconductors for high-power, high-temperature applications are gaining traction in applications beyond the performance envelope of silicon. These wide bandgap semiconductors enable lower on-resistance than silicon at a given breakdown voltage, a key figure of merit in power switching applications. Moreover, the low intrinsic carrier concentration resulting from the large energy gap also allows device operation at higher junction temperatures, which simplify heat sink design and cooling systems, with potential benefits in cost savings, form factor and weight.

The new F-2011.09 release of Sentaurus Device introduces a number of new models that are applicable to the simulation of III-Nitride devices.

New Expression for Polarization Model

The "strain" polarization model in Sentaurus Device computes the polarization component along the c-axis, P_Z, based on the material and mole fraction information at each mesh point. A new expression based on the work by Ambacher et. al. [25] was implemented in the latest release:

$$\mathrm{P} = P_Z = \mathrm{P}_{Z_{SP}} + 2\frac{a_0 - a}{a}(1 - relax)\left(\mathrm{e}_{31} - \mathrm{e}_{33}\frac{\mathrm{c}_{13}}{\mathrm{c}_{33}}\right) \quad (1)$$

where Pz_{SP} is the spontaneous polarization component, a_0 and a are the lattice constants of strained and relaxed materials, respectively, e_{ij} are piezoelectric coefficients, c_{ij} stiffness constants, and relax accounts for a possible strain relaxation. All model parameters are mole fraction dependent and, by default, linear interpolation is applied for ternaries based on their binary side materials.

This expression is equivalent to the previously existing expression in Sentaurus Device and the primary difference is the use of *e* instead of *d* piezoelectric coefficients. Both expressions produce identical results, provided **e** and *d* piezoelectric coefficients are equivalent.

Gate Polarization

Sentaurus Device F-2011.09 also introduces a new option to account for a modification to expression (1) proposed by Ashok et. al. [26]. Starting from the same simplifying assumptions, they account for the converse piezoelectric effect while computing the c-axis strain component, which leads to the addition

of an electric field dependent strained AlGaN polarization:

$$P = P_{Z_{CP}} = P_{Z_{SP}} + 2\frac{a_0 - a}{a}(1 - relax)\left(e_{31} - e_{33}\frac{c_{13}}{c_{33}}\right) + \frac{e_{33}^2}{c_{33}}F_Z = P_Z + \frac{e_{33}^2}{c_{33}}F_Z \quad (2)$$

Since F_Z is typically antiparallel to the polarization direction in AlGaN barrier layers, the main effect of the converse piezoelectricity is to reduce the overall polarization magnitude of the barrier layer, consequently decreasing the electron density in the channel.

While solving Poisson equation with this new option turned on, the term that contains the electric field F_Z is moved to the left-hand side and combined with the dielectric tensor so that the dielectric component along c is increased by e_{33}^2/c_{33}

$$\nabla\left\{\begin{bmatrix}\epsilon_a & 0 & 0\\ 0 & \epsilon_a & 0\\ 0 & 0 & \epsilon_c + \frac{e_{33}^2}{c_{33}}\end{bmatrix}\nabla\varphi\right\} = -\rho + \nabla\begin{bmatrix}0\\0\\P_Z\end{bmatrix} \quad (3)$$

Arbitrary Direction for Anisotropy

Since III-nitride semiconductors in Wurtzite crystals are transverse isotropic, their in-plane properties and the corresponding components parallel to the c axis are different. In particular, anisotropy in dielectric constants plays a first order role in the electrostatics of HFET devices and hence in their I-V characteristics. III-nitrides typically exhibit higher dielectric constant along the c axis, $\in_c$, compared to in-plane components, $\in_a$. The electric field around heterointerfaces is such that the higher dielectric constant leads to a reduction in magnitude of total polarization in the material with larger spontaneous and piezoelectric components, e.g. AlGaN, and increases it in the material with lower overall polarization, e.g. GaN. As a consequence, the channel 2-D electron density is lower when simulated using anisotropy compared to the simpler isotropic approach.

The release F-2011.09 of Sentaurus Device allows for arbitrary directions in the anisotropy of model parameters such as dielectric constants, which makes it possible to align it to the polarization direction as in III-nitride Wurtzite crystals. Figure 24 compares I_{DS} vs. V_{GS} curves simulated with isotropic dielectric constant, a dielectric tensor with the c-axis component increased by e_{33}^2/c_{33} to account for the converse piezoelectricity in the barrier layer and a case with an anisotropic dielectric tensor. The figure in the inset depicts the structure used for simulations.

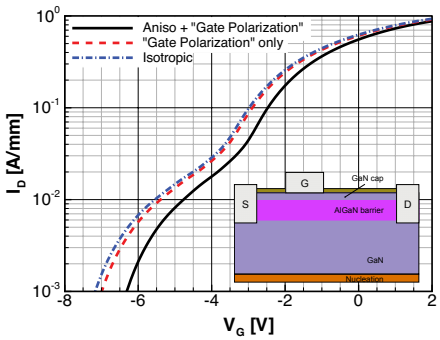


Figure 24: I_D vs. V_G curves comparing results from simulations including isotropic dielectric constant (dash-dotted line, blue), converse piezoelectricity under the gate (dashed, red), and converse piezoelectricity under the gate plus an anisotropic dielectric tensor (solid, black)

Activation of Charge Due to Polarization

When using the built-in polarization models in Sentaurus Device, the interface charge at the barrier/channel interface is automatically computed via the divergence of the polarization fields. Other heterointerfaces where significant polarization divergence is observed would also exhibit strong polarization charges. However, these charges at interfaces below the GaN buffer layer are likely to be compensated by charged defects and are frequently irrelevant to the simulation of the DC behavior of devices. Sentaurus Device F-2011.09 provides a switch named `activation` that allows the scaling of the polarization charge at any of the interfaces. Therefore, the setup may be simplified by simply setting a null activation for the lower, irrelevant interfaces.

Converse Piezoelectricity

Converse piezoelectricity has been associated with degradation of GaN based HFETs [27]. High electric fields that develop near the drain side of the gate lead to strain relaxation through the formation of mechanical defects and consequently to the generation of electrical traps. When negatively charged, these traps reduce drive currents, shift V_T positively, and increase the drain access resistance. Simulations of the operation of these devices under stress conditions with Sentaurus Device F-2011.09 allow for the visualization of the spatial distribution of converse piezoelectric fields, as illustrated in Figure 25, and provide an important tool to optimize the device design to mitigate these deleterious effects.

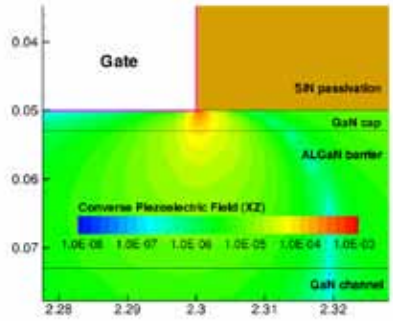


Figure 25: Contour map of the XZ shear converse piezoelectric field component near the gate edge in the drain side caused by large electric field parallel to the device channel. V_G = -4V, V_D = 28 V applied to the same structure as in the inset of Figure 24.

Improved Avalanche Model for Silicon Carbide

Power devices based on 4H silicon carbide (4H-SiC) can provide unique advantages such as high breakdown voltage and high temperature operation. Due to its hexagonal crystal structure 4H-SiC exhibits different physical properties along the 0001 axis compared to the $11\bar{2}0$ plane. This anisotropy requires special models for device simulation.

Starting with the F-2011.09 release, Sentaurus Device offers a new anisotropic avalanche model proposed by T. Hatakeyama [28] which

has been specifically calibrated to model the breakdown voltage in 4H-SiC devices. It is based on the well-known Chynoweth law [29]:

$$\alpha = a_e e^{-\frac{b_e}{F}} \qquad \beta = a_h e^{-\frac{b_h}{F}}$$

where α and β denote the impact ionization coefficients for electrons and holes, respectively.

The Hatakeyama avalanche model focuses on the computation of the impact ionization parameters for an arbitrary direction of the driving force $\vec{F}$. Along the anisotropic 0001 axis, the anisotropic values of the parameters a_e, b_e (electrons) and a_h, b_h (holes) must be selected. Similarly, within the isotropic plane ($11\bar{2}0$ direction) the isotropic values for the parameters a_e, b_e and a_h, b_h must be selected. For an arbitrary intermediate direction, the Hatakeyama avalanche model interpolates all parameters simultaneously based on physical arguments.

In contrast to this, the existing anisotropic avalanche models in Sentaurus Device (van Overstraeten-de Man and Okuto-Crowell) interpolate each model parameter individually based on the direction of the current. For this reason the Hatakeyama avalanche model is expected to provide more predictive results for arbitrary directions.

The Hatakeyama avalanche model supports all the standard driving forces in Sentaurus Device, including:

- Gradient of the quasi-Fermi potential
- Electric field parallel to the current
- Straight electric field
- Carrier temperature driving force for hydrodynamic simulations

Figures 26 and 27 show, respectively, the structure of an n-type trench 4H-SiC IGBT and its breakdown characteristics as a function of crystal orientations. The IGBT has a long (260µm) and lightly doped ($10^{14}cm^{-3}$) drift region. As a result, the breakdown voltage is more than 20kV when the channel is along the 0001 axis. The simulations show that the Hatakeyama model gives the same results as the existing model when the structure is axis aligned and predicts different breakdown voltages in other orientations due to its more physical approach.

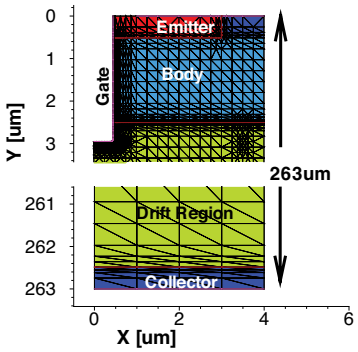


Figure 26: Structure of the n-type 4H-SiC IGBT used in the simulation. The middle part of the drift region is truncated for clarity.

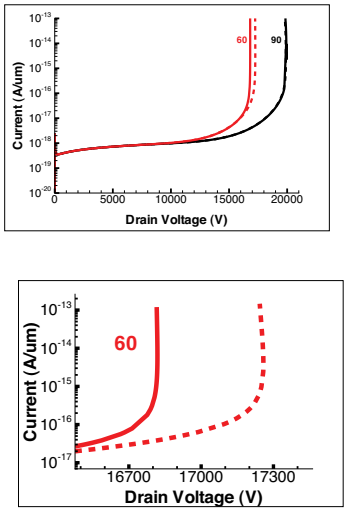


Figure 27: Breakdown characteristics of the n-type 4H-SiC IGBT built at different crystal orientation (60 and 90 degrees from $11\bar{2}0$ direction) using Hatakeyma model (solid lines) compared to Okuto model (dash lines).

Optoelectronic Enhancements

New physical models have been introduced in the optoelectronics framework of Sentaurus Device to strengthen the modeling capabilities for solar cells and CMOS image sensors.

A simple photon absorption heat model has been added so that interband and intraband absorption of photons can be translated partially to heat production processes. Thereafter, these heat sources are entered into the lattice heat equation. This model is implemented under the unified optical generation interface. Another new feature under this interface is the automatic interpolation of optical generation profiles that have previously been computed on a different grid or another wavelength. The different optical generation profiles can be imported into the interface seamlessly. This enables the user to simulate combined electrical transport effects caused by spectrally distributed light in solar cells and CMOS image sensors. Physical modeling of free carrier absorption is enabled via the complex refractive index library.

A Fresnel type boundary condition has been added in the Sentaurus Device raytracer. This acts as a default boundary condition that can unset other types of boundary conditions as a complementary set. Implemented diffusive surface boundary conditions include the Phong, Lambert, Gaussian and random scattering models. Plotting of the interface flux is now possible with the raytracer through the unified optical generation interface, and the user will be able to retrieve the reflected, transmitted and absorbed photon fluxes at any interface of the device.

Various new functionalities have been introduced in EMWplus. It is now possible to extract fields in extraction domains that intersecting a number of different regions. Truncated plane wave and Gaussian excitation sources have been implemented to provide a localized field source. A material can now be defined as PEC or PMC so that the appropriate electric or magnetic fields will be set to zero within the material.

Sentaurus Device Monte Carlo

Single-Particle Monte Carlo

Device Monte Carlo enables the simulation of quasi-ballistic transport which occurs in highly scaled CMOS devices as well as the treatment of band structure-related effects such as the impact of strain and device orientation on performance. There are two main approaches to Device Monte Carlo:

ensemble Monte Carlo and single-particle Monte Carlo. With the F-2011.09 release, exclusive development focus has now been placed on the single-particle approach. The single-particle approach provides a number of algorithmic and practical advantages, including the ability to handle unstructured meshes and high doping with improved stability [30]. As an example, Figure 28 shows the result of a single-particle Monte Carlo simulation on a 20nm gate-length nMOSFET with a non-planar geometry and unstructured mesh. A plot of the mean electron energy is shown. This capability allows device Monte Carlo to be used on the same device structures and same meshes that are used for conventional drift-diffusion and hydrodynamic simulations. In addition, the single-particle Monte Carlo engine is already integrated into Sentaurus Device and is activated and used through the familiar Sentaurus Device input syntax. On the algorithmic side, due to reduced number of required iterations with the Poisson equation, the single-particle approach offers the potential to extend device Monte Carlo to 3-D and to obtain significant speedups in wall-clock time via parallelization. In fact, one of the main features added to device Monte Carlo for F-2011.09 is parallelization through multi-threading.

Parallelization

Single-particle device Monte Carlo is based on the propagation of independent particles through the device structure. Quantities like the position dependent carrier density and velocity are successively constructed from the trajectories of these particles. This statistics collection procedure takes place at fixed electrostatic potential. After enough statistics for smooth density profiles has been collected, Poisson's equation will be called to update the electrostatic potential. In this manner, a self-consistent solution of the Boltzmann transport equation and Poisson's equation is obtained in a relatively small number of iterations (typically 20 to 50) [30].

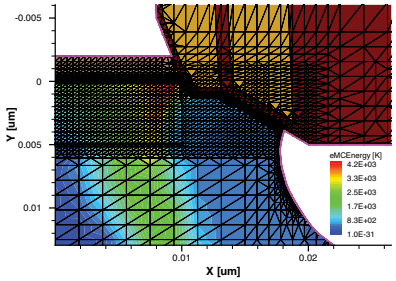


Figure 28: Drain-end of an Lg=20nm bulk nMOSFET showing the mean carrier energy computed with Device Monte Carlo within a non-planar device with an unstructured mesh.

The computational effort involved in single-particle Monte Carlo simulation is almost exclusively spent on the statistics collection part. Since the construction of different particle trajectories is independent, this task is well suited for parallelization. Instead of tracking just a single particle in a single thread of execution, an OpenMP thread-pool can be employed to propagate several particles simultaneously, one particle per thread. Compared to serial execution, this allows collection of equivalent particle distribution statistics in a fraction of 1/#threads of the single-threaded (wall-clock) time. Initial set-up tasks and communication between the Boltzmann and the Poisson equation introduce some overhead that may detract from ideal scaling. Despite this, the speed-up observed in realistic application examples is typically around 10× on 12 threads. Long-running simulations usually profit more easily from parallelization than short running simulations, because constant computational overhead becomes less relevant. This explains why in Figure 29 the long channel device (total runtime: 2h) experiences essentially ideal scaling all the way up to 12 threads, whereas the speed-up of the much less expensive short-channel simulation (total run-time about 15min, brief sampling intervals between Poisson updates) saturates at around 6.5, corresponding to a wall-clock time of 2:20min.

Parallel execution is controlled by the `numberOfSolverThreads` keyword in the Math section of the Sentaurus Device input file. One license of Sentaurus Parallel enables four threads.

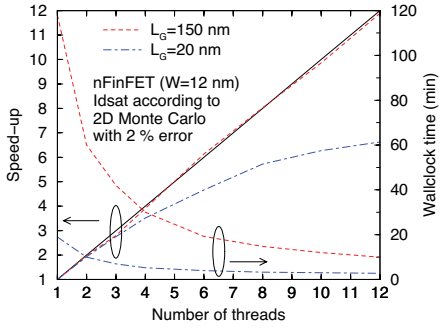


Figure 29: Parallel speed-up of a single-particle device Monte Carlo simulation of long and short channel nFinFET devices; the simulation domain is a horizontal 2D cut through the fin.

Other Enhancements in Sentaurus Device

Improved Gaussian Density of States

Gaussian density of states is a prerequisite for an accurate computation of the carrier densities in the emerging organic devices, where the classical parabolic density of states is known to produce poor results. A new Gaussian density-of-states implementation covering the non-degenerate and degenerate cases is now available. In the new implementation, the carrier densities are computed based on an analytical approximation of the Gauss-Fermi integral [31]. The accuracy of the analytical approximation is good enough for most practical problems encountered in organic devices.

Level 69 PSP100 DFM Support Series Model

A new compact model based on HSPICE MOSFET level 69 PSP100 DFM support series was added to the set of available MOSFET compact models. The new compact MOSFET model is intended for digital, analog

and RF design. It is a surface-potential based model containing all relevant physical effects to model present-day and upcoming deep-submicron bulk CMOS technologies.

Floating Metal Region Embedded in a Wide-bandgap Semiconductor

The metal floating gate has been generalized so that it can be used not only with insulator but also with wide bandgap semiconductors. This is similar to the previously introduced model for generalized semiconductor floating region with charge boundary condition. The new generalized metal floating model is a simpler and more robust alternative than its generalized semiconductor floating gate counterpart. It can be used as a faster and more robust approach for simulating memory devices when no details about the inside of the memory cells are needed.

As an example, a structure with three memory cells in a NAND flash string with two select transistors on either end is used to study programming disturb effects. The dimensions of the memory cell gates and the spaces between them are typical of a 45 nm node. The gates of the select transistors are 2 µm long to accommodate the larger voltages applied to them, and they are each spaced 120 nm away from the memory cell string to minimize the program disturb effects. The structure and biasing voltages are shown in Figure 30. In this example, generalized metal floating gates are used to model the memory cell string. The SHE distribution is used for accurate modeling of hot carrier injection. The oxide on the top of the channel is replaced by an `OxideAsSemiconductor` layer to allow tracing of injected hot carriers toward all the metal floating gates in the string. Figure 31 shows the memory cells disturbance due to the chosen disturbing biases on the control gates. The example shows how the new generalized metal floating gate can be combined with other models to study in great detail problems in memory devices which could not be easily been solved before.

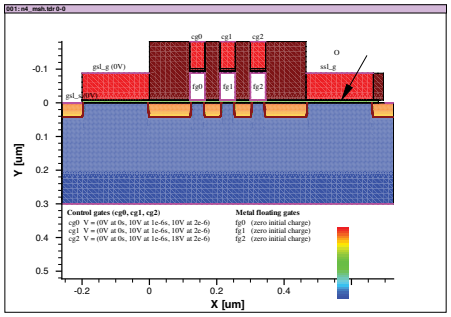


Figure 30: NAND Flash String Structure

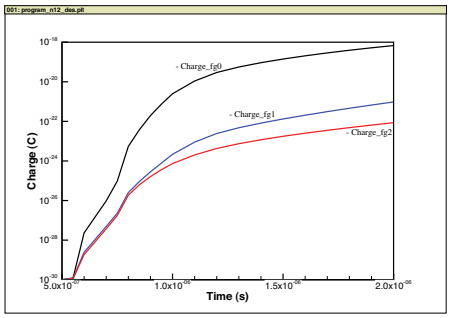


Figure 31: Disturbance Simulation of NAND Flash String

Sentaurus Interconnect

Sentaurus Interconnect, the latest addition to the Sentaurus family of tools, was released in October of 2010. The December issue of TCAD News introduced the main current application areas for Sentaurus Interconnect: back-end of line (BEOL) mechanical stress, electromigration and stress migration. In this issue we present an analysis of solder joint reliability, an important topic in flip chip and 3D IC technologies. A new link between Sentaurus Interconnect and a new resistance-capacitance solver in Raphael is also introduced, thereby extending the application of Raphael to more complex interconnect structures.

Reliability Analysis of Solder Joints

Introduction

Solder joints are used to attach die to packages or other die. Reliability of solder joints is an important part of performance characterization of electronic devices. With the introduction of newer materials and smaller sizes, accurate simulation of material behavior in interconnect structures is becoming critical.

Solder joints are subject to high temperatures (close to the melting point) during manufacturing of electronic devices while the operating temperatures of such devices may be in the range of -55°C to 125°C. Such large variations in temperatures can create residual stresses due to different coefficients of thermal expansion of materials used in these devices. Additionally, cyclic temperature changes, while the device is in use, can cause these stresses to build up and solder joints to fail.

Metals and alloys at high temperatures exhibit strain-rate dependence and creep when the material is undergoing plastic deformation. Viscoplastic material models are used to describe such complex behavior. Sentaurus Interconnect implements the Anand model (see [32], [33]) that is well suited for modeling viscoplastic material behavior. Due to its good predictive capability for a variety of alloys and well documented procedure for fitting material parameters to experimental data, this model is widely used in the electronics industry [34]-[36].

This new capability is demonstrated here through finite element based stress analysis of solder joints under cyclic temperature loading.

Model

A typical flip chip model is considered here with an array of solder balls joining a silicon die and a substrate. The flip-chip is assumed to be 3.2 mm long, 3.2 mm wide and 1.18 mm high with 0.2 mm diameter solder balls. The solder balls are made from 96.5Sn3.5Ag solder alloy and have copper pads on top and bottom. The space around the solder balls is occupied by an underfill material. The silicon die and the underfill are encapsulated in a molding compound. Figure 32 shows the details of the model.

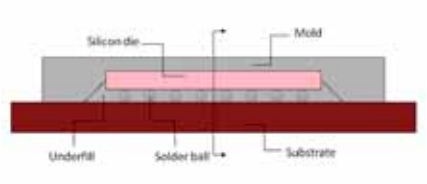


Figure 32: Side view of a flip chip model with symmetry plane. The chip is 3.2 mm long, 3.2 mm wide and 1.18 mm high with 0.2 mm diameter solder balls.

The geometric symmetry of the model is exploited when creating the finite element model, which consists of a single row of solder balls and the surrounding materials, as shown in Figure 33. The bottom, left, back and front faces of the structure are assumed to have zero normal displacements to simulate symmetry boundaries without any rigid body motion.

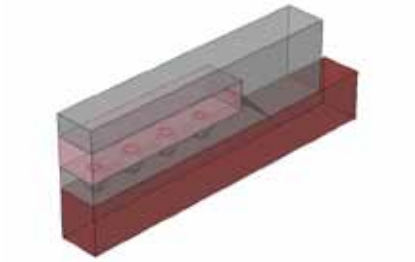


Figure 33: 3D model of a flip chip with 3 symmetry planes. Symmetry boundaries are assumed on left, back and front faces.

Isotropic linear elastic material behavior is assumed for substrate, underfill and mold. The solder balls are modeled as viscoplastic while the copper pads are modeled as elastic-plastic.

A cyclic temperature load is applied to the structure to simulate operational conditions.

Analysis and Discussion of Results

A finite element analysis is performed using Sentaurus Interconnect. Nodal deformations and various components of stresses and strains are extracted from the solution to understand the behavior of solder joints.

Figure 34 shows contours of displacement magnitude for solder balls at the end of the analysis. The leftmost solder ball shows symmetric displacements along the vertical direction. This is consistent with boundary conditions—the bottom and the lateral directions are constrained while the top is free. The displacement pattern becomes less symmetric towards the right. This is also consistent with the free surfaces on the right and the top of the structure.

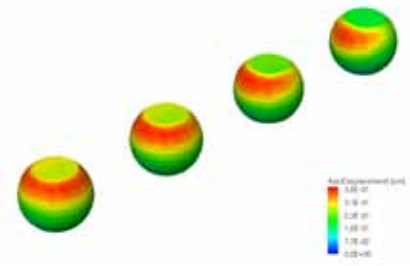


Figure 34: Magnitude of displacements for solder balls.

Figure 35 shows the variation of equivalent viscoplastic strain at the end of the analysis. The magnitudes are higher near the top of the solder balls and increase going from left to right. The strains, which are caused by differences in coefficients of thermal expansion for the solder alloy and other materials, are higher on the right side due to greater displacements around the free surfaces.

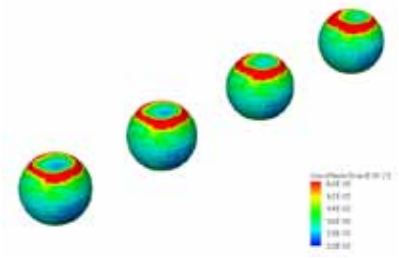


Figure 35: Equivalent viscoplastic strain for solder balls.

Figure 36 shows the variation of von Mises stress over time at a point near front-bottom of solder ball on left (SB1) and at a point near front-bottom of solder ball on the right (SB4). Von Mises stress varies with temperature. After the first cycle, von Mises stress increases when temperature decreases and vice versa. Von Mises stress decreases exponentially (relaxation) when temperature is held constant. This behavior is consistent with viscoplastic model and demonstrates the rate dependence of plastic deformation. The change in extreme values of Mises stress from the first cycle to the last cycle shows the effect of hardening. The jump in Mises stress at the beginning of first cycle is caused by elastic deformation during initial loading of the structure.

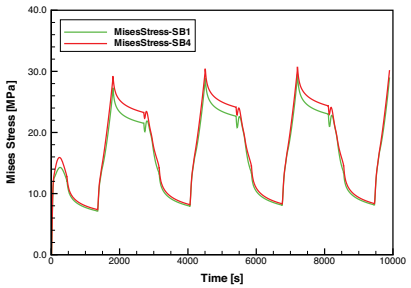


Figure 36: Variation of Mises stress with time at SB1 and SB4.

Figure 37 shows the variation of equivalent viscoplastic strain over time at SB1 and SB4. Equivalent viscoplastic strain increases whenever there is a change in temperature and it remains more or less unchanged when the temperature is constant. Increase in equivalent viscoplastic strain with every cycle indicates build up of plastic deformation that eventually leads to failure.

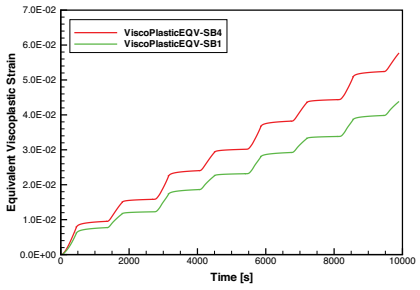


Figure 37: Variation of equivalent viscoplastic strain with time at SB1 and SB4.

Figure 38 shows the variation of viscoplastic shear stress with viscoplastic shear strain in the horizontal plane at SB4. The hysteresis loops show how the material achieves steady state under cyclic loading. The range of

viscoplastic shear strain over a cycle at steady state can be used for predicting lifetime of the solder joints by using fatigue equations like Coffin-Manson.

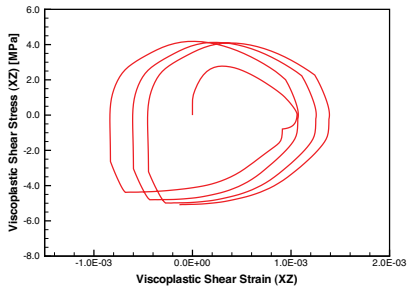


Figure 38: Variation of viscoplastic shear stress with viscoplastic shear strain at SB4 over all loading cycles.

Solder joints undergo complex deformations when the flip chip is subjected to cyclic temperature loading. Proper understanding of the material constitutive behavior is necessary to realistically simulate the evolution of stresses and to predict the failure of solder joints. The Anand model for viscoplasticity in Sentaurus Interconnect provides a valuable tool for advanced material modeling of critical components in electronic devices.

Raphael Interface to Sentaurus Interconnect

The performance of today's deep submicron silicon technologies is dominated by the parasitic capacitance and resistance. The new Raphael solver RCX has been designed to extract parasitic capacitance and resistance in complex interconnect structures. It receives structures from Sentaurus Interconnect through a seamless interface.

In a typical RCX simulation to extract capacitance or resistance, users specify the simulation type with the *mode* command. If no contact information is given with the mode command, all conductors are treated as contacts for the analysis. Floating conductors and/or merged contacts are also supported. Using the above analysis, internal field variables (e.g., electric potential and field, temperature, and current density) can also be extracted and visualized, thus providing users with unsurpassed insight into the electro-thermal characteristics of the interconnect structures.

With Sentaurus Interconnect's powerful geometry creation engine, MGOALS, and meshing engine, Sentaurus Mesh, the RCX solver is able to handle more realistic geometries and thus generates more accurate parasitic models.

Figure 39 shows a six-transistor (6T) SRAM cell interconnect structure [37]. The structure comprises copper conductors (c0, c1, …, c7), from "Contact" to "Metal 3" layers. Various insulating layers fill up the intervening space between metals, including low-k dielectrics and etch stop materials. Silicon is used as the substrate and heat sink.

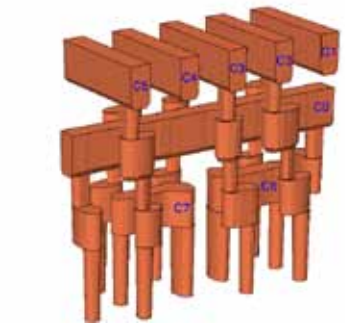


Figure 39: Six-transistor (6T) SRAM cell interconnect structure. Dielectric layers are not shown.

In order to investigate the effect of geometry details, such as tapering and corner rounding, a set of metal shapes, mainly due to etching variations, are compared as shown in Figure 40. With the same layout, shape (1) results from an anisotropic etching, shape (2) results from an 89-degree trapezoidal etching, and shape (3) incorporates additional tapering between metal and via layers, and corner rounding at the bottom of vias and contacts. The angle of tapering can vary during manufacturing and can change the parasitic capacitance values between metal lines due to thinner vertical profiles at the bottoms. Table 3 shows the capacitance difference between shapes (1) and (2) can be up to 7.8%. Another 3.3% difference is observed if the metals are thinned further from the shape (2) to shape (3) due to dual damascene processing and corner rounding at the intersections with etch stop layers.

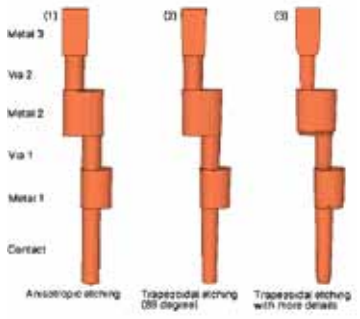


Figure 40: Shape changes due to process variations.

	c0	c1	c2	c3	c4	c5	c6	c7
c0	-3.3%	-3.8%	-2.9%	-2.2%	-2.8%	-4.0%	-3.6%	-3.6%
c1	-3.8%	-4.2%	-2.3%	-1.4%	-0.8%	-1.0%	-7.8%	-1.8%
c2	-2.9%	-2.3%	-3.8%	-3.3%	-0.5%	-0.9%	-7.6%	-1.9%
c3	-2.2%	-1.4%	-3.3%	-4.3%	-3.3%	-1.5%	-7.0%	-7.0%
c4	-2.8%	-0.8%	-0.5%	-3.3%	-3.8%	-2.3%	-1.9%	-7.6%
c5	-4.0%	-1.0%	-0.9%	-1.5%	-2.3%	-4.3%	-2.1%	-7.8%
c6	-3.6%	-7.8%	-7.6%	-7.0%	-1.9%	-2.1%	-6.4%	-6.0%
c7	-3.6%	-1.8%	-1.9%	-7.0%	-7.6%	-7.8%	-6.0%	-6.4%

Table 3: Percentage change in parasitic capacitances between shapes (1) and (2) for the contacts as shown in Figure 39.

Mixed Mode Analysis with Sentaurus Compact Models

Sentaurus Compact Model (SCM) is now available in Sentaurus Interconnect for mixed-mode analysis. Mixed mode analysis increases the accuracy and flexibility of Sentaurus Interconnect analyses by including external compact models in the simulation.

The compact models support external and internal nodes and general device types. The device types include elementary devices such as resistor, capacitor and voltage controlled switches, voltage and current sources and transistors and diodes. Certain HSPICE MOS models are also available.

The compact models in Sentaurus Interconnect are consistent with those in Sentaurus Device. To use this feature, the users can define the circuit model in three different ways:

1. Using external files .scf using Sentaurus Device language
2. Using System command
3. Using new Sentaurus Interconnect circuit command.

All supported models are accessible with the combination of these 3 types of syntax. Due to the use of compact models instead of physical transistors, a mixed mode simulation usually consumes considerable less CPU time. While a circuit can be simulated with compact models components exclusively, the real advantage of this feature is when one or more physical structures are combined with the compact models. The capability is demonstrated in the following SRAM example which contains a physical interconnect structure as the back-end and a set of six transistors as the front-end which are defined with compact models. The six transistors, defined as compact models, are connected to the contacts in the physical structure, while a set of voltage sources are connected to higher metal levels. Figure 41 shows the circuit schematic and the connections to the physical structure. The transistor models are generated from Predictive Technology Model (PTM) (BSIM4) for the 32nm CMOS technology node with threshold voltages of +0.25V/-0.20V, a drain voltage of 0.9V, and optimized subthreshold drain induced barrier lowering (DIBL) coefficients [38]. The p-type transistors and n-type access transistors are designed with 0.03µm long and 0.06µm width, while the n-type driver transistor are bigger, nearly two times wider, to maintain proper write/read operations [39].

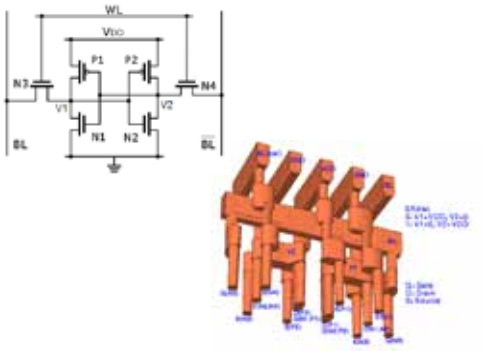


Figure 41: 6T SRAM circuit schematic and connections.

The 6T SRAM cell comprises two cross-coupled CMOS inventers with two access transistors. By sweeping the output of one inverter and observing the output of the other one, the voltage transfer characteristics (VTC) are extracted as seen in Figure 42, where the SRAM cell is in the hold state and the upper-left and lower-right intersection of the curves represent the logical stable states, 0 or 1. The static noise margin (SNM) with a value of 0.31V is plotted as a key merit of stability.

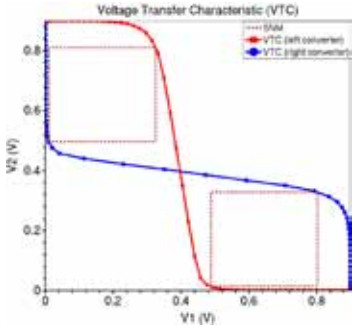


Figure 42: 6T SRAM static noise margin plots in "Hold" operation computed with the physical interconnect structure as shown in Figure 40 and compact models for all transistors.

During the operation of SRAM, current flow causes heat generation within the copper interconnect structure due to Joule heating. Sentaurus Interconnect is capable of capturing heat generation by coupling electrical and thermal analysis. While the thermal analysis is not yet supported in Sentaurus Interconnect for compact models (SCM) in the F-2011.09 release, thermal analysis is available for the interconnect structures. Figure 43 shows the temperature trend at point V2 in figure 41 during a set of repeating read/write operations. The temperature increases during the initial few cycles, and eventually reaches a balance between joule heating and thermal dissipation. After that, the temperature oscillates with the operation cycle: increasing with a current flow (read/write) and decreasing when holding.

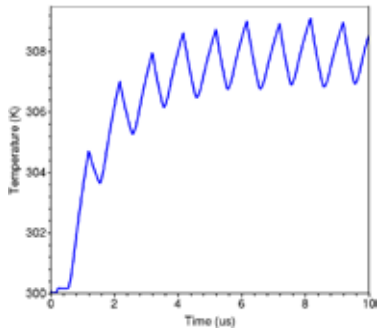


Figure 43: Temperature changes during SRAM operations.

Point Force and Pressure Boundary Condition for Mechanics

The F-2011.09 release of Sentaurus Interconnect introduces point force and pressure boundary conditions. The point force boundary condition allows the user to apply a concentrated load directly on the bulk nodes. Figure 44 shows the displacement and stress profiles due to a point force loading at the center of the top surface. High stress concentration is noted near the node where point force is applied. The pressure boundary condition applies a uniform pressure on the exterior boundary using a distributed load.

This boundary condition is applied through equivalent nodal forces and can also be applied to contacts.

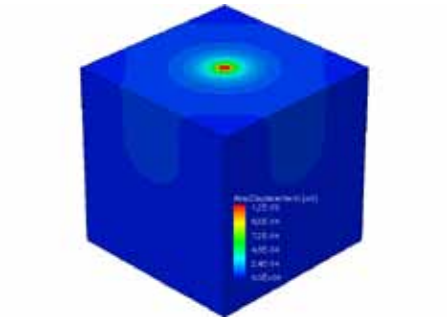


Figure 44: Plots of z-component of displacement vector due to a point force applied at the center of the top surface in the z-direction.

Sentaurus Mesh

In this release, the offsetting algorithm has been extended to work with 2-D structures. With this feature, which can be triggered with "-offset" option in the command line, the user can generate continuous layers from a requested interface and combine them with the 2-D axis-aligned refinement available in Sentaurus Mesh. Usage of this feature is recommended when the input device boundary contains curved interfaces. All the existing noffset3d command files are supported, except for a few parameters which are disregarded by the algorithm. Figure 45 shows an example mesh containing layering along the trench generated by Sentaurus Mesh.

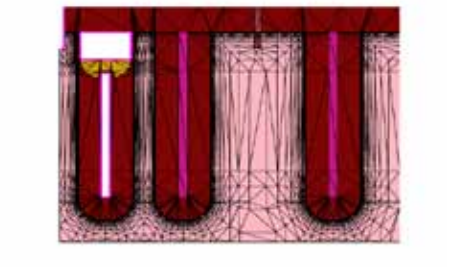


Figure 45: Layered mesh along a trench generated with the new offsetting algorithm.

In addition, two new improvements have been added to increase the robustness of the layering module in this release. The first improvement preserves the axis-aligned faces/edges that intersect layering. This is done to avoid any holes in the junction that is aligned with axis-aligned faces/edges. Figure 46 shows the improvement in maintaining the axis-aligned faces/edges along the junction.

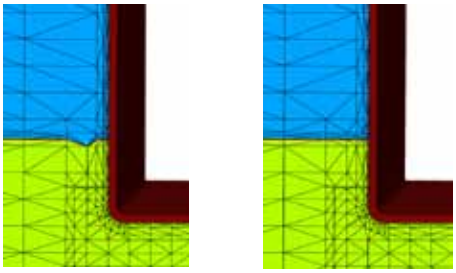


Figure 46: Improvements in the layering module help avoid meshing holes. The left panel shows that in older releases meshing holes could appear in areas where gradient-based refinements and layering competed. These issues have been resolved in F-2011.09.

The second improvement is the addition of an isotropic refinement algorithm to the layering module. Presently, the elements inside the layers may not satisfy the user-refinement specification. With the new isotropic doping refinement option, the elements in the layering are refined isotropically until they satisfy the user-refinement specifications.

In Sentaurus Mesh, a new algorithm allows the user to scan the data fields searching for field gradients that might be missing due to the coarseness of the mesh. When this algorithm is enabled, the mesh generator automatically checks each cell in the binary refinement searching for refinement that could be missing. This feature is activated with the "overscan" keyword in the AxisAligned section.

Sentaurus Structure Editor

The Sentaurus Structure Editor GUI provides a command line window for executing the Scheme scripting commands. The Scheme command line window allows typing and copy-pasting with some limited editing capability. In case the user wants to debug or partially execute a Scheme script, the script file needs to be opened in a separate text editor and the scripting commands need to be copy-pasted to the Sentaurus Structure Editor command line window. This technique is rather slow and error prone, especially for longer scripts. Release F-2011-09 of Sentaurus Structure Editor can be coupled with the powerful Java based text editor jEdit.

When jEdit is installed, the Edit pull down menu in Sentaurus Structure Editor will contain a Text Editor menu item (see also [40]). By selecting the Text Editor menu item, jEdit can be launched from Sentaurus Structure Editor in such a way that jEdit is coupled with the Sentaurus Structure Editor Scheme command line window. A Scheme script file can be opened in jEdit and individual Scheme commands, or blocks of Scheme commands, can be selected in jEdit and then executed directly in Sentaurus Structure Editor. The selected Scheme commands can be executed in Sentaurus Structure Editor by the jEdit Plugins -> Send to SSE command (available from the jEdit pull down menu). There are some additional jEdit macros available which can provide the following operations:

- send-command-starting-on-current-line
  * Executes the complete line where the cursor is positioned in jEdit.
- send-next-command
  * Selects the next Scheme command (by parentheses matching) and execute it in Sentaurus Structure Editor (F8)
- send-selected
  * Executes the selected command
- send-undo-command
  * Executes the (roll) Scheme command

The -editor command line switch can also be used to start Sentaurus Structure Editor in a coupled mode with jEdit. In this case, jEdit is started together with the Sentaurus Structure Editor GUI. In case a file name is given, as an optional argument, the specified file will be loaded to jEdit.

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