Sentaurus Lithography (S-Litho)

Predictive modeling of lithographic processes

Sentaurus™ Lithography (S-Litho) represents the industry standard in lithography simulation for semiconductor process development and optimization in advanced memory and logic applications.

It covers a wide range of patterning techniques such as proximity printing, deep ultraviolet (DUV), extreme ultraviolet (EUV), and electron beam (e-beam) lithography. Process-limiting effects within the imaging system of an exposure tool can be thoroughly analyzed, taking the impact of mask and substrate topography on photoresist patterning into account. Interfacing S-Litho with TCAD tool such as Sentaurus Topography enables seamless modeling of complex integration techniques such as double-patterning. The link between S-Litho and Proteus™ tools accelerates the development of optical proximity correction (OPC) solutions and supports the verification flow through automated hotspot analysis, significantly reducing cycle time.

Technology simulation plays an invaluable role in the field of advanced process development and optimization. Simulation effectively minimizes experimental engineering lots and short-loop experiments, resulting in accelerated process development, considerable cost savings, and a faster time-to-market.

S-Litho provides all the modeling capabilities necessary to enable engineers to make precise and reliable predictions on the performance of lithography processes and strategies. Individual modules of S-Litho address challenges in all relevant areas.

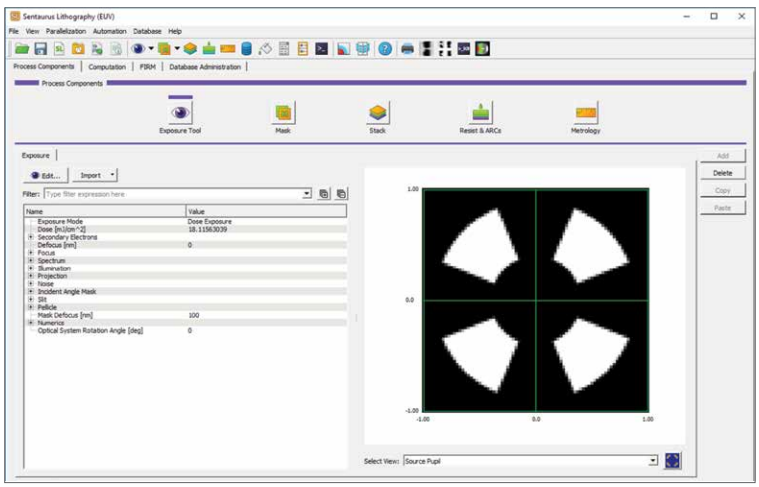

Figure 1: The S-Litho GUI provides full access to all simulation set-up parameters and enables an efficient and powerful analysis of results

S-Litho Benefits

- Predict the impact of process variations on lithographic performance without running costly experiments
- Address complex process integration techniques such as multi-patterning, shortening process development time
- Support lithography strategy path-finding for current and future technology nodes before litho equipment is ready
- Enable early development of mask synthesis solutions for correction and verification, reducing cycle time and accelerating yield ramp, resulting in a faster time to market

S-Litho Introduction and Key Functionality

S-Litho offers a comprehensive feature set, using the predictive power of computational lithography to cost-effectively explore complex technology options. All functionality is embedded in an intuitive graphical user interface (Figure 1) which allows engineers to navigate easily through a wide range of lithography simulation features. S-Litho supports simulation setup and analysis capabilities for the most advanced process technologies:

- Realistic simulation conditions through parameters characterizing the most relevant exposure tool properties
- High flexibility through importing arbitrary layout clips, and creating programmable, parameterized test patterns
- Powerful assessment through multi-dimensional parametric analysis, process window evaluation, and optimization
- Accurate 3D resist profile representation through physical models, built within an integrated calibration environment

DUV (Optical) Lithography Simulation

In today's IC manufacturing, the DUV (i.e. optical) lithography process is the most frequently used patterning technology step for critical layers in high volume production. S-Litho enables simulation of all relevant effects impacting the lithographic performance of the exposure tool/resist processing system:

- From broadband exposure via i-line to ArF immersion projection lithography
- Comprehensive mask treatment, including transmission and phase effects due to mask topography
- Accurate treatment of pre-patterned wafers, e.g. for implant layers (Figure 2) or wafer alignment marks
- Advanced resist processing, including Negative Tone Development (NTD), resist shrinkage and post-development bake steps (reflow)

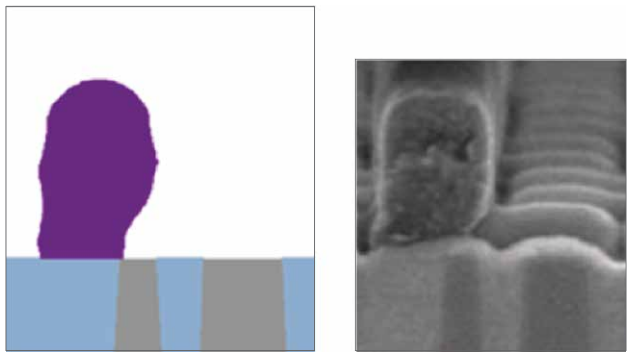

Figure 2: Resist 3D profile prediction on implant layer

Proximity Printing—Lithography Simulation

Within the manufacturing process of micro-electro-mechanical systems (MEMS) or modern flat panel displays (FPDs), classical proximity printing techniques are used for lithographic patterning. As the resolution limit of the exposure tools is approached, simulations become essential for process optimization. The simulation engine has been adjusted to efficiently address Proximity Printing specific parameters such as the gap size. Distinct patterning techniques such as gray-scale lithography, and resist processing steps such as Resist Reflow, can be used to engineer a 3D resist profile target shape.

EUV Lithography Simulation

EUV lithography has been introduced into high volume production for printing the most critical features at the N7 technology node. It becomes mandatory to understand and accurately quantify effects which are caused by the EUV specific characteristics of the image and resist pattern formation process. Simulation enables complex sensitivity studies to assess appropriate compensation strategies, validate compact models and develop OPC solutions.

EUV lithography specific simulation functionality includes:

- Non-telecentric illumination of the reflective EUV mask, including topography effects, pattern shift, shadowing, etc.
- Printability assessment of multi-layer defects
- Through slit aberration and source characteristics
- Stochastic modeling, line edge roughness (LER) characterization and prediction of nano-defects (Figure 3)
- Advanced EUV resist processes and novel materials such as metal-oxide cluster-based resists
- Coverage of high-NA projection and anamorphic imaging, addressing next generation EUV lithography challenges

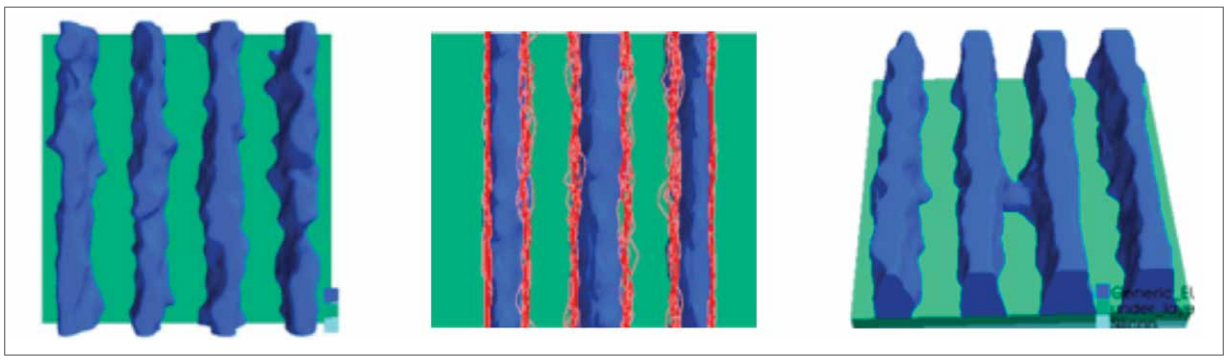

Figure 3: Stochastic simulation results. Single run result with LER (left); contour results of multiple runs (middle); localized nano bridge defect (right)

Electron-beam (e-beam) Lithography Simulation

Traditionally, e-beam lithography is used to define the pattern within the absorber layer on photomasks. Moreover, it can be applied to direct-write device-specific structures on the substrate (mask-less lithography), offering an alternative to DUV/EUV lithography during device prototyping. S-Litho addresses both use models for e-beam assisted patterning, mask-writing as well as wafer direct-write. Simulation is based on characteristics of electron scattering in the potentially inhomogeneous substrate. A detailed understanding of the mask absorber patterning process and resulting mask properties such as corner-rounding and slide wall angle become essential for creating models deployed in full-chip optical proximity correction (OPC) and verification.

Automation and Parallelization

S-Litho offers numerous pre-defined analysis capabilities as well as supports a flexible, multi-dimensional parametric exploration of any given parameter space. State-of-the-art multi-core processors or compute clusters can be used to parallelize computations and significantly reduce simulation time without sacrificing accuracy. The built-in application programing interface (API) allows users to customize and execute complex simulation tasks, and to integrate S-Litho into application flows. S-Litho supports:

- Parallel computations on Linux® and Microsoft® Windows operating systems, using multi-threading or distributed processing
- Extensive support of scripting, including Python™, MathWorks® MATLAB®, and Tcl/Tk

These capabilities are being used to interface S-Litho with other Synopsys tools:

- Interface to Sentaurus TCAD tools, enabling Device-Technology-Co-Optimization (DTCO) flows
  - Process Explorer for setting up substrate topography and multi-patterning scenarios
  - Sentaurus Topography for physical etch simulation, enabling the 3D litho/etch analysis of hotspots
- Interface to Proteus mask synthesis tools, enabling layout centric simulation, rigorous correction and verification

S-Litho/Proteus Interface: Layout Environment, Rigorous Verification and Correction Flows

S-Litho offers a seamless interface to Synopsys' layout editor Proteus WorkBench (PWB), a cockpit tool for OPC development and optimization. This interface enables users to directly access S-Litho simulation results such as resist contours, or 3D profiles directly from within the full-chip layout environment. Results are visualized together with the layout information, while complex simulation settings remain hidden in the background.

The S-Litho/Proteus interface allows users to easily switch between fast compact models and predictive rigorous models within Proteus mask synthesis applications. Within the verification flow, the integration of S-Litho enables a seamless and automated validation of a detected hotspot, using the predictive rigorous model to analyze various process conditions or 3D resist profile behavior (Figure 4, left). Compact and rigorous model results are stored in a common database and can be evaluated independently, which significantly reduces engineering time within the hotspot review process.

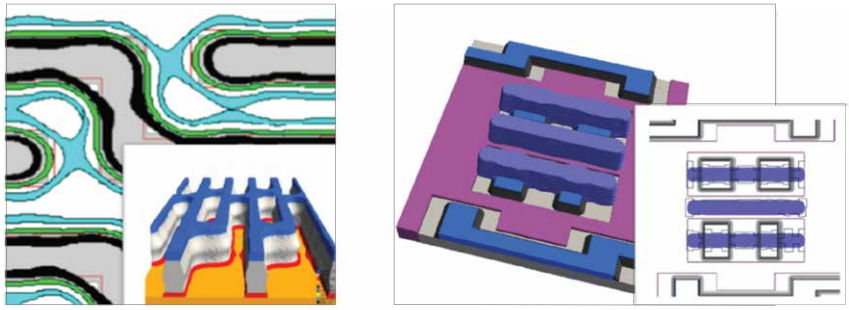

Figure 4: Rigorous verification result of hotspots (left); rigorous correction results based on wafer topography effects (right).

Combining S-Litho with layout correction tools such as Proteus OPC or Proteus ILT facilitates an early development of OPC solutions, since predictive, rigorous models can be used to create and evaluate OPC options long before compact models become available. Moreover, rigorous models can be used to incorporate effects which are not captured by conventional compact models, such as wafer topography at implant layers (Figure 4, right). Localized, rigorous correction has been successfully deployed in the manufacturing of CMOS image sensors or Displays, significantly improving CD uniformity.

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