

Sentaurus Lithography

Predictive modeling of lithographic processes

Overview

Sentaurus Lithography represents advanced lithography simulation for semiconductor device manufacturing process development and optimization.

It covers a wide range of applications in proximity printing, optical, immersion, extreme ultraviolet (EUV), and electron beam (e-beam) lithography. Process-limiting effects within the imaging system of an exposure tool can be thoroughly analyzed, taking the impact of mask and substrate topography on photoresist patterning into account.

Interfacing Sentaurus Lithography with Sentaurus Topography allows a seamless modeling of complex integration techniques such as double-patterning. The link between Sentaurus Lithography and other Synopsys tools in the area of design and mask synthesis accelerates the generation of optical proximity correction (OPC) models, and helps to minimize process sensitivity.

Technology simulation plays an invaluable role in the field of advanced process development and optimization. Simulation effectively minimizes experimental engineering lots and short-loop experiments, resulting in accelerated process development, considerable cost-savings, and a faster time-to-market.

Sentaurus Lithography provides all the modeling capabilities necessary to enable engineers to make precise and reliable predictions on the performance of lithography processes and strategies. Individual modules of Sentaurus Lithography address challenges in all relevant areas.

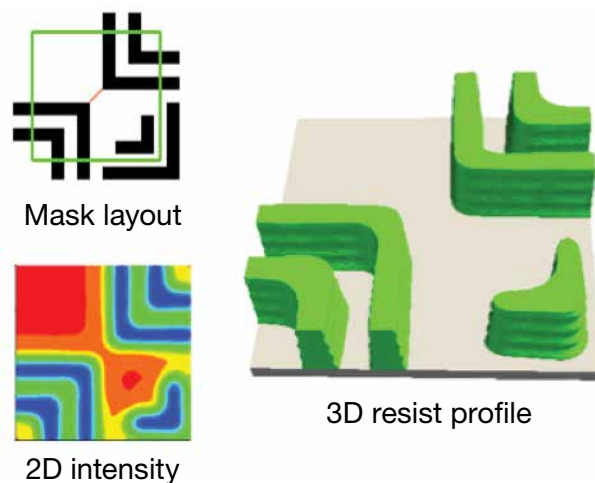


Figure 1: Basic lithography modeling results—2D aerial image and 3D resist profile

Benefits

- Predict the impact of process variations on lithographic performance
- Address complex process integration techniques such as multi-patterning
- Support lithography strategy path-finding for current and future technology nodes by supporting proximity printing, optical projection, EUV and e-beam lithography
- Enable integration with mask synthesis tools to support manufacturing applications, to reduce cost and improve yield

Introducing Sentaurus Lithography

Sentaurus Lithography offers a comprehensive feature set, using the predictive power of computational lithography to cost-effectively explore complex technology options, defining the lithography strategy for current and future technology nodes, extending from single exposures in dry lithography to the application of immersion and multiple exposure or patterning techniques. In addition, effects specific to EUV and e-beam lithography can be investigated.

Resist simulations in 3D are particularly important, since they can reveal details that remain hidden in the aerial image, see Figure 1. In order to be able to predict the behavior of a lithographic result for a given process under changing conditions, it is essential to calibrate a few resist model parameters against experimental data, such as CDs and cross sections, including information on side wall angles and resist height loss. Sentaurus Lithography enables users to calibrate or fine tune model parameters for their own specific processes, which is essential for obtaining predictive resist models.

All Sentaurus Lithography features are embedded in an intuitive graphical user interface, which allows engineers to navigate easily through a wide range of lithography simulation capabilities. Engineers can look at the behavior of an individual evaluation parameter, or perform complex computational investigations, from a multi-dimensional parametric analysis to optimization tasks.

Moreover, Sentaurus Lithography includes a comprehensive set of features to analyze process windows based on modeled data. For more information, please see the Sentaurus Lithography PWA (Process Window Analyzer) datasheet.

Sentaurus Lithography provides an interface to a central database that acts as a repository for all information relevant to a simulation. Extensive scripting functionality allows users to set up and automate complex design of experiments, and supports integration into customized workflows.

Advanced algorithms of Sentaurus Lithography use state-of-the-art hardware resources such as multi-core CPUs or high-performance computation clusters in an optimum way, which enables engineers to address highly complex, multi-dimensional problems, or the simulation of large areas in a timely manner.

Optical Lithography

In today's IC manufacturing, the optical lithography process is the most critical patterning technology step. Sentaurus Lithography enables simulation of all relevant effects that influence the lithographic performance of a system. It can be used to analyze the impact of different source shapes, single wavelength or broadband exposures, optical effects caused by projection lens aberrations and polarization, noise, as well as multiple-exposure techniques for resolution enhancement—in both dry and immersion lithography.

The integrated layout editor allows the generation of parameterized test patterns, the drawing of arbitrary mask features, or the import of GDS2 clips from a production mask layout.

3D Structures on the Mask

If dimensions on the mask level approach the wavelength of the exposure light, transmission and phase effects need to be considered in the modeling approach. Sentaurus Lithography allows detailed studies of variances that are introduced by the mask-making process, such as corner-rounding and sidewall angles of the mask absorber layer material.

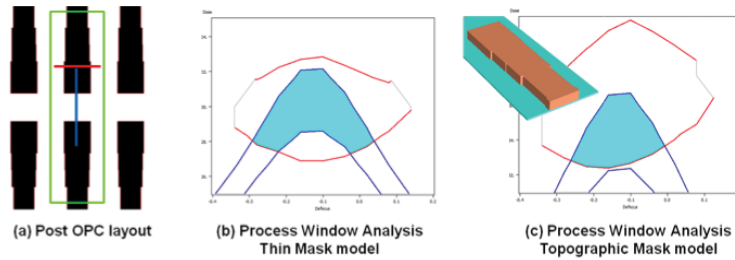


Figure 2: Process window analysis for a test pattern under thin mask and topographic mask modeling conditions

Figure 2 shows an example where the impact of the modeling approach on the overlapping process window is demonstrated. The test structure is shown in Figure 2a, with gauges defined for the line width as well as the line-end to line-end gap. The process windows differ noticeably, depending on the thin mask model (Figure 2b) or the topographic mask model (Figure 2c).

Simulations help to quantify the corresponding effects, which need to be taken into account for optical proximity effect correction schemes.

Patterned Wafer Substrates

Upcoming process integration technologies such as double-patterning require accurate simulation of critical imaging layers on pre-patterned surfaces, either nonplanar or planar with locally varying optical properties.

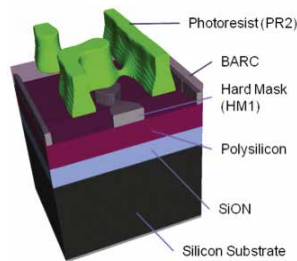


Figure 3: Wafer topography simulation result for a double patterning/pitch split example

Figure 3 shows the simulation result of the second lithography step in a double-patterning process. The first patterning step creates a well-defined topography within the hard mask (HM1). In this example, the presence of topography in combination with its optical properties causes bridging of the photoresist structures (PR2) at a critical location. On a planar, homogeneous wafer stack, these structures would be well resolved and separated.

The links between Sentaurus Lithography and other tools of the TCAD Sentaurus product family offer simulation capabilities for complex technology options, including parameter variations across different process steps. Figure 4 demonstrates the link between Sentaurus Lithography and Sentaurus Topography 3D. The lithography results, i.e. the developed resist profile, is automatically transferred to Sentaurus Topography 3D for modeling of the etch step. The final results can be inspected within the GUI of Sentaurus Lithography.

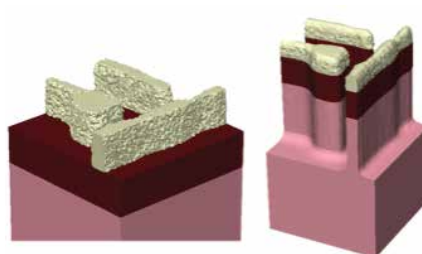


Figure 4: Modeling results after resist development step (left) and after substrate etch step performed by Sentaurus Topography 3D (right)

EUV Lithography

EUV lithography is considered a viable solution for printing the critical features associated with technology nodes below 10nm. It becomes increasingly necessary for all potential EUV users to understand the origin of the sources of CD variations to develop appropriate compensation strategies.

A key requirement in the modeling of EUV lithography processes is the correct treatment of the reflective EUV mask and the resulting nontelecentric illumination, which will cause pattern shift and shadowing effects on the wafer. Imaging itself is very sensitive to flare because of the short exposure wavelength. Moreover, almost unavoidable defects in the multi-layer structure can significantly impact imaging performance.

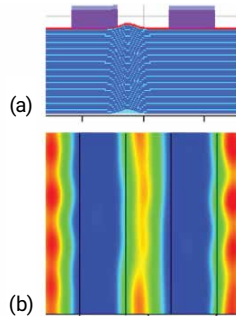


Figure 5: (a) Mask blank defect propagating through the multi-layer stack; (b) resulting aerial image

Figure 5 shows the effect of a Gaussian-shaped mask blank defect on the aerial image of a lines and spaces test pattern. The corresponding result can be used to determine whether or not a defect prints on wafer under different process conditions, and to develop compensation strategies. Simulation offers the opportunity to separate the impact of, for example, illumination, absorber properties, pattern orientation, or flare. It allows determining their significance for manufacturing the actual device and, therefore, enables users to evaluate a suitable correction methodology.

Especially in EUV lithography, statistical effects become more and more a limitation to process performance. The modeling capabilities of Sentaurus Lithography can be extended by a stochastic resist model, which predicts the impact of various process conditions on parameters such as line edge roughness (LER), for which a comprehensive set of analysis methods exists.

Figure 6 illustrates the results of such a simulation, showing LER of a resist line, not only along the side walls, but also on top of the profile due to resist height loss.

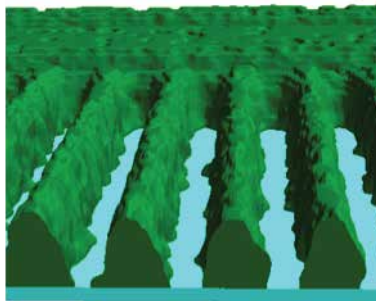


Figure 6: Modeling line edge roughness

E-Beam Lithography

Traditionally, e-beam lithography is used to define the pattern within the absorber layer on photomasks. Moreover, it can be applied to direct-write device-specific structures on the wafer level (maskless lithography), offering an alternative to EUV lithography or complex optical lithography processes such as double-patterning.

Sentaurus Lithography addresses both use models for e-beam assisted patterning, wafer direct-write as well as mask-writing processes. Simulation results include characteristics of the electron scattering in the substrate, as well as a prediction of the 3D resist profile, as it is observed by the lithography engineer. Figure 7 shows the effect of different materials used within a patterned wafer stack, causing a line-width variation for the resist line.

A key application of e-beam lithography simulation is the development and evaluation of proximity correction strategies, even at a very early state of the exposure tool development. This reduces the dependency on the hardware itself and improves development cycle times.

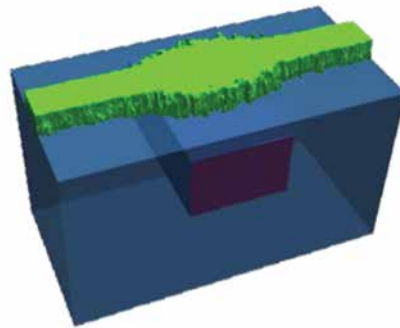


Figure 7: Resist line created by e-beam lithography, running across a buried metal line

Proximity Printing Lithography

Within the manufacturing process of micro-electro-mechanical systems (MEMS) or modern flat panel displays, classical proximity printing techniques are used for lithographic patterning. As the resolution limit of the exposure tools is approached, simulations become essential for reducing process development time.

An area of particular interest is the control of 3D resist profiles in order to simplify subsequent processing steps. A well-established technique to create regions with different resist height is the application of gray scale lithography, which is efficiently supported within Sentaurus Lithography.

Another way to influence the resulting shape of a resist pattern is the tuning of exposure settings such as proximity gap size, or illumination conditions (Figure 8b), and the application of a resist reflow process step, the simulation results of which are shown in Figure 8(c).

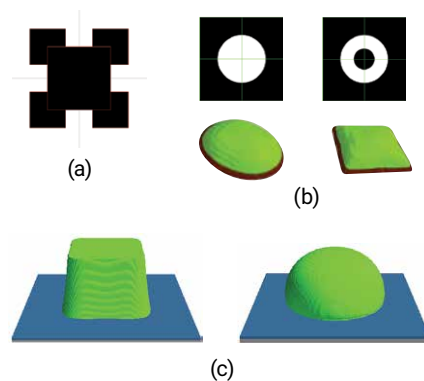


Figure 8: Resist profile simulation result for an array of mask pattern (a) with $CD=5\mu m$ and $pitch=20\mu m$, for (b) different illumination conditions (left: conventional; right: annular) and (c) different resist reflow conditions (left: after development; right: after hard bake at 130 degC for 90 seconds)

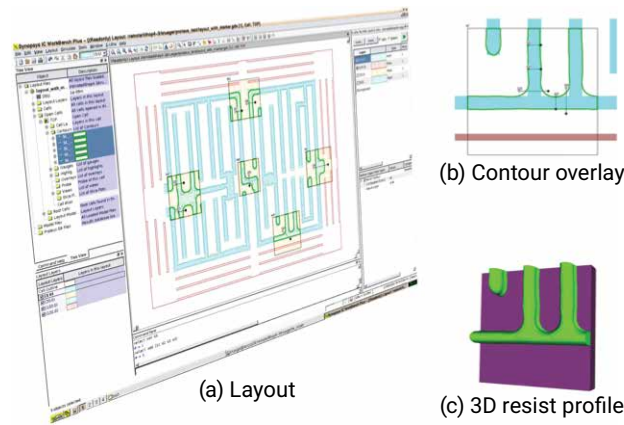


Figure 9: (a) Layout-centric simulation environment, providing direct access to Sentaurus Lithography results such as contours (b) or 3D resist profiles (c)

Layout-Centric Lithography Simulation

Sentaurus Lithography offers a seamless interface to Synopsys' layout editor and viewer tool, IC WorkBench EV+, as well as to Proteus WorkBench (PWB), a cockpit tool for OPC development and optimization. This interface enables users to directly access Sentaurus Lithography simulation results such as resist contours, or even 3D profile information directly from within the full chip layout environment. Results are visualized together with the layout information, while complex simulation settings remain hidden in the background. Simulated resist contours can be overlaid with the layout and 3D resist profile information can be displayed on demand. In case process window parameters are determined, contour bands can be used to display the corresponding results in PWB, as indicated in Figure 9. Moreover, any evaluation results can be accessed through the API, if needed.

Sentaurus Lithography serves as an ideal verification tool for most critical areas or process conditions. For more information on the layout tools, please see the PWB datasheet.

The Power of Parallelization

To accelerate complex simulations with multiple variables or large-area problems, Sentaurus Lithography is able to leverage compute clusters. It intelligently distributes independent parts of a simulation to cluster nodes for processing, thereby offering a highly scalable solution to multi-faceted problems. Moreover, parallel processing on shared-memory hardware such as multi-core systems is supported.

Sentaurus Lithography running on high-performance compute clusters provides the fastest, most scalable and cost-effective computation lithography solution available today.

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