

Proteus Inverse Lithography Technology (ILT)

Advanced Correction of Optical Proximity Effects

Proteus ILT uses inverse imaging technology to resolve the most challenging optical proximity effects encountered on dense designs at leading technology nodes. Increasing design density due to semiconductor technology scaling provides little room for conventional segment-based OPC methodologies resulting in sub-optimal process windows. Proteus ILT significantly increases the degrees of correction freedom by approaching the problem from an inverse imaging perspective to identify the optimal mask shapes that are required to print the design intent. Proteus ILT provides several approaches that eliminate the segment-based correction constraints and enables the ideal placement of assist features and optimal main feature correction resulting in larger process windows and improved image fidelity while minimizing mask complexity and runtime.

Lithography patterning hardware improvements are advancing more slowly than the technology design nodes creating a wider gap between the fundamental resolution limits of the hardware and the features being printed on the mask. This is resulting in marginal process windows, higher correction complexity, and longer turnaround time. Proteus ILT addresses these process challenges with production-proven technology that was the first in the industry to pioneer the use of inverse lithography simulations for proximity correction. Today Proteus ILT is routinely used to increase the process window as shown in Figure 1 and maximize the sidewall angle for improved yield on the most challenging designs.

Flexible Integration for Maximum Efficiency

Proteus ILT is seamlessly integrated into the Proteus environment. Figure 2 illustrates the benefit of this integration by allowing ILT to be deployed only where it is needed most thereby enabling maximum process windows while minimizing mask complexity and turnaround time.

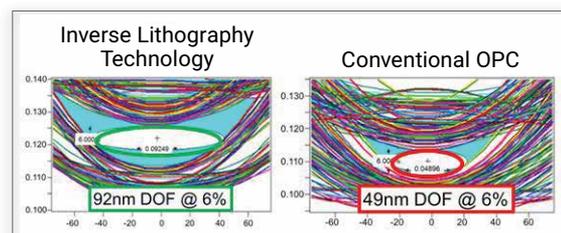


Figure 1: ILT increased common DOF by 43nm

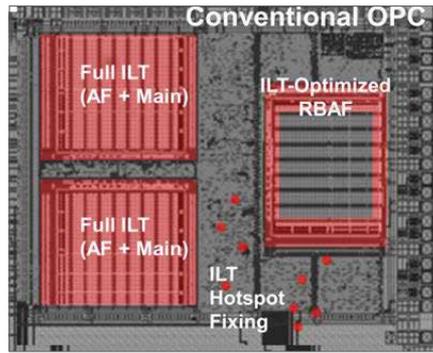


Figure 2: Proteus ILT is only applied where it is needed most

Proteus ILT Applications Resolve Common Mask Synthesis Problems

Proteus ILT can be utilized in multiple stages in the mask synthesis flow to address yield limiting problems found in advanced nodes resulting in up to 25% improvement in CD variability. These problems include RBAF placement limitations, conventional OPC convergence/segmentation problems, and critical hotspot failures (see Figure 3). Depending on the process requirements, one or more of the following ILT applications can be utilized in the mask synthesis flow:

- **ILT-Optimized Assist Features:** ILT is used to optimize the placement and size of assist features that have been placed with rules. This eliminates printing AFs and sidelobes as well as reduces CD variability through process window for improved yield.
- **Full ILT (AF+Main):** The most critical areas of a design (like memory) can take advantage of the full ILT engine to place AFs and correct the main feature. ILT's larger degrees of correction freedom and better correction convergence over conventional OPC delivers the maximum process window and superior quality of results.
- **ILT Hotspot Fixing:** Hotspots found during lithography verification using Proteus LRC can be automatically corrected with Proteus ILT for hotspot fixing and seamlessly blended with the surrounding features. This avoids rerunning OPC on the full layout and reduces costly delays in bringing new products to market.

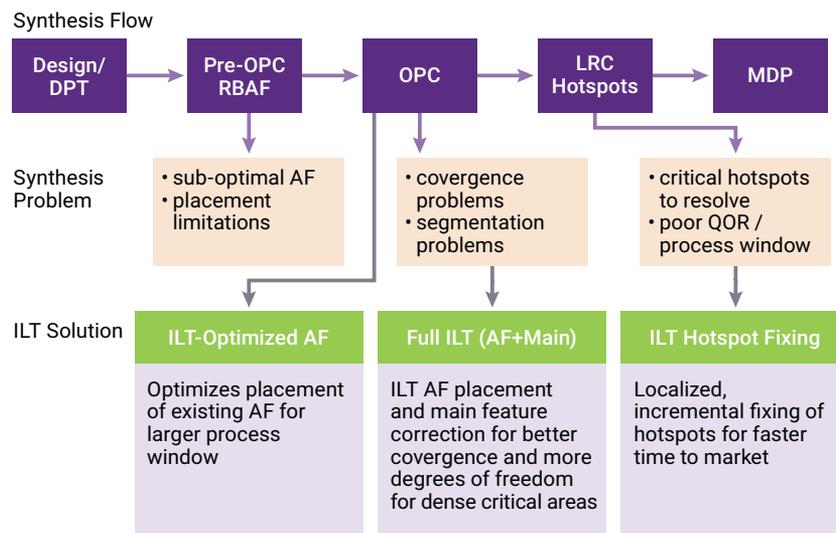


Figure 3: Proteus ILT solutions to common mask synthesis problems

Key Technical Features

- Custom cost functions for controlling the aggressiveness of the correction and prioritizing it by feature type
- Automated pitch relaxation on routing layers to improve contrast and process window

- Efficient handling of periodic structures eliminates redundant simulations and ensures symmetry enforcement for faster TAT and improved quality
- Options for managing mask complexity to keep mask costs down (see Figure 4)
- Seamless OPC-ILT boundary repair for localized insertion

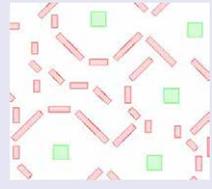
AF Style	Sample AF Style Image	Shot Count
Stair-stepped (complex) Manhattan		777.3K
Simplified Manhattan-45deg only		390.5K

Figure 4: Flexible control of mask complexity and shot count for managing mask costs

Proteus EUV ILT

Proteus EUV ILT provides added inverse lithography correction support for EUV processes enabling correction compensation for off axis shadowing effects and variation across the lens slit. The inverse correction capabilities naturally correct across lens slit effects with asymmetric AFs to maximize the available process window.

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