Proteus

Full-Chip Mask Synthesis

Proteus provides a comprehensive and powerful environment for performing full-chip proximity correction, building models for correction, and analyzing proximity effects on corrected and uncorrected IC layout patterns. Proteus mask synthesis products (Figure 1) are the tools of choice for leading edge IDMs and foundries and have been production proven for over a decade.

Proteus Pipeline Technology provides a fully concurrent tapeout flow for maximum CPU utilization and is a major departure from serial manufacturing flows, in which a complete post-optical proximity correction (OPC) database must be available before the latter applications can be initiated. Using a dual-domain simulation engine which combines the strength of field-based simulation and flash-based simulation, Proteus delivers the most accurate OPC results and fastest turnaround time for both dense and sparse designs. Proteus' programmability and modularized applications provide optimal flexibility while ensuring protection of valuable customer IP.

Benefits

- Production-proven performance and superior quality of results
- Fully pipelined tapeout flow to efficiently utilize expensive hardware resources
- The most accurate, easy to use, and flexible modeling environment
- Production-proven comprehensive suite of RET applications
- Proteus LRC through process window lithography verification
- Sentaurus Lithography rigorous simulation interfaces within Proteus manufacturing tools
- Best cost of ownership through the use of optimized general purpose hardware
- Core technology uniquely connects manufacturing information to design

Production-Proven Performance and Superior Quality of Results

Dual-domain simulation allows for the flexibility to choose from two powerful simulation algorithms in one platform; field-based simulation and flash-based simulation. It also enables the fastest simulation for any process node and pattern density.

The field-based engine simulates in the frequency domain and computes the entire field at once. Since the simulation is done everywhere, it is ideal for applications requiring dense simulations. Flash-based simulation simulates in the geometry domain and is ideal for sparse simulation. The two types of simulation shown in Figure 2 provide users with the flexibility to choose the best simulation methodology for their specific technology and flows.

Minimal effort is required to convert a model and recipe from flash-based format to field-based format; a few clicks in the easy-to-use graphical user interface perform the conversion. No new calibration or silicon verification is required. Users can maximize their return on investment by choosing the fastest simulation algorithm for a given process node and pattern density, while reusing learning between technology nodes.

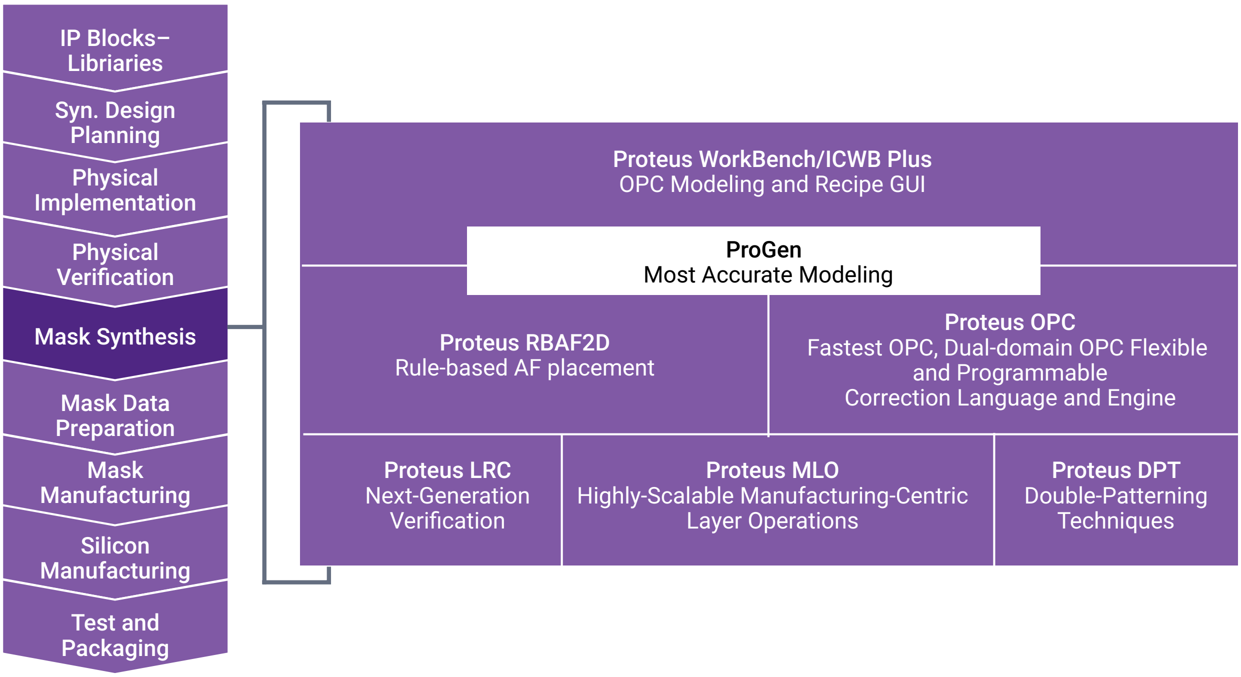


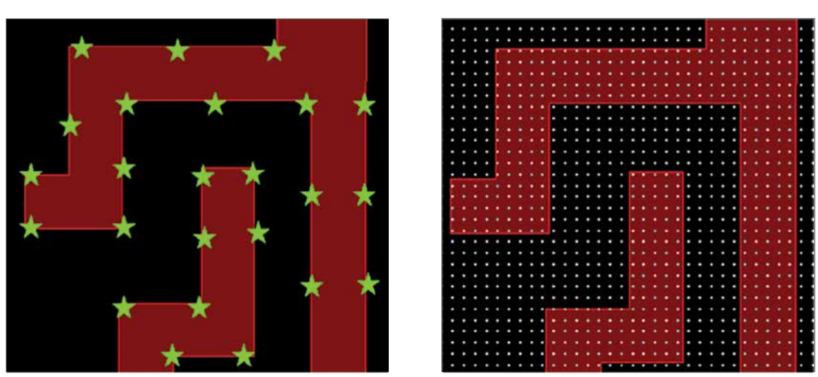
Figure 1: Proteus is a full-chip mask synthesis suite

Fully Pipelined Tapeout Flow to Highly Utilize Expensive Hardware Resources

The industry-unique Proteus Pipeline Technology (Figure 3) utilizes a novel concurrent data-processing mode by which computational resources are uniformly engaged and the effects of

I/O latencies are masked by synchronal processing. Data and computational tasks are distributed over cluster resources so that applications such as resolution enhancement techniques.

(RET), OPC, mask rule checking (MRC), lithography rule checking (LRC), mask data preparation (MDP), and user-customized geometry operations are executed concurrently. Customers benefit by reduced total mask tape-out turnaround time (TAT) and improved hardware utilization, compared to conventional flows that require each sequential stage in the mask tapeout flow to generate a complete database before handing it off to the next stage.



Flash: Discrete sampling in space domain at polygon edges.

Field: Discrete sampling in frequency domain across the entire image.

Figure 2: Dual-domain simulation. Flexibility to choose from two powerful simulation algorithms in one platform; field-based simulation and flash-based simulation

Without the need to hold complete databases at any point, cluster memory footprint is drastically reduced.

Proteus Pipeline Technology benefits include:

- Reduced total mask tape-out TAT
- Improved hardware utilization
  - Concurrent processing of all Proteus and CATS applications
  - Removal of intermediate I/0 and hierarchical management steps
- Reduced cluster memory footprint
- Effortless job-flow environment, offering both ease-of-use and programmability
- Template-aware environment for MRC applications
- Single recipe and layer-operation (Proteus MLO) environment for customization of all pre-OPC, OPC and post-OPC jobs

Highly scalable distributed processing and efficient hierarchy delivers specified target TAT via parallel processing

Proteus products are designed to run on multiple CPUs for fast TAT. A large design database can be dissected, distributed and processed simultaneously using multiple CPUs for shortened cycle time. Users have the flexibility to choose the desired number of CPUs to meet their target TAT. In addition, Proteus is a pioneer in enabling fast TAT through highly efficient hierarchical processing.

Proteus achieves the specified TAT by effectively minimizing the correction redundancy and curtailing correction data expansion. Designs with memory or many repetitive blocks benefit significantly from the Proteus hierarchy processing.

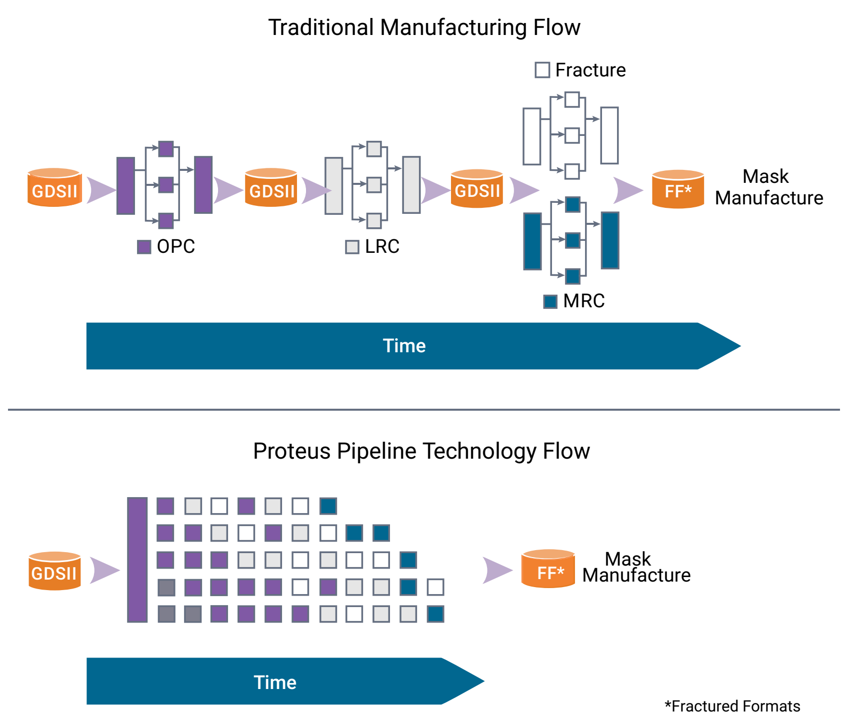


Figure 3. Proteus Pipeline Technology is a fully pipelined tapeout flow that maximizes CPU utilization, reduces memory footprint and significantly reduces TAT

Fast model regression through highly distributed parallel architecture

At advanced process nodes, a large number of optical and resist parameters must be tuned correctly to achieve an accurate model. ProGen supports multi- CPU parallel processing for fast, accurate model creation. ProGen offers near linear scalability and over 37X regression time reduction. As a result, significant savings in model regression time are realized (Figure 4).

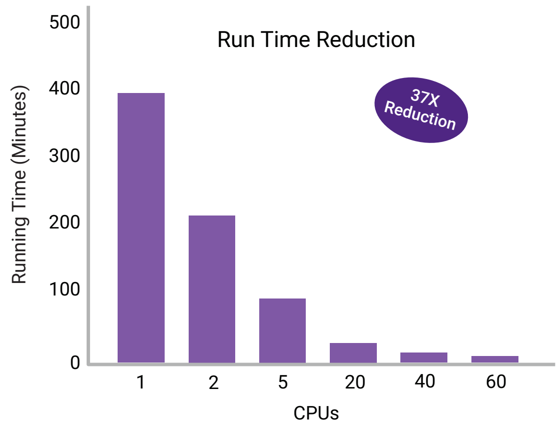


Figure 4: Scalability of ProGen distributed regression

Most Accurate, Easy to Use, Flexible Modeling Environment

Reliable and predictable models through advanced resist profile modeling

ProGen compact models use advanced resist profile modeling techniques, providing the best foundation for highly accurate and predictable models through the process window. In addition, ProGen provides a seamless interface to Sentaurus Lithography, the industry standard for rigorous lithography simulation.

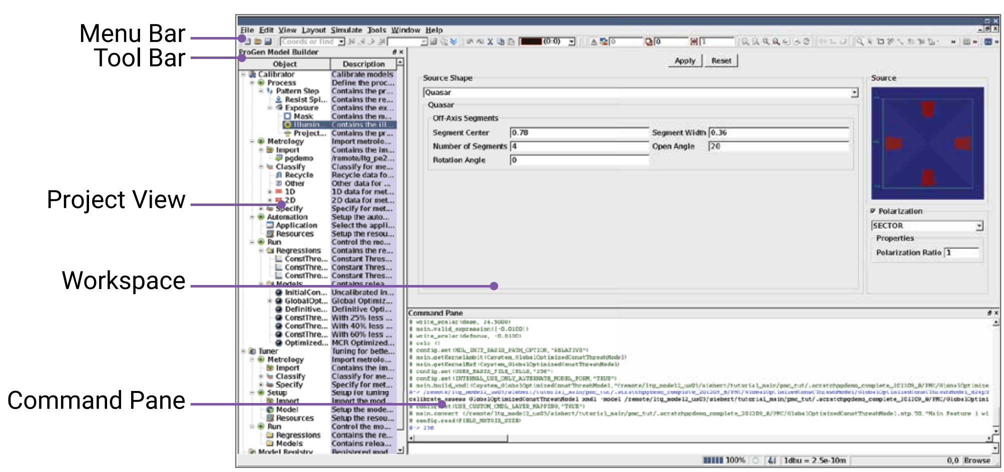


Figure 5. Proteus WorkBench's PMB module for automated model building

Model calibration and recipe tuning automation

The ProGen Model Builder (PMB) module within Proteus WorkBench is the most highly automated model calibration utility on the market (Figure 5). PMB steps the user through a series of prompts for information about their lithography process and measurements of silicon structures.

It uses this information and incorporates modeling best practices and expertise embedded in the tool to provide accurate models for use in OPC, LRC, and RETs.

PMB benefits include:

- Fully-automated calibration environment to eliminate user subjectivity
- Built-in modeling best practices
- Default algorithms emulating Proteus expertise
- Intuitive GUI to ensure model consistency and optimal Time-To-Accurate-Model

Highly accurate models through staged modeling

Based on field-based simulation, stagedmodeling describes optics, resist, etch, and mask phenomena one at a time. This enables accurate description of each process step.

Highly predictive process window modeling

Process Window (PW) modeling facilitates hot spot detection during verification and correction across the process window. Proteus uses a parameterized approach to generate models across the process window. Models at non-nominal conditions are built by extrapolation of the focus and dose shift from the nominal condition, without involving the laborious steps in building each model in a repetitive manner (Figure 6).

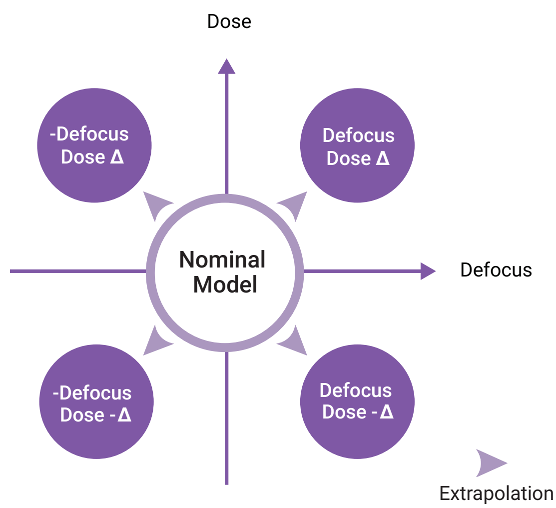


Figure 6: ProGen parameterized process window modeling

Production-proven, Comprehensive Suite of RET Applications

At advanced process nodes, the usable process window can become very small. Extreme ultraviolet lithography provides some added resolution capabilities but also introduces asymmetries, shadowing, and variation across the exposure slit that need to be compensated for. RETs such as Inverse Lithography Technology and Double-Patterning Techniques (DPT) have become necessary to enhance the pattern fidelity and enlarge the process windows. Proteus provides a production-proven and comprehensive suite of RET applications to address these advanced technology needs.

Inverse Lithography Technology Proteus ILT and Proteus EUV ILT use inverse-lithography technology for model-based assist feature positioning and main feature correction (Figure 7) supporting both contact and line/space layers. The optimization process is at both the pixel and polygon level enabling optimal correction and assist feature placement in tight multi-pitch and complex geometry situations for the largest possible process window. Proteus ILT incorporates a printability check to ensure that no assist features will be printed on silicon and can be used to optimize assist features that have already been placed with rules. This correction option can be applied full chip or run in line with Proteus OPC or Proteus EUV and only applied where it is needed most for optimal turn-around time and maximum process window.

- ILT benefits include:Greater degrees of freedom for optimal OPC convergence and larger process windows
- Flexible ILT/OPC hybrid flows to minimize runtime
- More robust and symmetric AF placement without complex scripting
- No empirical data required for AF placement ILT-based hotspot fixing for faster time to market

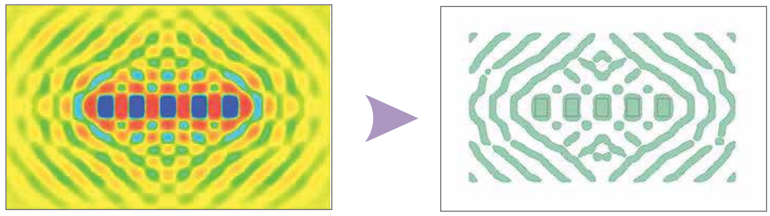


Figure 7: Proteus MBAF IMT placements on contacts

Production-proven Proteus DPT

Proteus DPT offers unmatched design compliance checking and cost-based solver, reducing design-rule violations. Proteus DPT ensures decomposition symmetry through mask-rule constraints (MRC), as shown in Figure 8, resulting in uniform mask density and hierarchy retention in all design types, which minimizes runtime. Color seeding is offered to enable more design and route-level control as additional means to retain hierarchy and to minimize runtime. Proteus DPT operates in the Proteus Pipeline to facilitate the most cost-efficient decomposition techniques on the market.

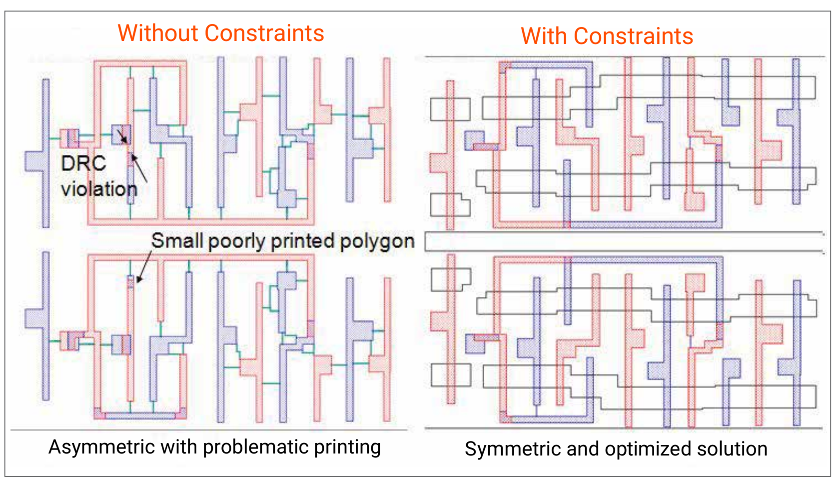


Figure 8: MRC turned on in Proteus DPT enforces symmetry

Proteus LRC Lithography Verification

Proteus LRC provides a comprehensive set of process window aware check functions to identify traditional process failures before committing a design to manufacture. For the unique challenges associated with double patterning processes, there are DPT-specific functions to reduce deployment time and consolidate results for efficient review. The highest level of accuracy is achieved with industry-proven OPC models and embedded access to rigorous first-principle models from Sentaurus Lithography for thorough analysis of resist profile and topography affects (Figure 9). Built on the Proteus engine, Proteus LRC is fully integrated into the Proteus Pipeline Technology for near-linear scalability to support the large data volume and dense transistor designs of the most demanding leading-edge full-chip applications. Proteus LRC is completely enabled for EUV deployment with the lowest cost of ownership on standard x86 hardware.

Sentaurus Lithography Rigorous Simulation Interfaces Within Proteus Manufacturing Tools

Sentaurus Lithography is the reference simulator for all lithographic process solutions, and with the 20nm node and beyond, there is demand to have rigorous simulation reference flows within the manufacturing environment. Sentaurus Lithography resist model calibration is now fully integrated into Proteus WorkBench allowing users to supplement experimental data by rigorous simulation results and validate compact model performance. Sentaurus Lithography is also embedded into Proteus LRC for automated rigorous calls on marginal verification checks. Lastly, a Sentaurus Lithography interface resides within Proteus OPC to execute localized rigorous correction when needed.

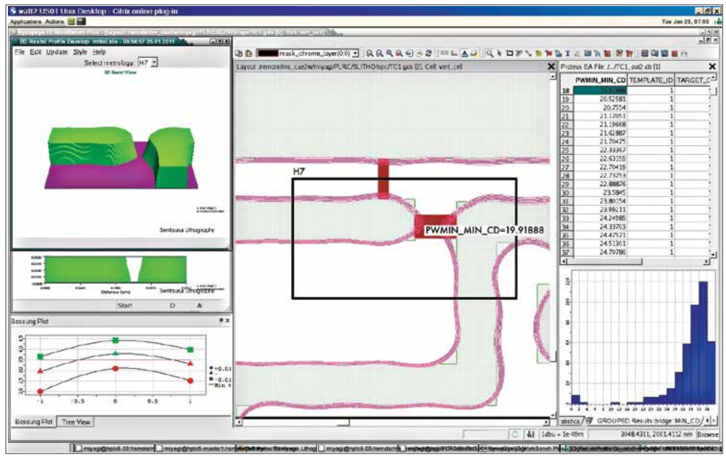


Figure 9: Proteus Error Analysis Module in Proteus WorkBench

Core Technology Uniquely Linked to Synopsys Manufacturing Solutions

Mask synthesis impacts yield and manufacturability of designs and is a key component of a complete Manufacturing solution. Proteus provides the core manufacturing link for multiple Synopsys tools, including Yield Management and PrimeYield LCC, enabling key Manufacturing links across the Synopsys portfolio.

For more information please contact your local sales representative or email us at manufacturing@synopsys.com.