SYNOPSYS®

DATASHEET

Avalon

CAD Navigation and Fault Isolation Solution for Failure Analysis

Overview

Synopsys Avalon™ is the industry standard CAD navigation and fault isolation solution for failure analysis, design debug and low-yield analysis of microelectronics. Avalon is an advanced solution that provides a complete environment for fast, efficient and accurate investigation of potential device failures indicated by test and diagnostics tools. Avalon optimizes the efficiency of failure analysis (FA) equipment and personnel resources associated with design and semiconductor FA labs by providing an easy-to-use software interface and navigation capabilities for almost every type of test and analytical FA equipment.

Avalon provides an option for CAD navigation for system-level failure analysis of multi-chip module (MCM) and printed circuit board (PCB) with interactive signal tracing and cross-probing between board → substrate → interposer → die → FA equipment, etc. as well as correlation with design elements to facilitate fast and accurate fault isolation. This solution option provides system-level CAD navigation capabilities and interfaces with most of the leading FA equipment used in FA labs.\

Avalon enables close collaboration between product and design groups and FA labs, dramatically improving time to yield and thus, time to market. Avalon can import CAD design data from all key design tools and several user-proprietary formats while providing visual representations of circuits that can be annotated, explored, searched and linked with ease.

Benefits

- Improves failure analysis productivity through a common software platform for various equipment in FA labs
- Significantly reduces FA cycle time and hence decreases time to market
- Faster problem solving by cross-mapping between device nodes to view all three design domains (layout, netlist and schematic) simultaneously
- Complete access to all debug tools that are critical for circuit debug and hence faster root cause analysis of demonstrable defects
- Design independent solution that supports all major design platforms and layout versus schematic (LVS) tools
- Enables secure access to all FA information using Avalon's KDB™ database
- Ease of conversion from layout, netlist and schematic data to KDB™ database and establishing cross-mapping links between data domains
- Simple deployment setup with support for Linux and Windows operating systems

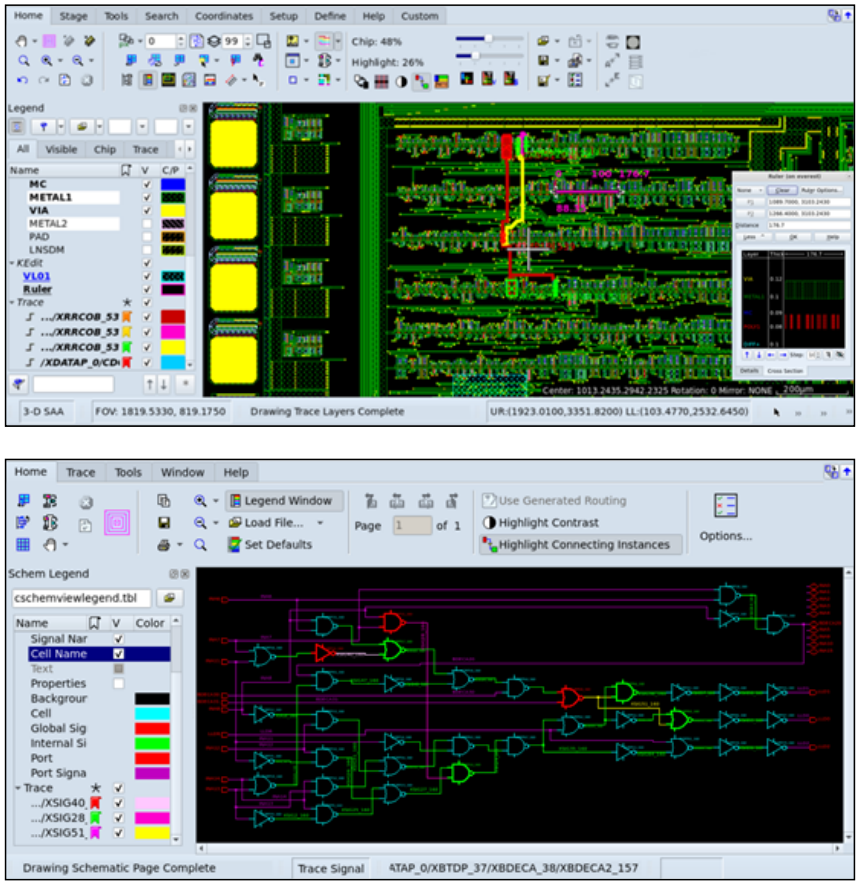

Figure 1: Avalon CAD-navigation solution integrating layout and schematic through signal cross-mapping

Supporting all CAD Design Data

Synopsys is committed to being the leading provider of software solutions that links all CAD design data. Avalon is a comprehensive package that reads chip design data from all leading EDA tools. The KDB™ database is designed to support key design formats which stores entire chip design data.

The following chip design data formats are supported by Avalon:

- Layout: GDSII, OASIS®.
- Netlist: SPICE, EDIF, Lef-Def and OpenAccess
- LVS: Synopsys (ICVTM), Cadence (AssuraTM, PVSTM), Mentor Graphics (CalibreTM)

Key requirements for Avalon users are faster data accessibility, CAD navigation support for diverse failure analysis equipment and availability of debug tools. Avalon provides the optimal solution for both small and continually expanding larger FA labs and design debug teams. The Avalon database is design independent and offers a superior level of data consistency and security. The unique design of the internal database schema guarantees compatibility with decades-old databases. This is an indispensable feature for all failure analysis, QA and manufacturing organizations especially in the automotive industry.

Providing Critical Analysis Functions

In addition to its CAD navigation and database capabilities, Avalon's analysis features have become indispensable to the FA lab. Different viewing options are critical in tracking potential failures and determining the source and origin of demonstrable defects. Avalon includes special schematic capabilities and layout features that are invaluable to FA engineers as they debug chips manufactured using new advanced processes.

Below are details for some of the most commonly used applications.

SchemView provides tracking of potential failures through visualization of the chip logic. By cross-mapping nets and instances to the device layout and netlist, SchemView helps determine the source and origin of chip failures. The entire design is displayed in cell hierarchy format, allowing viewing down to the transistor level.

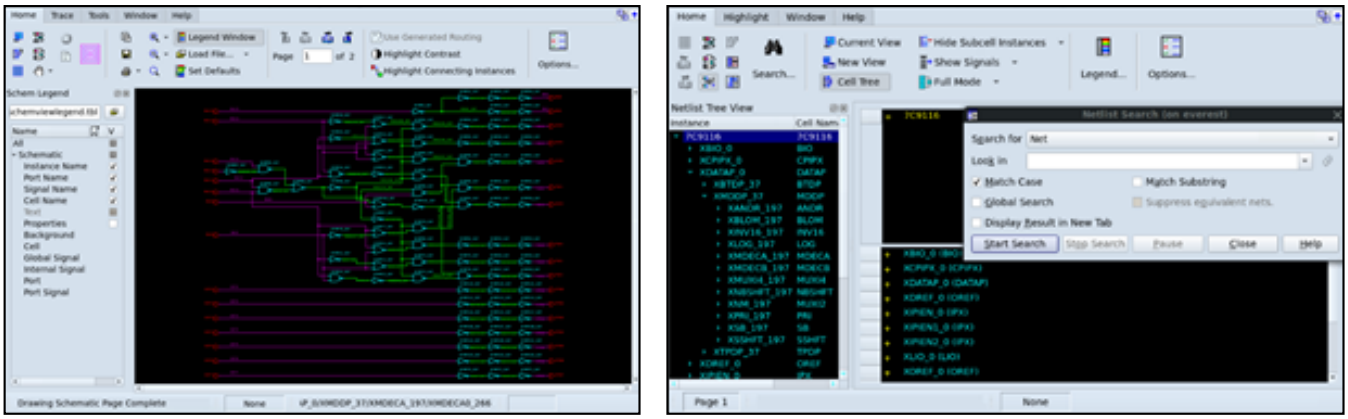

Figure 2: Avalon SchemView and NetView provide an easy way to navigate inside circuit schematics

Defect Wafer Map integrates defect inspection data with the device CAD design using the defect coordinates to navigate an equipment stage and pinpoint the defect for closer inspection and characterization. Avalon sorts the defects by size, location or class, as well as layout location and allows the user to define custom wafer maps. Additionally, users can classify defects, attach images and write updated information to the defect files.

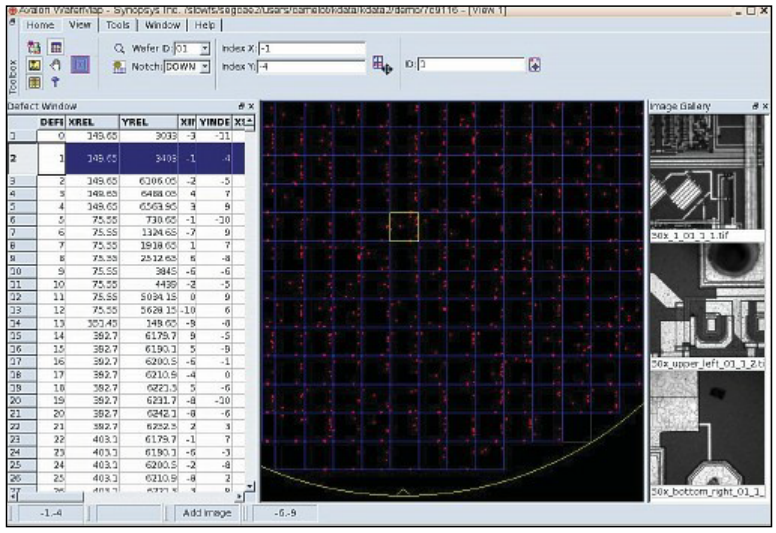

Figure 3: Defect Wafer Map pinpoints defects for closer inspection

I-SchemView (Interactive Schematic) creates a schematic from a netlist in a net-oriented format allowing forward and backward tracing to locate a fault. Features like Add Driver or Add Input Cone allow for quick analysis and verification of diagnostic results in scan chains.

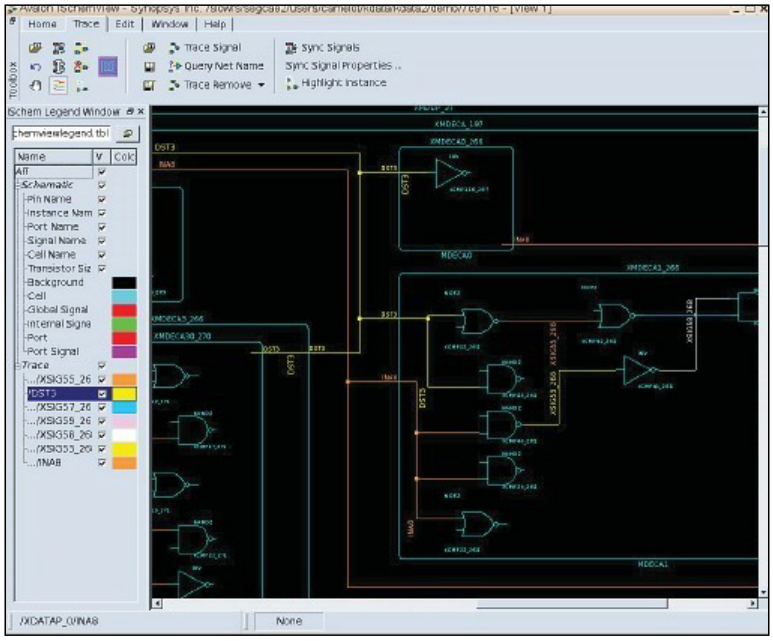

Figure 4: I-Schem creates a schematic from a netlist

Bitmap enables equipment CAD navigation when analyzing memory chips by identifying the physical location of failing memory cells. It eliminates tedious screen counting by converting the logical addresses, or row and column coordinates, to the physical location.

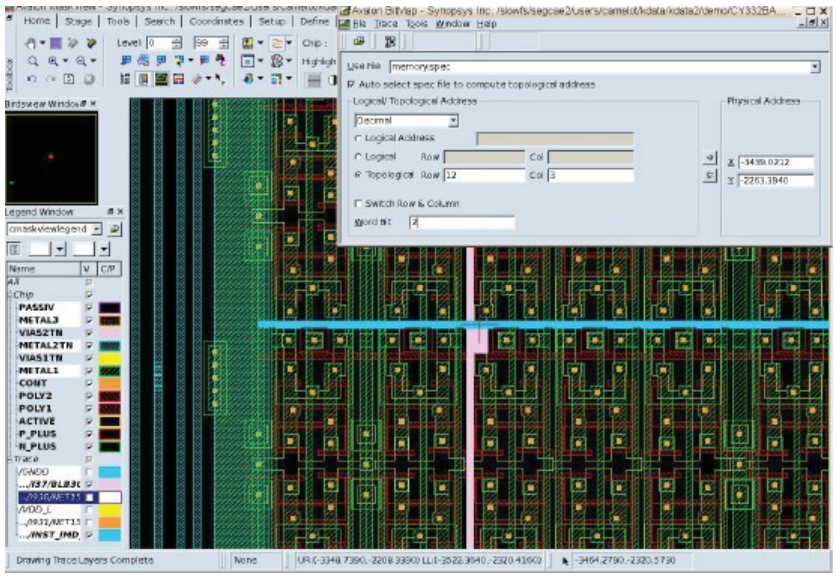

Figure 5: K-Bitmap identifies the physical location of bit addresses in memory devices

3D Small-Area Analysis provides a three-dimensional cross-section capability to FA engineers, enabling faster localization of circuit failures to accelerate IC manufacturing yield improvement.

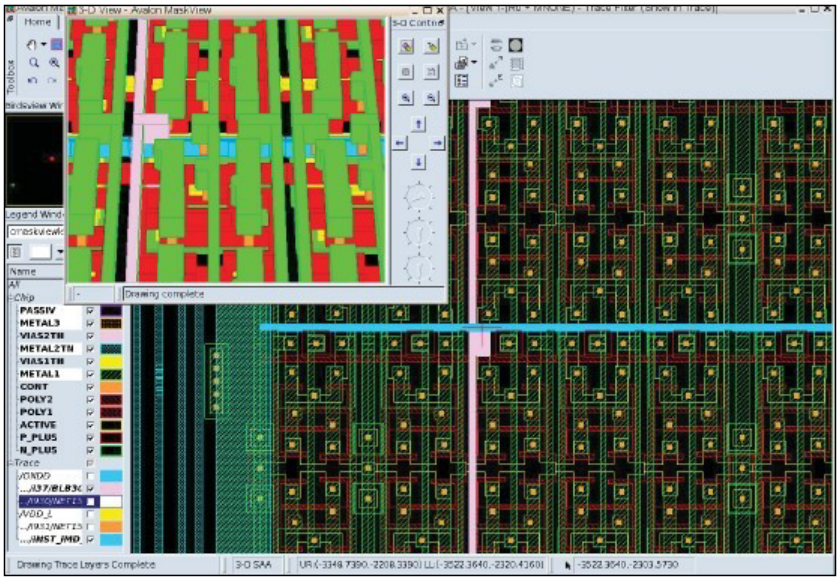

Figure 6: 3D Small-Area Analysis enables faster localization of circuit failures

Hot-Spot Analyzer allows users to draw regions on the layout that correspond to hot-spot regions (emission spots) to detect the crucial nets. It finds the nets in each hot-spot region and plots a pareto graph of nets crossing one or more hotspots which helps to easily locate the defective net.

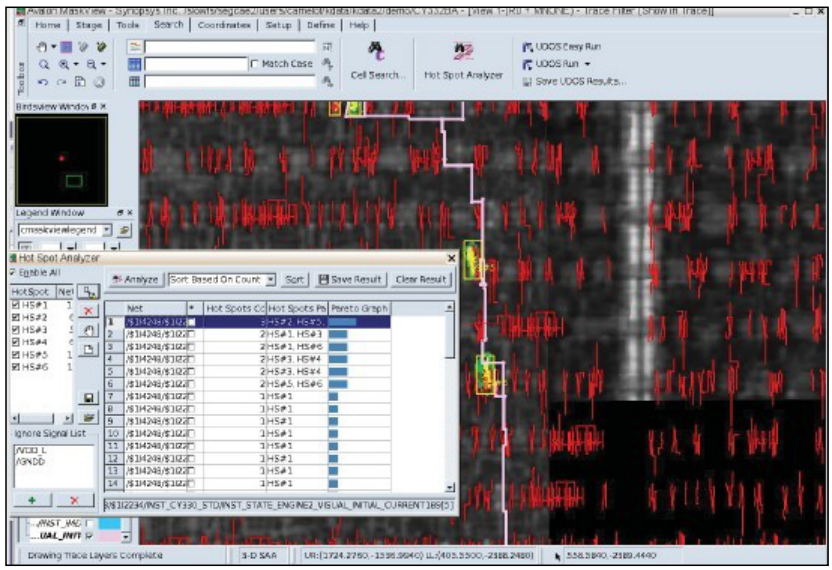

Figure 7: Hot-Spot Analyzer displays number of nets in a hot spot

User-Defined Online Search (UDOS) allows users to search a small area of a die for unique polygon features, repeated features or lack of features. Applications include, but are not limited to, FIB-able regions, repeaters, pattern fidelity and lithographic applications.

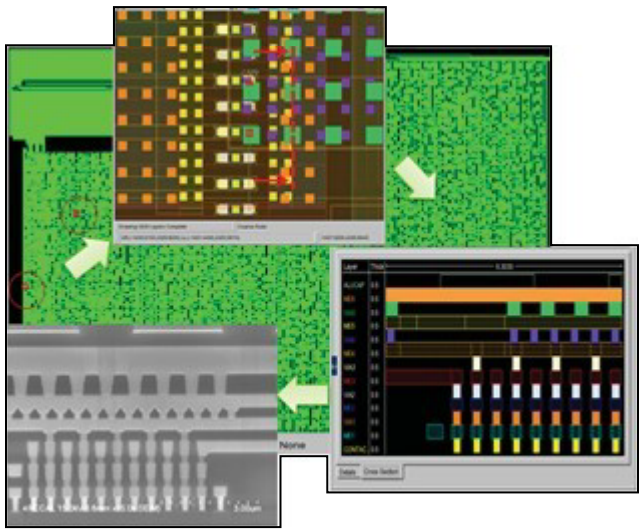

Figure 8: UDOS finds easy-to-access traces

Passive Voltage Contrast (PVC) Checker quickly and accurately validates the integrity of a circuit's conductivity and provides detailed information for identifying suspect faults at via or metal traces.

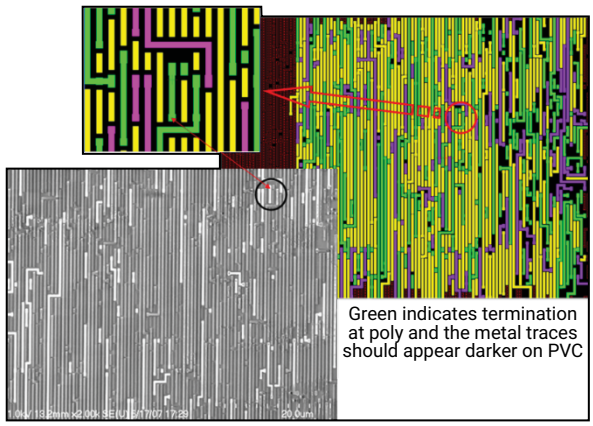

Figure 9: PVC Checker identifies suspect vias or metal traces

PathFinder enables the FA engineer to find a connecting path between two or more instances under analysis. The source of potential failing instances can be reported by diagnostic tools or can be instances under hotspots emitted by a photon emission microscope. ISchemView application enables the PathFinder capability to find the connecting path between such instances. The connecting path could be a direct connection or go through transmission gates.

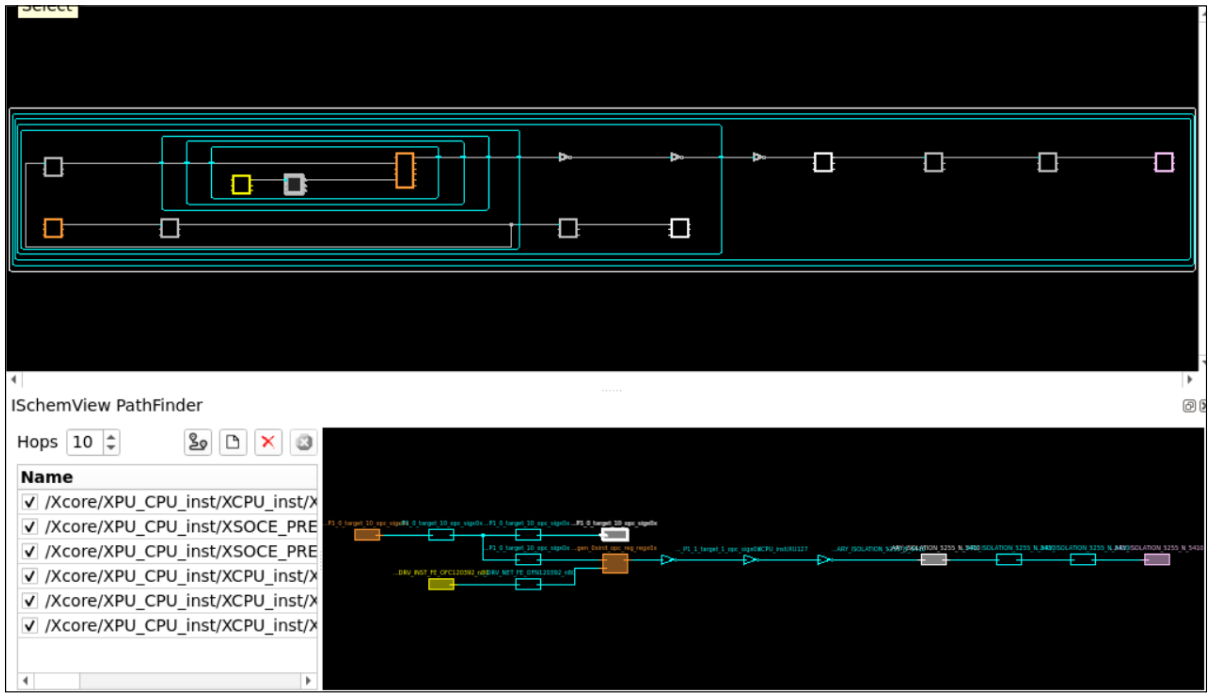

Figure 10: Connecting path found by PathFinder between selected instances

Electronic Virtual Layer marks objects that represent net connectivity during a FIB deposit or cut using KEdit. The online trace will simulate the new connectivity to the virtual layer. PVC checker could be used on this virtual layer to simulate the crack or short.

Export Partial Layout enables the customer to share partial layout data with service labs without compromising the IP of the product.

Advanced 3D Viewer displays a 3D view of the selected layout area. It shows each process step in the 3D view for which it uses the process data along with design data. It zooms into smaller details and helps to minimize unintended consequences during FIB cuts due to underneath high density structures. **Value Links** of Avalon with other products in the ecosystem enables seamless data transfer across products and improves efficiency of FA flow.

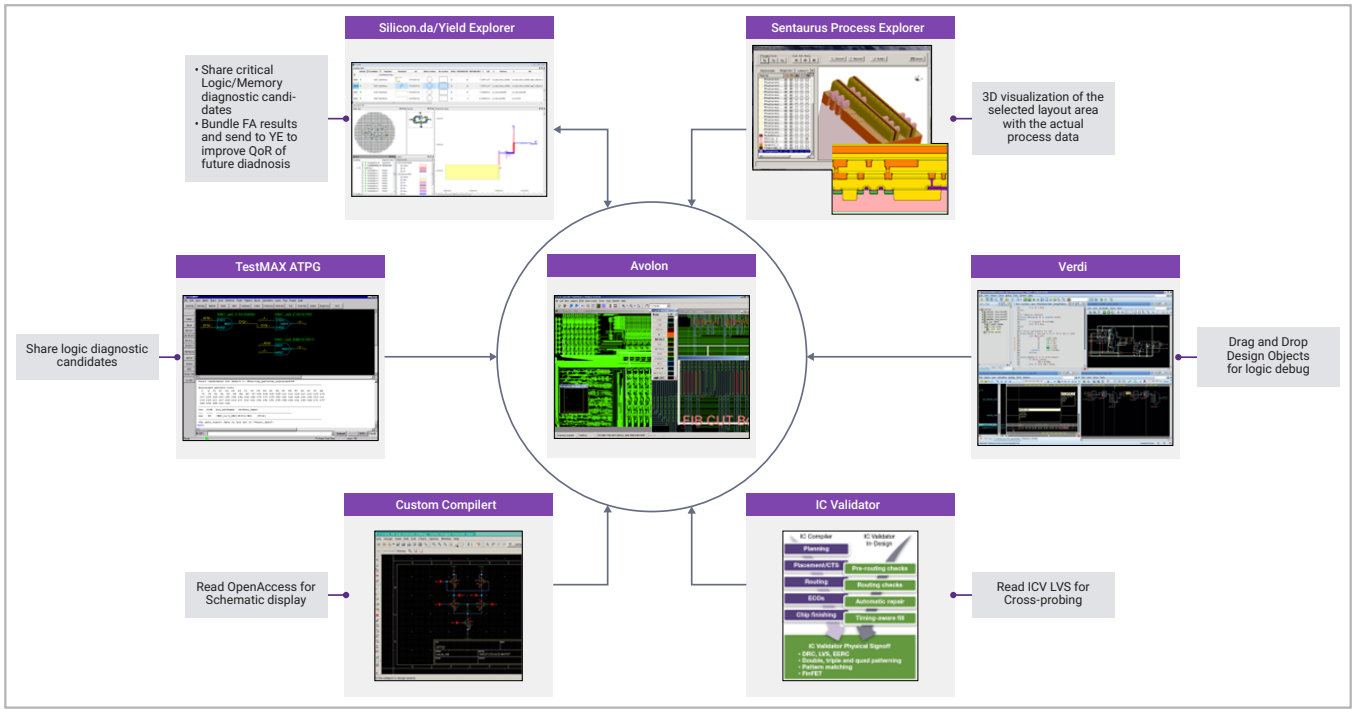

Figure 11: Avalon value links with Synopsys products in ecosystem

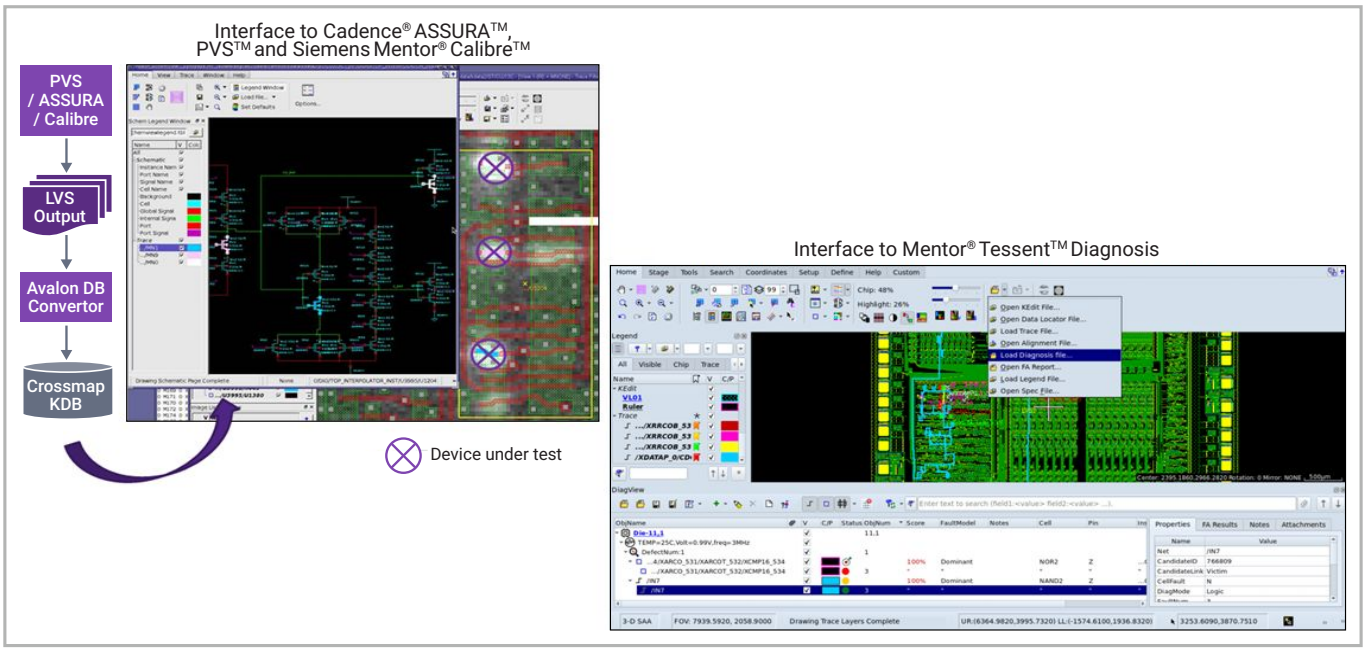

Figure 12: Avalon value links with external EDA platforms

Avalon—Silicon.da interface enables secured and seamless FAB—FABless Collaboration. The interface provides end-2-end solution to track and interact with FA results to reduce yield learning time. Correlation of diagnostics data with historical FA results saves time and expensive resources to perform FA.

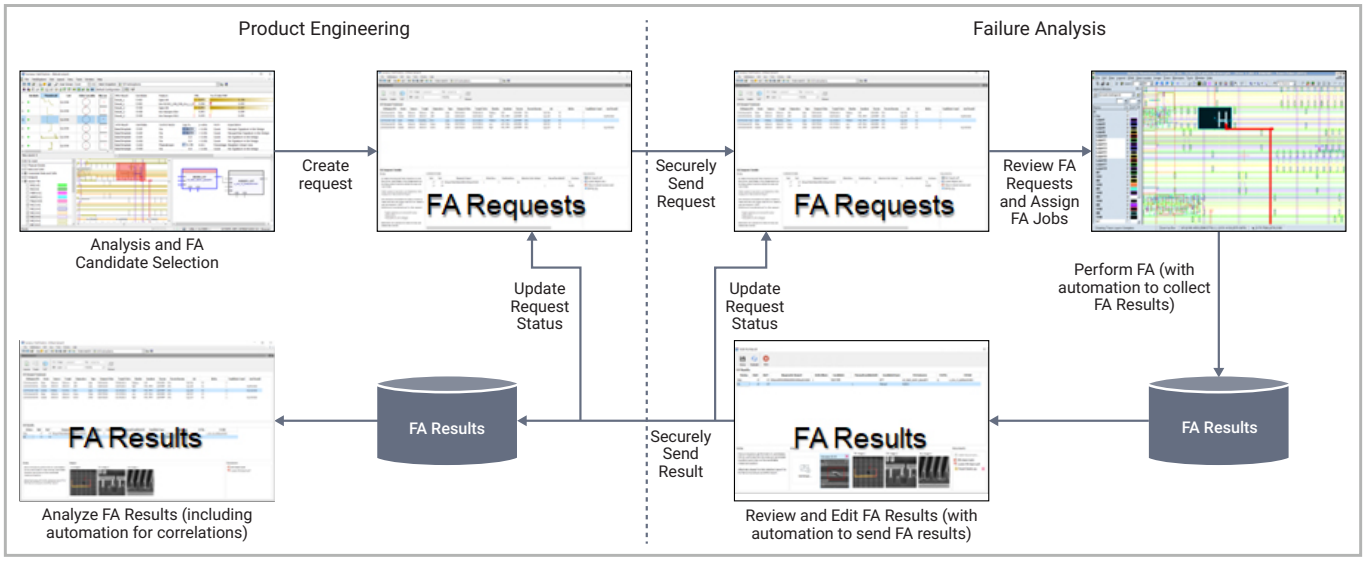

Figure 13: Secured and Seamless FAB—FABless Collaboration

PackageView extends Avalon™ die-level failure analysis capabilities to the packaging industry. PackageView integrates multiple, interactive IC and PCB designs with seamless CAD navigation capabilities. PackageView allows rapid signal tracing on dies, stacked dies, multi-chip modules and PCBs. The FA engineer can now trace a signal from chip to board, back to chip and then quickly navigate failure analysis tools to X, Y locations to determine the root cause of the failure. PackageView reads package design data from the KDB database generated using industry standard formats: ODB++ and Gerber RS 274X. PackageView provides access to many die-level failure analysis capabilities at the board-level including 2D cross-section, 3D view of selected small area, adding annotations, partial KDB export, etc. PackageView supports various surface mount technologies including TSV, Ball Grid Array (BGA) and Wirebond. PackageView uses an integrated system navigation database which allows the user to seamlessly trace signals across multiple heterogeneous components with by means of a singular net name.

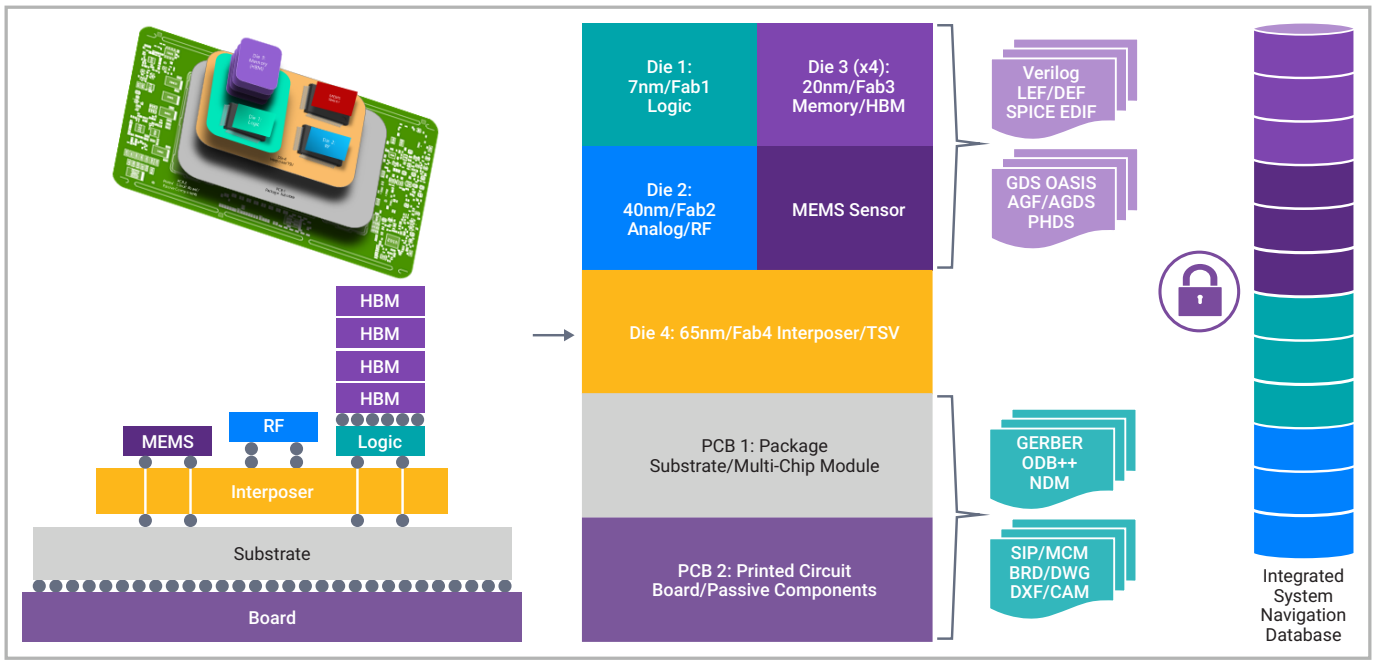

Figure 14: Homogeneous package KDB

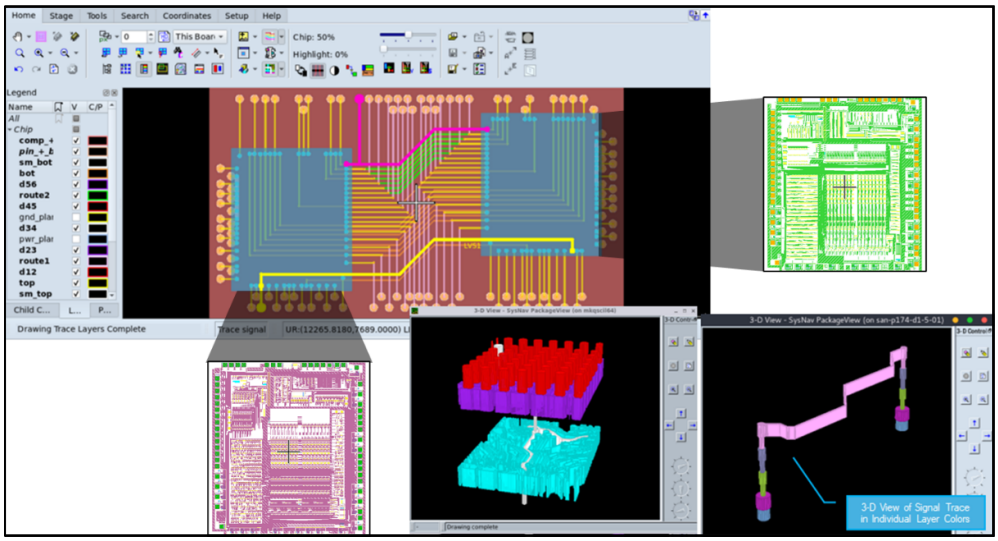

Figure 15: PackageView tracing the signals across dies and a 3D view of a small area

Comprehensive Library of FA Tool Drivers

Avalon provides navigation to almost every equipment used in an FA lab. With a continued commitment to support drivers for all types of test and analysis equipment, Synopsys will continue to develop driver interfaces for new tools as they are introduced to the market, as well as maintain the drivers for the next generation of existing tools.

Equipment Supported by Avalon

- Analytical Probe Stations
- Atomic Force Microscopes
- E-Beam Probers
- IR Imaging
- Mechanical Stage Controllers
- Emission Microscopes
- Microanalysis Systems
- FIB Workstation
- Laser Voltage Probe
- LSM
- EDA LVS
- Microchemical Lasers
- OBIC Instruments
- Optical Review
- SEM Tools
- Photon Emission Microscopes
- Laser Scan Microscopes