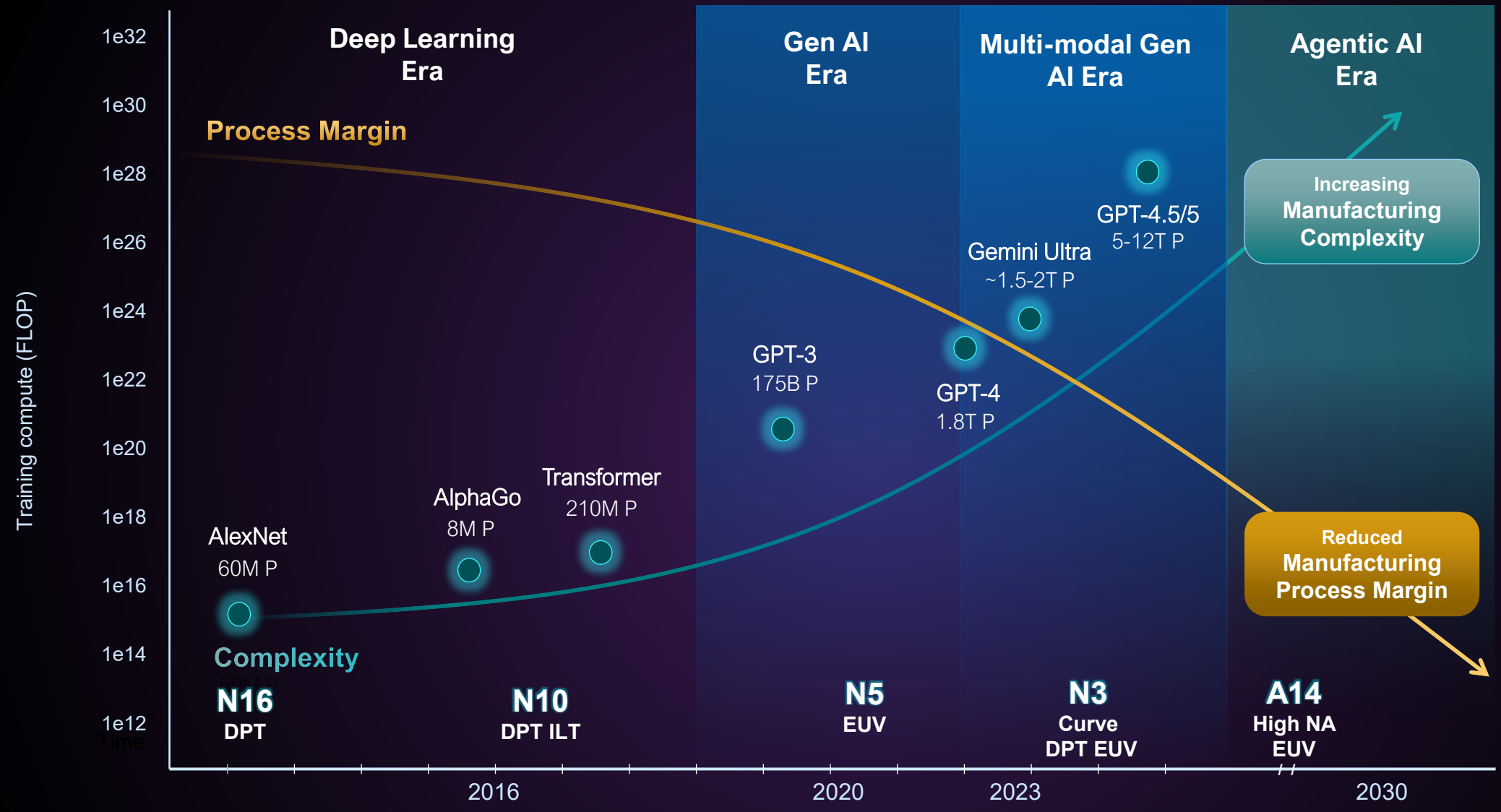
SYNOPSYS®

Scaling Computational Lithography with GPUs & AI

Michael Buehler-Garcia

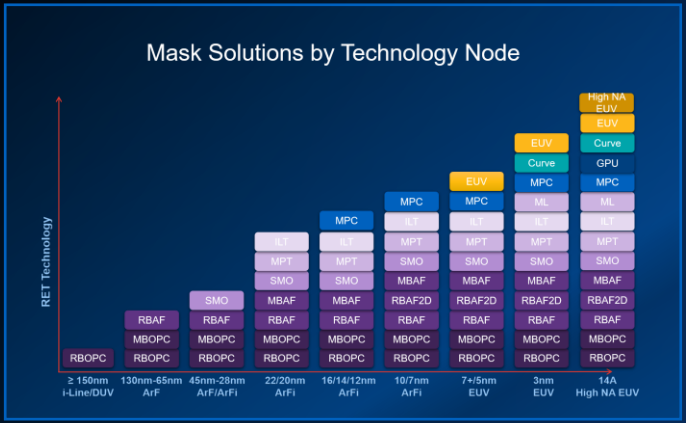
SVP, Synopsys Product Management Group

AI Driving Insatiable Demand for More Compute Power



Manufacturing Complexity Drives a Compute Inflection Point

Process Complexity

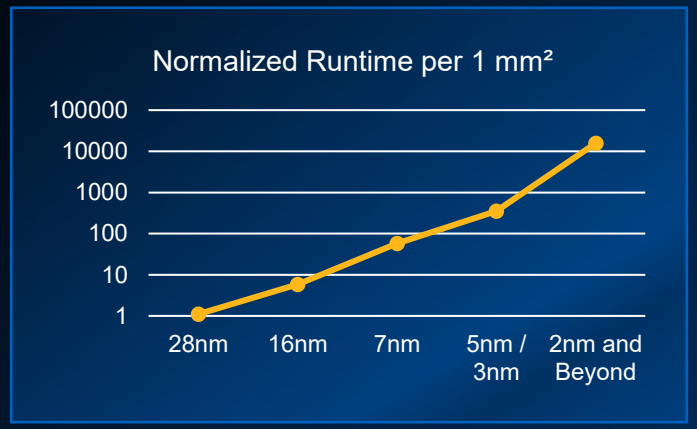


Process Scaling Continues to Raise the Bar for Correction

Physics

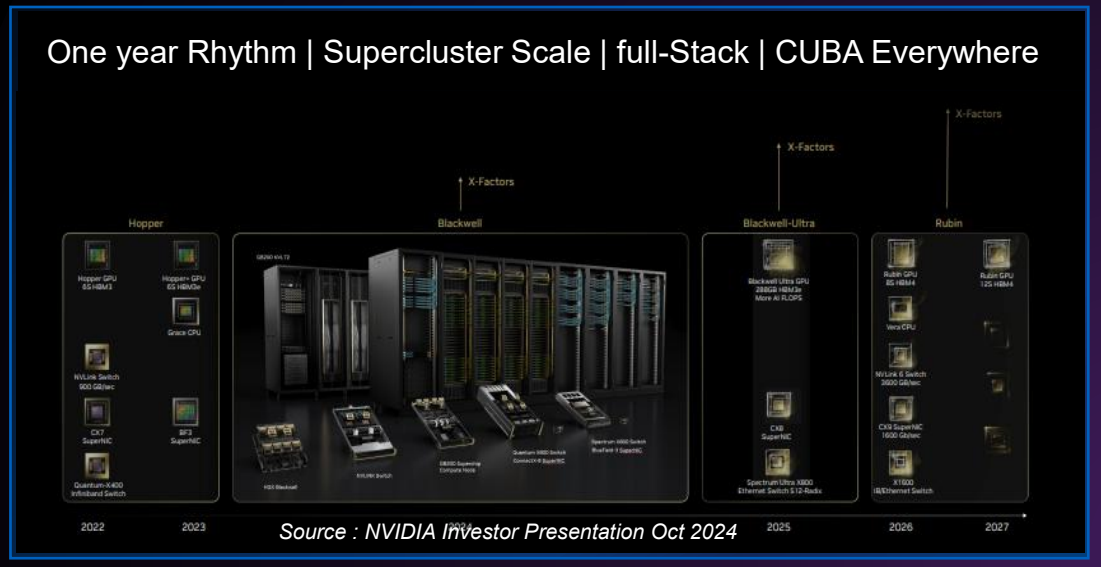
Predictive Simulation Complexity Is Growing Exponentially

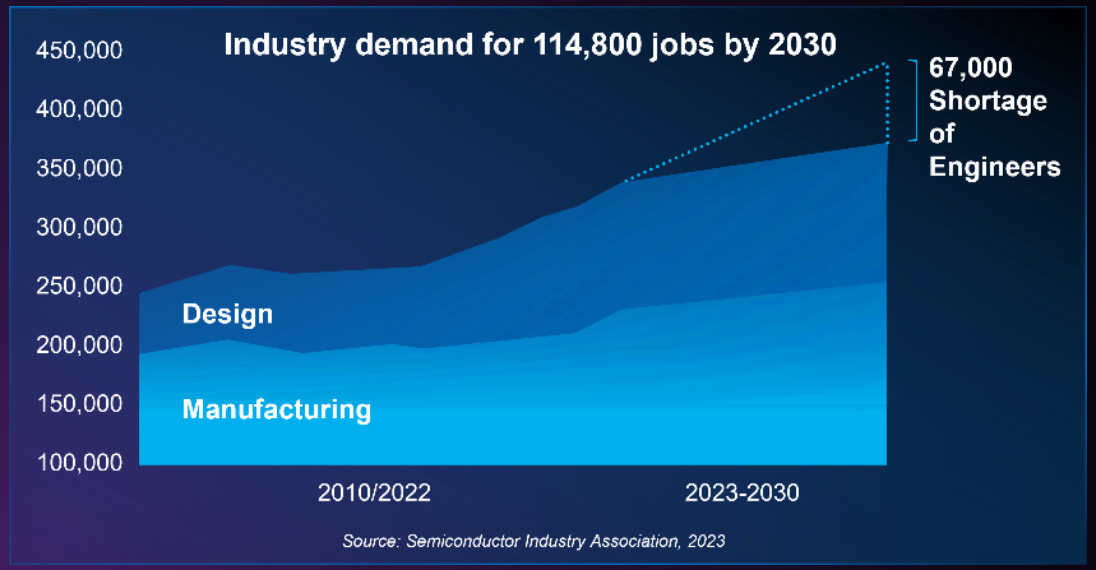
Computation



Compute Requirements Continue to Escalate

Compounded by Accelerated Cycles and Talent Shortage





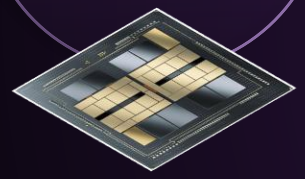
Limited engineering availability risks the shorter development targets

Rising Complexity, Shorter Design Cycles, Talent Shortage

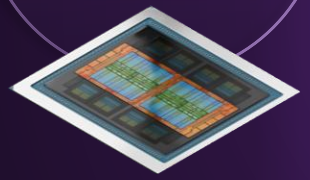
The Productivity Challenge

Rising Complexity

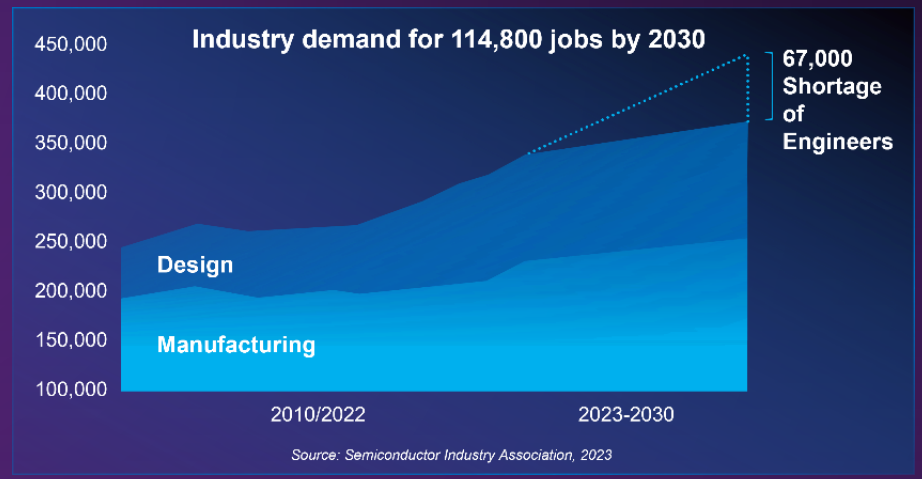
2023
Intel Ponte Vecchio
100B+
Transistors



2025
AMD Instinct MI350
185B
Transistors

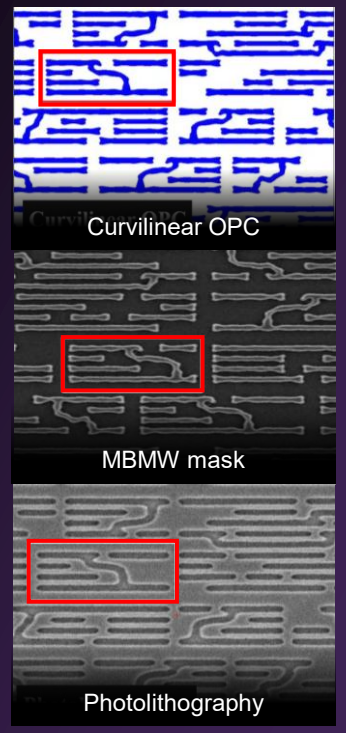


2026
NVIDIA Rubin
336B
Transistors



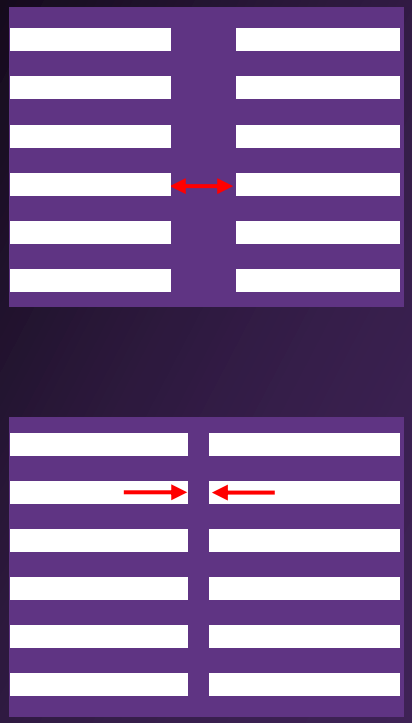
Innovation Is Accelerating — And It All Has to Be Corrected

Curved Designs for die shrink and COO reduction



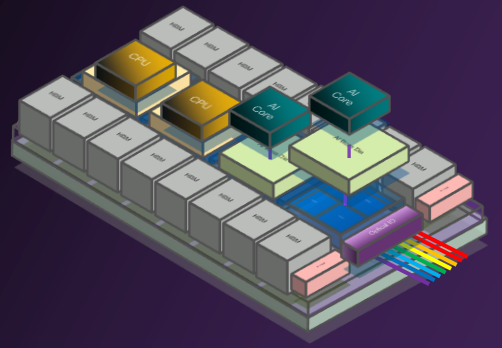
Source: imec

Directional Etch for Line End Control



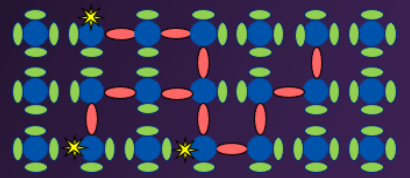
Source: AMAT

3D IC & Advanced Packaging Introduces Thermal and Mechanical Distortions



High NA Insertion Reduces DOF and Adds Anamorphic Imaging

Depth of Focus

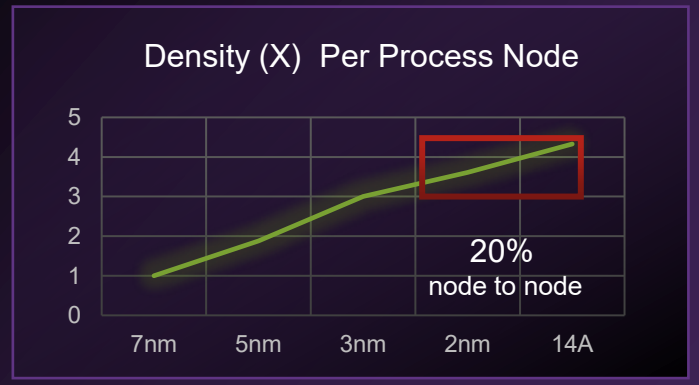


Metal Oxide Resists Introduce New Chemistry

Source: ASML Source: Inpria

Computational Lithography TAT Increasing Exponentially

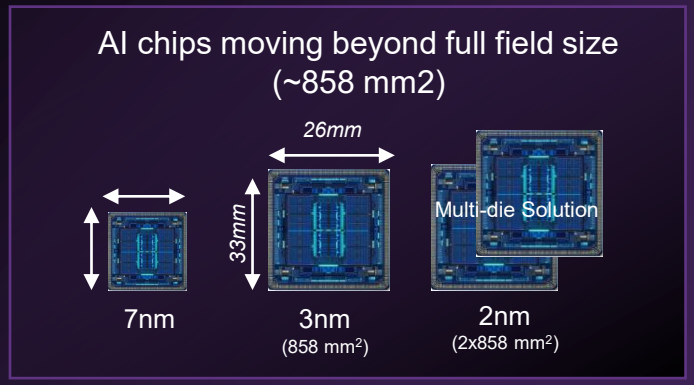
Rising Density



Every node advance enables denser designs that Require More Compute resources and Longer Runtimes

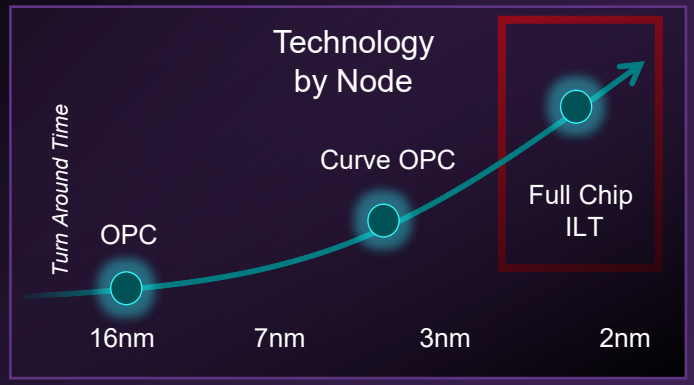
Source: TSMC

AI Designs Push Reticle Area Limits



Full reticle Designs have more pattern that requires More Compute resources and Longer Runtime

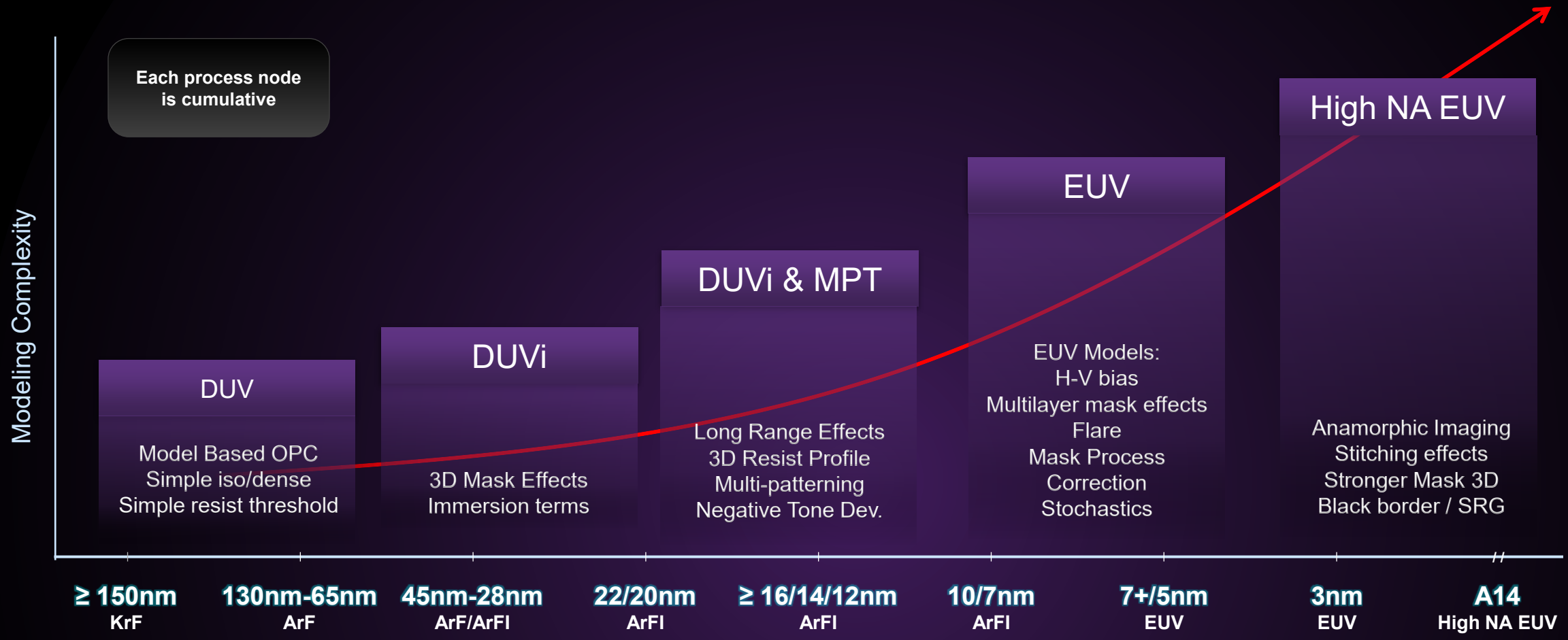
Rising Litho Complexity



Process Technology advances require more sophisticated models that need more compute

Chip design and process complexity demand more aggressive correction

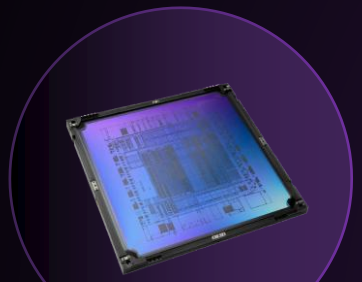
Every New Node Adds New Physics to Model

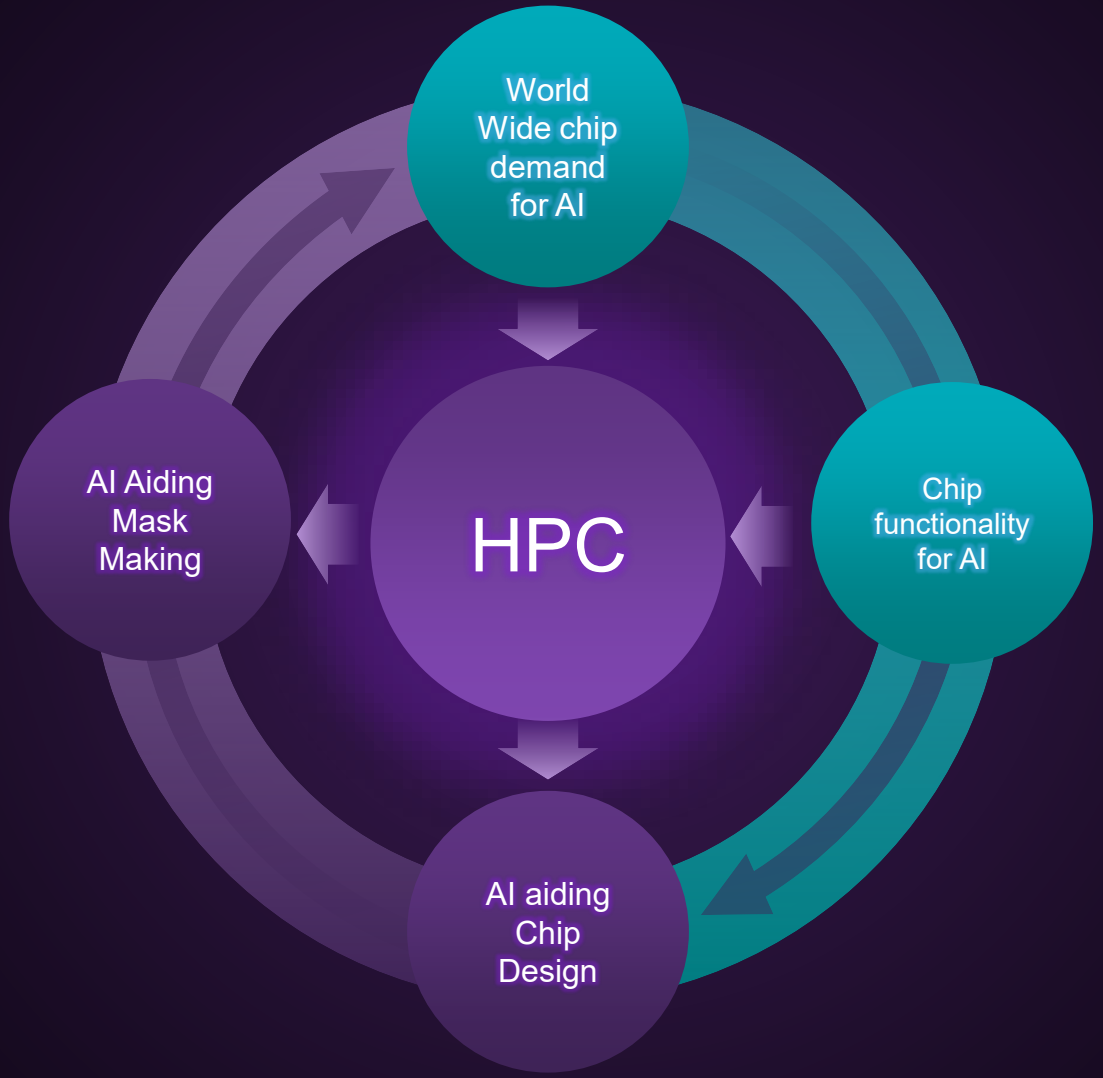


Predictive models require exponentially new physics effects for every nodes

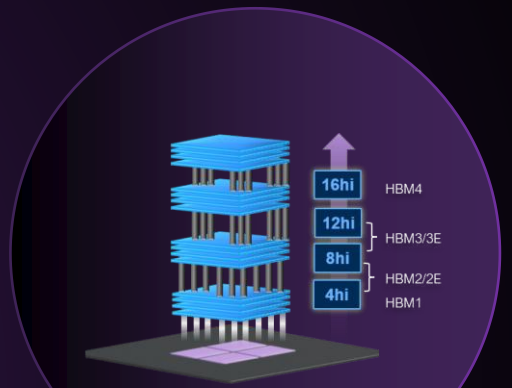
Computational Lithography uses AI to Build AI

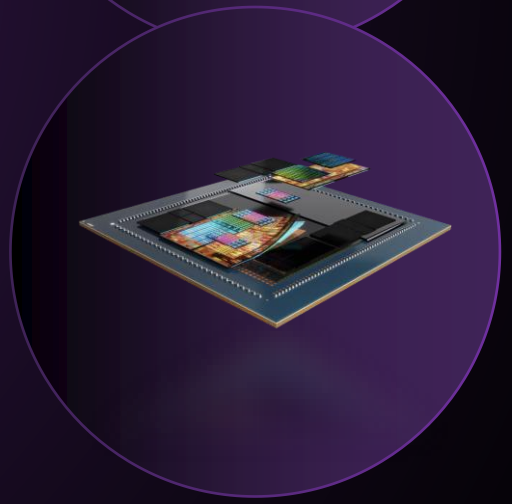
AI Applications





AI Infrastructure

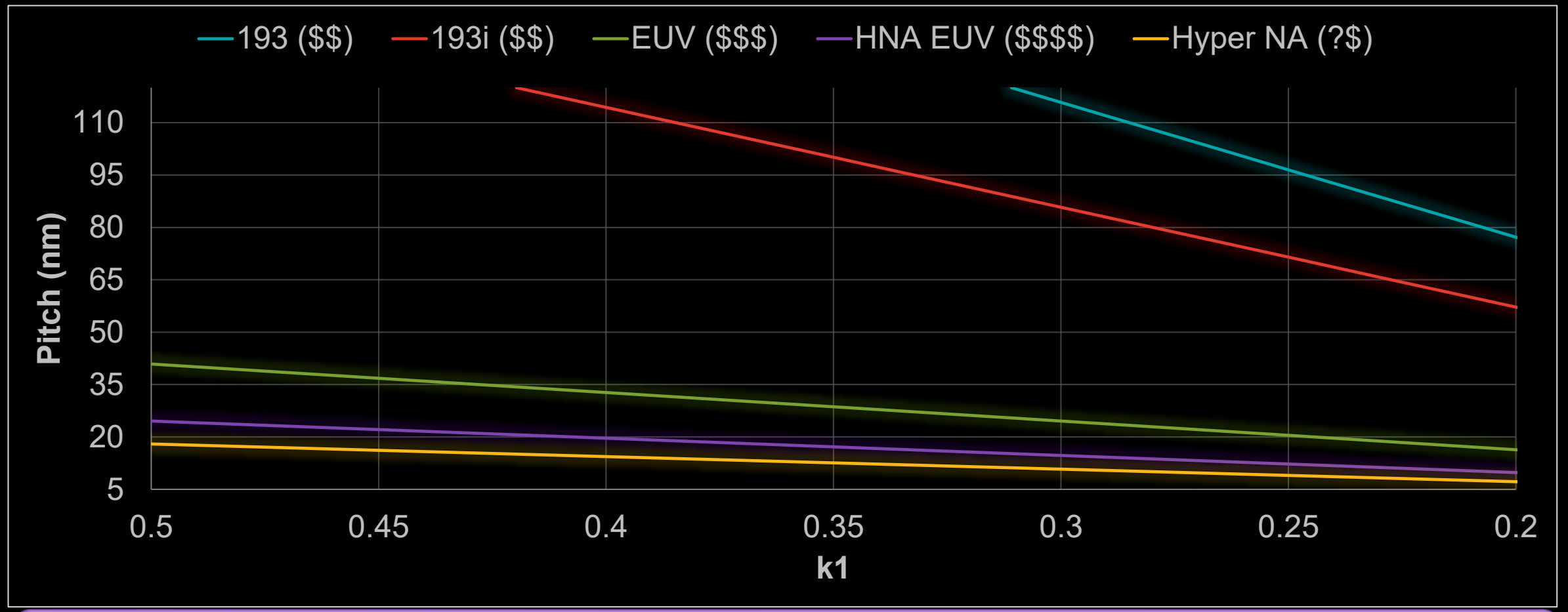




Pattern Structures Drive Mask and Computation Complexity

Introduction Year - Standard	1996 	2002/2005 	2022 – moving into production 
Pattern Class	Manhattan	Piecewise Linear, Curvilinear	Parametric Curve, Multigon
Application	Straight lines at constant angles	Curved lines from straight line segments	Continuous curved edges using Bezier representation
Correction Technology	Manhattan model based OPC	Curve OPC or ILT	Curve OPC or ILT
Impact		Increased file size, reduced MRC constrained areas	Reduced file size, less MRC constrained areas

Correction extends low-k1 Patterning without cost of new hardware

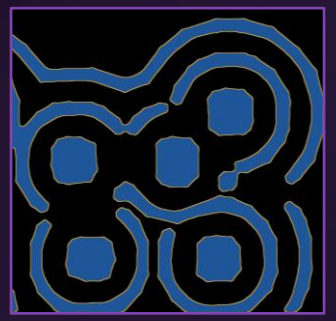


Correction Solution	RB OPC ($)	MB OPC ($)	SRAF ($)	ILT ($)	MPT($$)

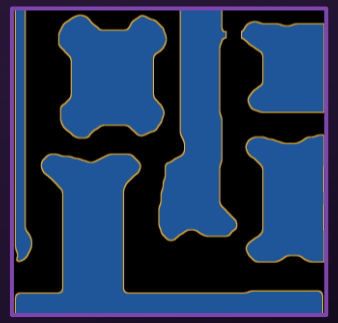
Each step in correction — Rule Based OPC to Model Based OPC to SRAF to ILT — buys another node of low-k1 patterning at a fraction of the cost of Multi-Patterning (MPT) or the next scanner generation.

Curvilinear Correction is Required to Maximize Process Margin

Curves Enable Correction Freedom



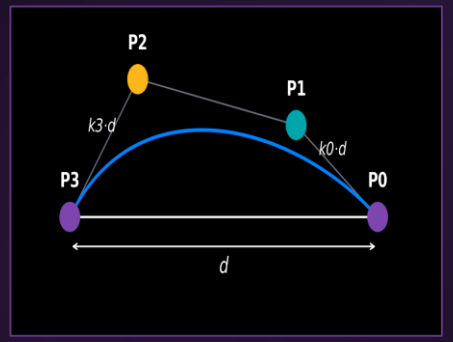
Inverse Lithography Technology



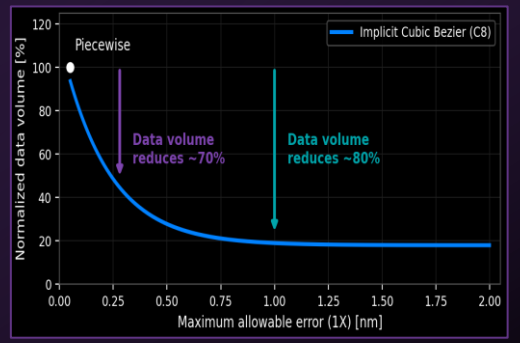
Curvilinear OPC

Curvilinear masks maximize process margin

Data Volume Increase due to Curves



Bezier Curve

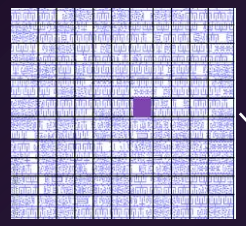


Bezier Curves Reduce Data Volume

Multigon polygon representation reduces data volume

ILT Enables Continued Pitch Scaling

ILT Repair

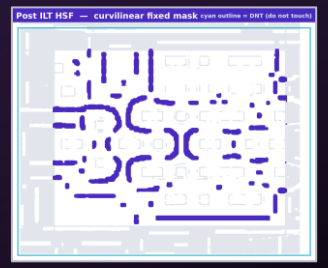


Surgical fix and blended into original design

Detected Problems

Pre ILT Repair

Initial Corrections in Magenta

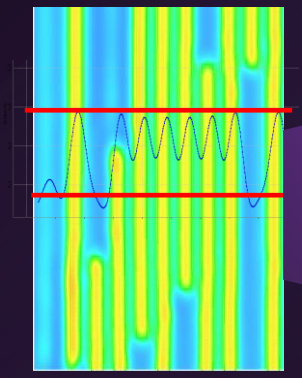


Post ILT Repair

ILT Repairs in Blue

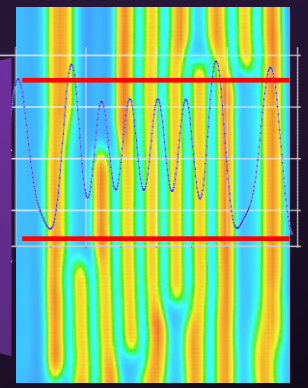
Hotspot repair enables tighter pitches

Full Chip ILT



OPC: Low Contrast

ILT Improves pattern fidelity



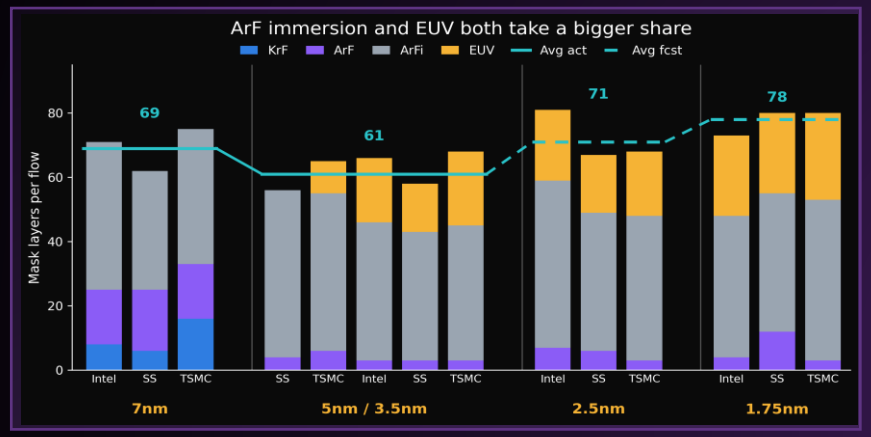
ILT: Improved Contrast

Full chip ILT Improves contrast for full chip

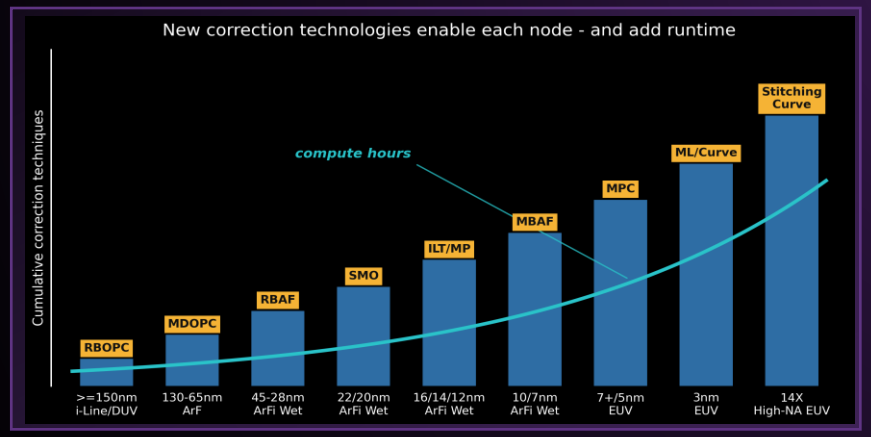
Compute Demand is Rising - GPU Economics Level the Field

Demand

more masks, more physics per node

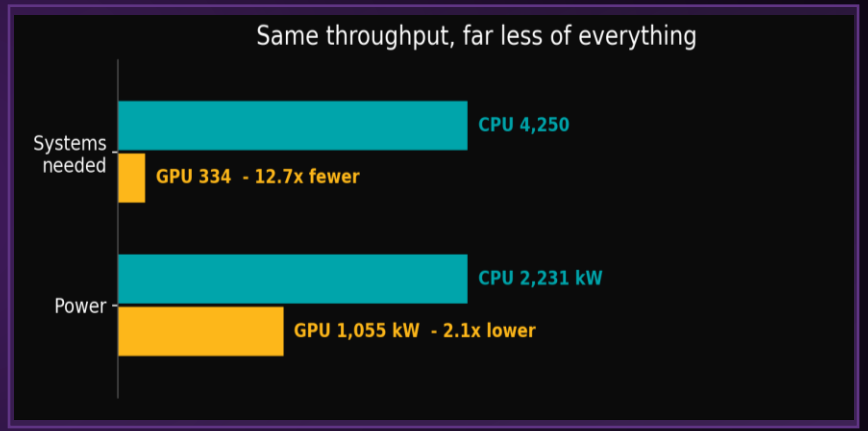


Source: TechInsights



Economics

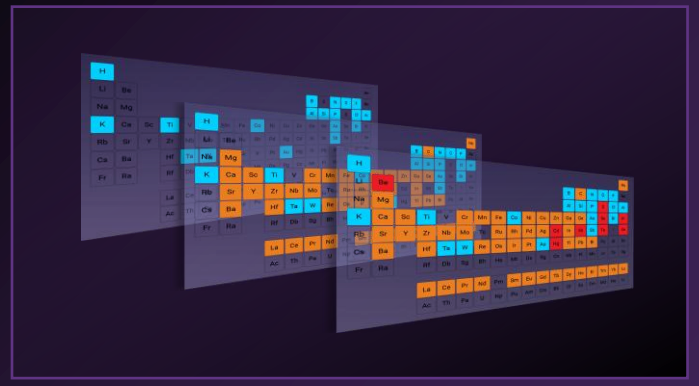
the GPU vs CPU premium is disappearing



Breaking Down Silos: Cross-Domain Expertise for Every Engineer

From Siloed Experts to Orchestrated Intelligence

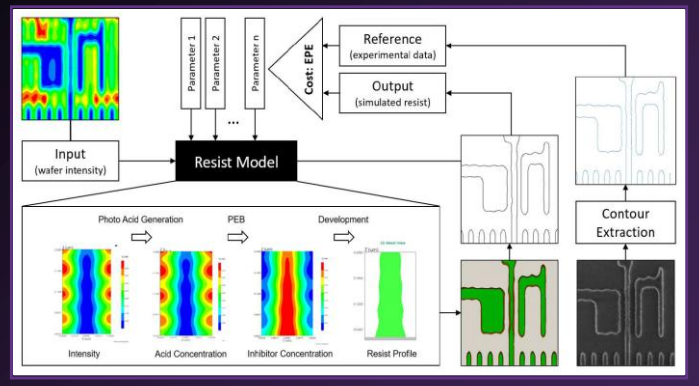
Material Expert



Modeling of atomic interactions
Material characterization

Material Model

Simulation Expert



What are the lithographic parameters for these materials?

Resist Model

Patterning Expert

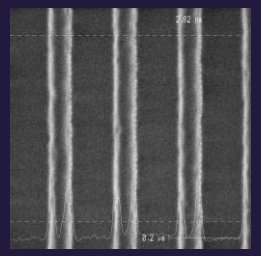
What patterning strategies provide the best yield?

Patterning Model

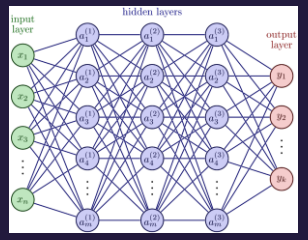
Agentic AI Orchestration Across Domains

Trusted AI, Grounded in Physics

Human-accessible flows and rigorous simulation keep AI results trustworthy

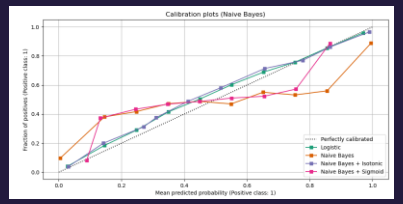


Measurement Data

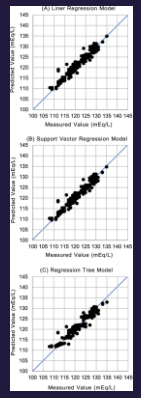


Model Form

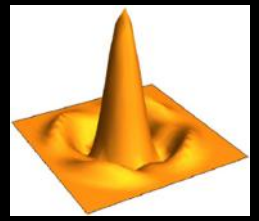
Human Accessible



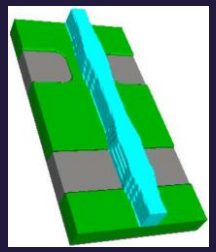
Model Calibration



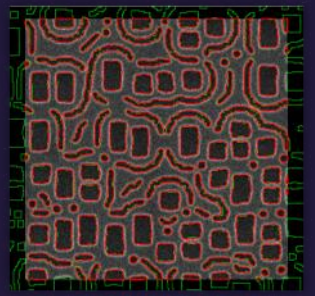
Model Validation



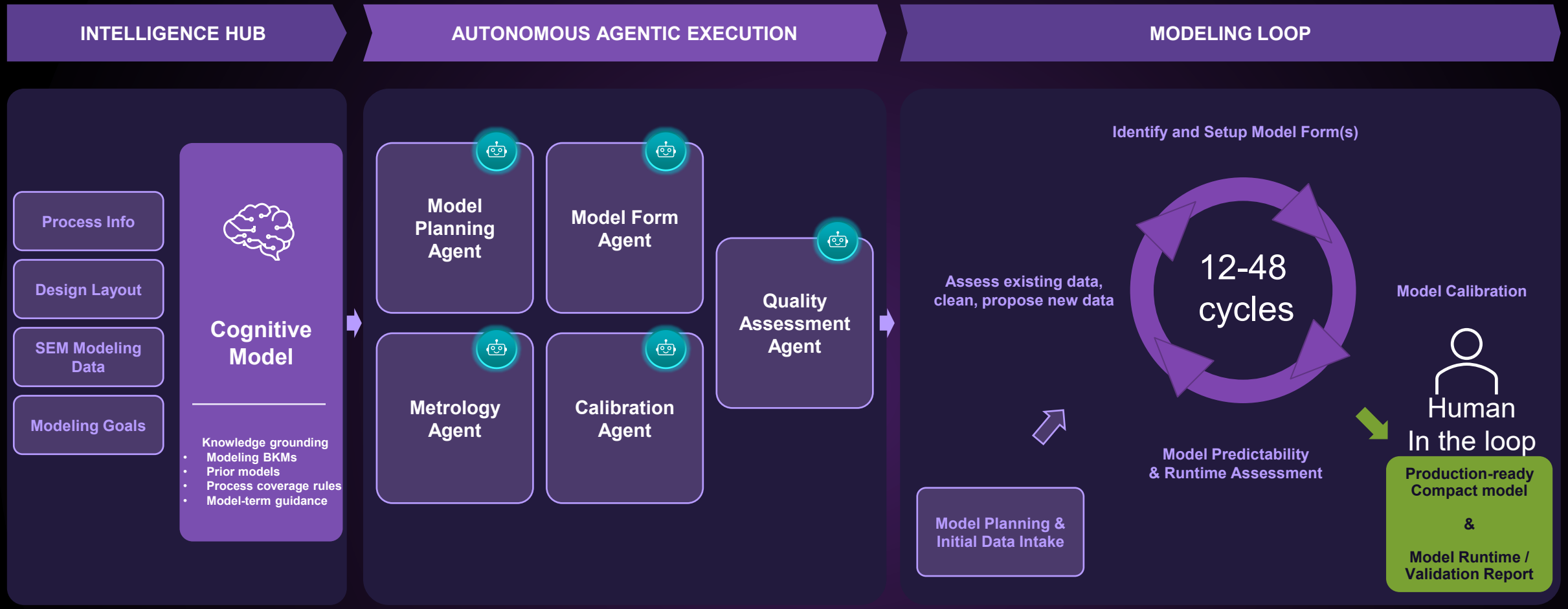
Process Model



Rigorous Validation



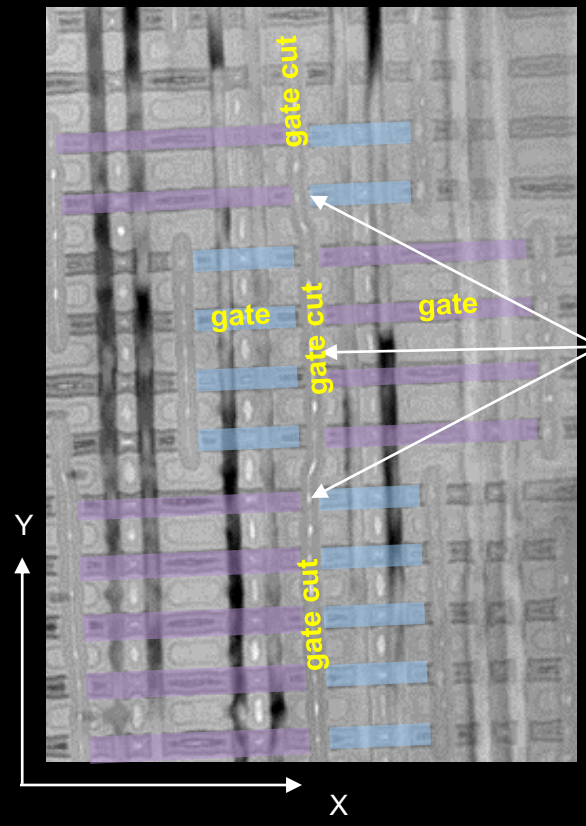
Every Engineer Gets an Expert Modeling Team



Value Enabling Increased Engineering Productivity with Faster, Higher-Quality Model Deployment

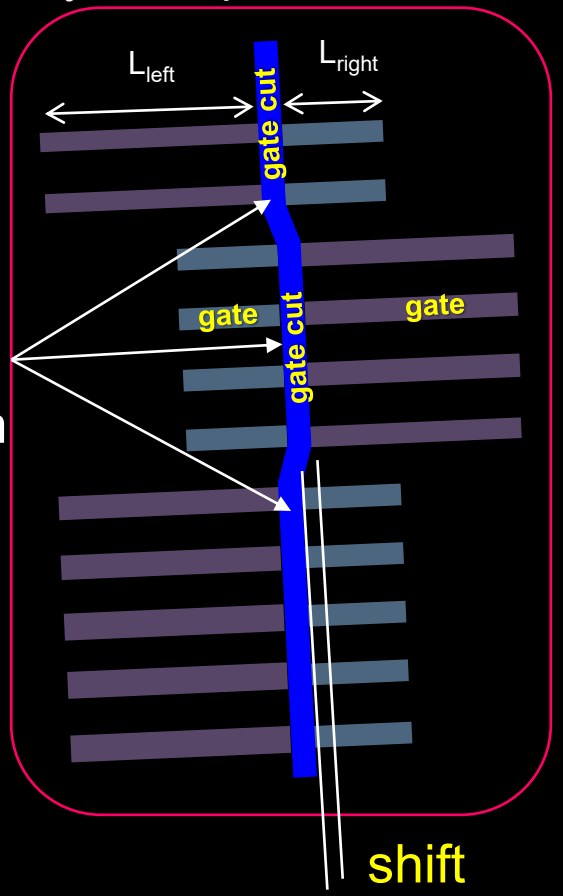
Mulitphysics Example: Stress Analysis leads to OPC Solution

TEM Impacted Area

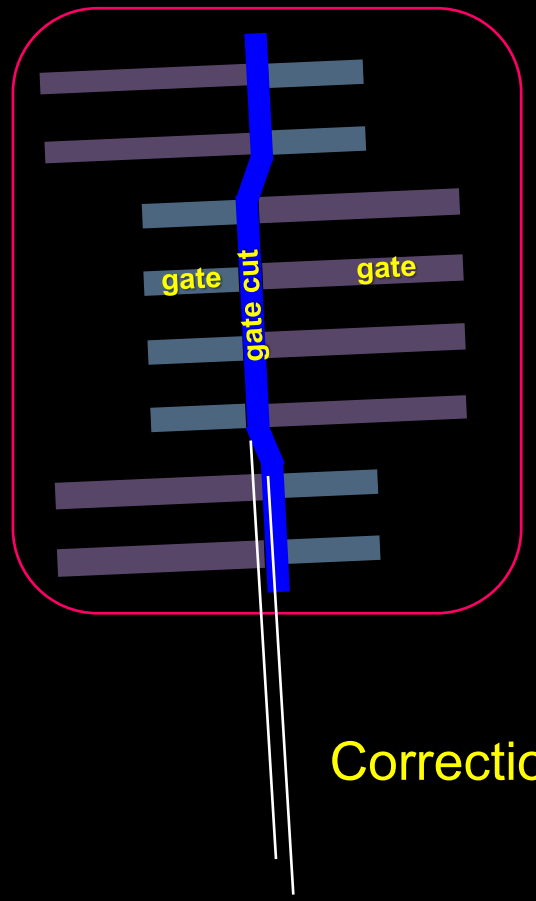


Gate cut trench distortion

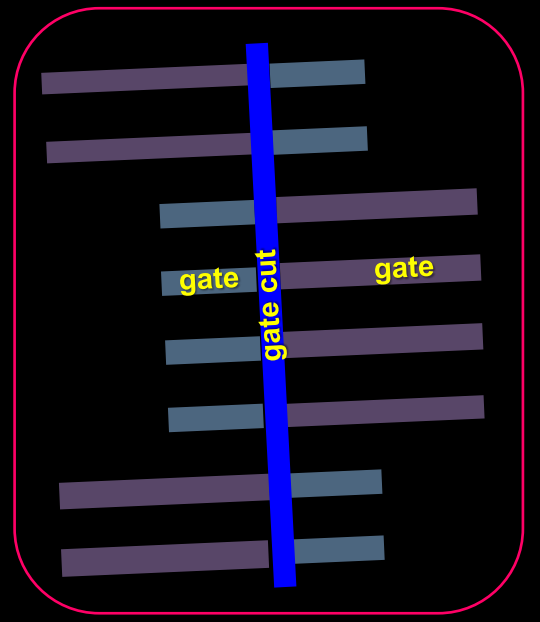
Layout Impacted Area



Stress Correction



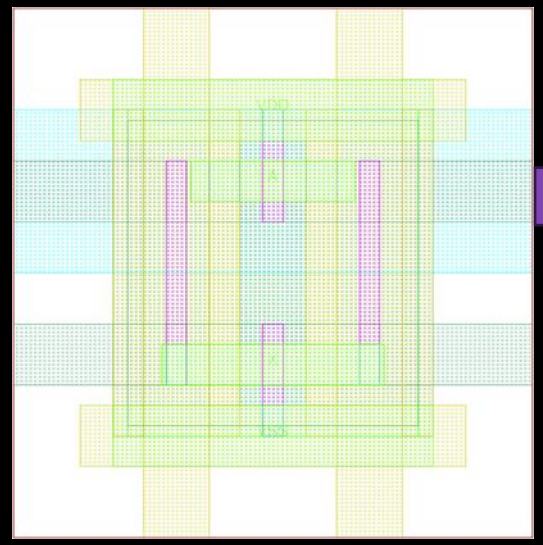
Stress Compensated



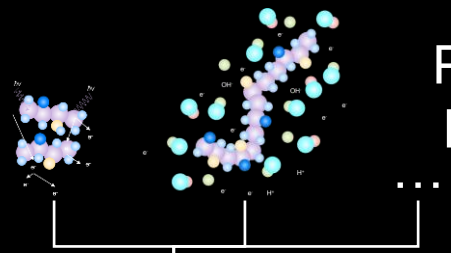
Multiphysics are increasingly important as product yield depends on integrated systems

TEM images from TechInsights

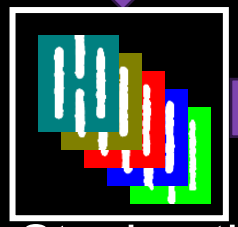
Process Models Work Together to Accelerate Development



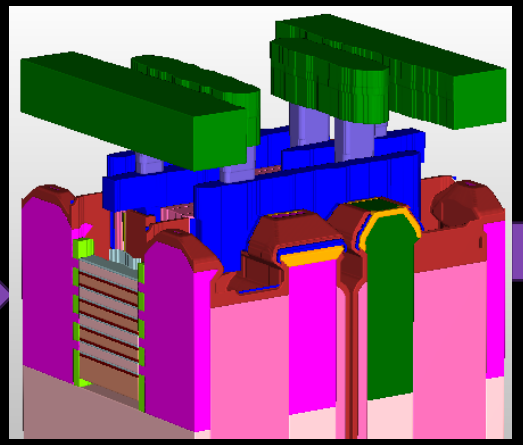
Device Design
Inverter



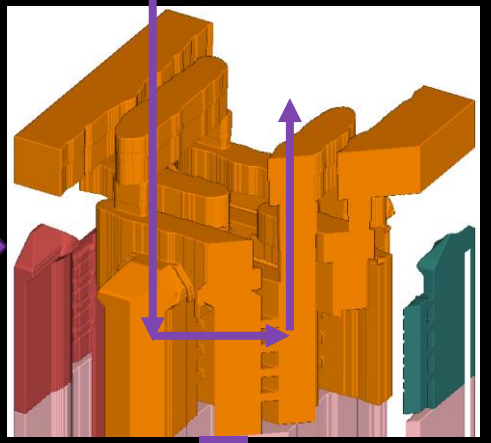
Process
Models



Stochastic
Outputs

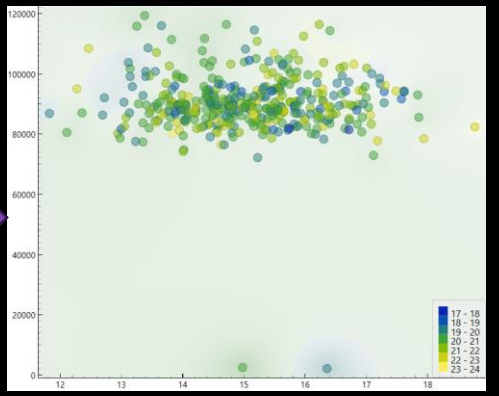


Virtual Device



Electrical Testing

Inline and Electrical
results across replicates



Computation Lithography with Agentic Workflows

Simulations beyond lithography are required to address decreasing process margin

GPU will aid TAT from the added computational burden

AI will aid optimizing these adjacent physics in an increasing complex system

			Value
Correction Agent	Correction Workflow OPC, ILT	Recipe creation, optimization, model integration	Improving process window
TCAD Agent	TCAD Agent Etch, Electrical, CMP, …	Stress analysis, thermal analysis, 3D IC, optical integration, device performance …	Improved process window and device performance beyond lithography
Verification Agent	Verification Agent DRC, MRC, LRC, Electrical, …	Process impact analysis, mask readiness,	Faster validation and disposition

Synopsys Pioneering AI-Powered Solutions Across The Full Stack

AI-powered

Hyperconverged

- Systems Architecture
- Design Capture
- Verification
- Implementation
- Signoff
- Test
- Manufacturing

Mask Optimizer

- Mask Space Optimization
- Pattern Data Analytics

Reinforcement Learning

AI as an Optimizer

Generative Assistant

Assistive	Creative
Run Assistance	Pattern Creation
Workflow Assistance	Model Creation
Knowledge Assistance	Recipe Creation

Generative AI / LLMs

AI as an Assistant

Agentic Coworker

Agent

AI as a Coworker

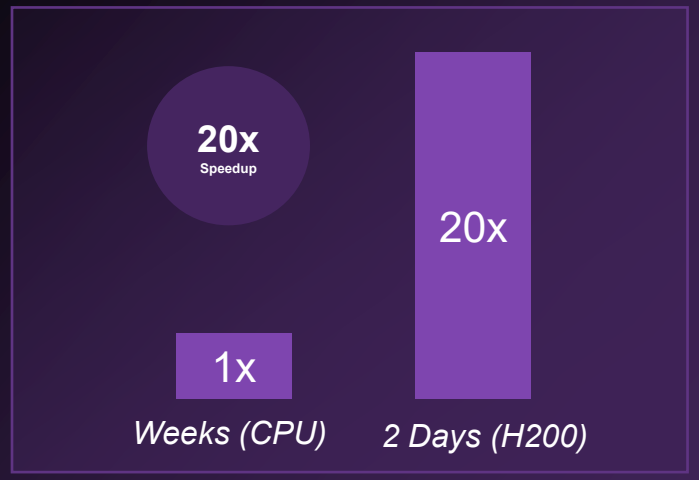
Impact of AI use across Synopsys EDA

Design	28nm Image sensor — 12% Area Shrink	4nm Mobile SoC — 25% Lower Power	FinFET CPU — 20% Faster TAT
Verification	HPC — 2X Tests Reduction	Automotive SoC — 15% Coverage Boost	CPU — 2X Faster TAT
Test	Mobile — 45% Pattern Count Reduction	Systems — 18% Pattern Count Reduction	Graphics — 25% Pattern Count Reduction
Manufacturing	Mask Recipe Tuning — 7X Productivity	Process Window — 44% Better Process Window	SMO TAT — 3.5x Faster TAT

Exemplary improvements found with AI applied to Synopsys cases

GPU-accelerated OPC/ILT enables highest throughput

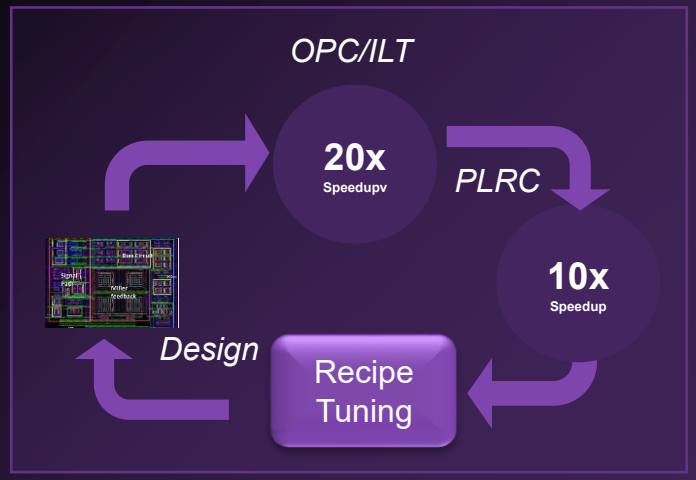
Increased Throughput



Reduce time to wafer with fastest time to results

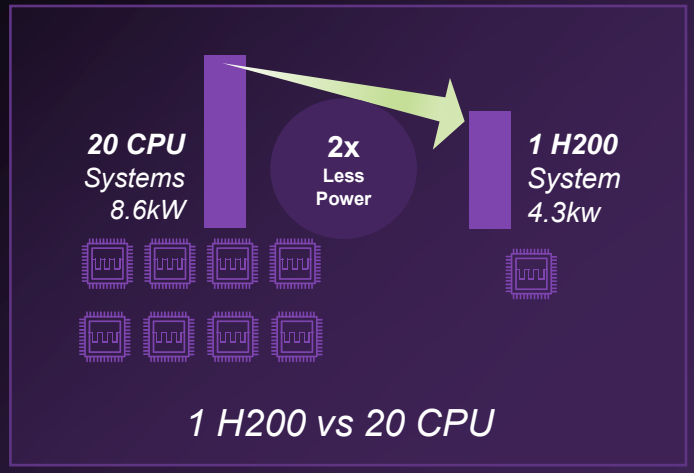
Cuts turn around time from weeks to days → 80k CPU cores to 250 GPU systems

Faster Recipe & Model Development Time



OPC/ILT/PLRC 10x Acceleration Reduces Process Ramp

Reduce Data Center Size & Power

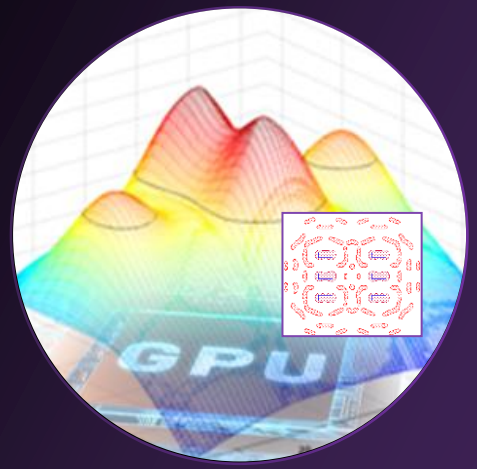


GPU Provides equivalent performance at 2x less power

GPU enables aggressive OPC & ILT production schedules

Synopsys Accelerates Time to Results with Higher Quality

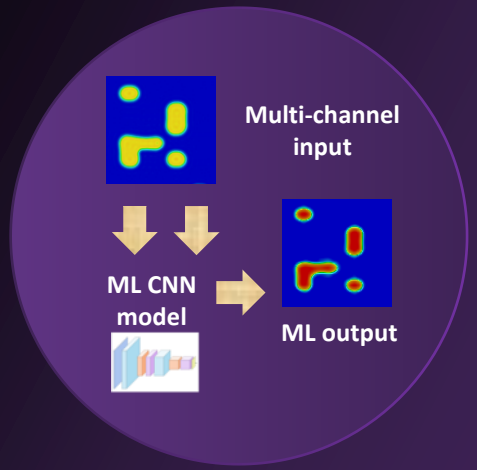
Full Chip ILT Enablement



GPU ILT Market Leader

20x acceleration and highest fidelity curve masks

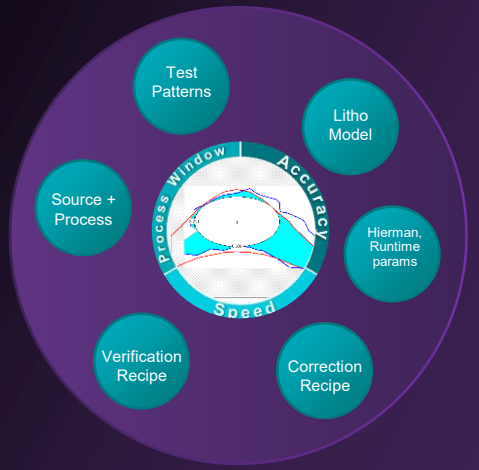
Predictive Machine Learning Models



Industry Proven ML Applications

Significantly improving quality of results

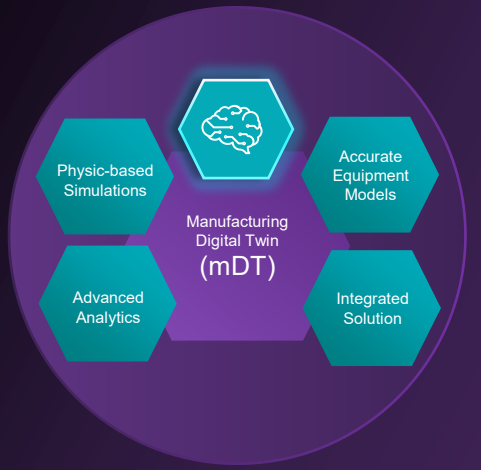
AI Driven Mask Space Optimization



Market Leading AI Solution

Higher efficiencies / Lower resource requirements

Manufacturing Digital Twins



Emerging Virtual Fabrication Workflows

Lower Cost / Faster Development

Synopsys Vision for Agentic AI and HPC in Mask

AI + GPU Enabling Tighter Manufacturing Specification

ML Models for OPC & ILT

ML ILT for faster TAT

Full Chip Rigorous ILT

AI Enabling Development of Computational Lithography

Correction Recipe Optimization

Pattern Selection

Multiphysics Grounded Truth Validation

Agent Improving Orchestration across Domains

Multiphysics integration into computational lithography

TCAD & Process exploration

Circuit Simulation

Material Exploration