SYNOPSYS®
Silicon to Software™

Tool and Methodology Consulting

Highlights

- Apply the latest tool features and methodologies to address specific design challenges like power, signal integrity, FinFET modeling and double patterning
- Advance your design methods and practices through project-based assistance
- Accelerate your learning curve with new Synopsys technology

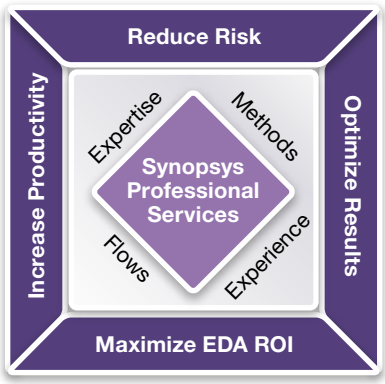
Take Advantage of Technology Leading Chip Design Tools and Methodologies

Synopsys customers realize how important it is to maintain a leading-edge chip design environment. To maximize an investment made in Synopsys physical design tools, they understand that the faster the latest EDA technology is adopted, the more productive design teams become and the more differentiated end-products will be.

Synopsys Professional Services provides experts in Synopsys' technology-leading design tools and platforms. Benefiting from close ties to the tool developers, extensive and ongoing employee training, and a broad resume of customer project experience, Synopsys design consultants are uniquely qualified to help rapidly deploy the latest EDA tools and technology into a customer's design flow.

Synopsys' offers the industry's leading suite of implementation and verification design tools for developing complex chips. Maintaining that technology leadership means continual enhancement of products with the most advanced features for low power design, hierarchical design and emerging technology nodes - all to improve designer productivity and address the latest design challenges.

Synopsys consultants help customers take immediate and full advantage of Synopsys tools' capabilities and run time improvements, rapidly integrating them into production flows and applying them in real-time to the most critical designs.



Tool and Methodology Services

Synopsys' services include assistance with:

- Migrating and customizing design scripts for new tools, platforms and versions
- Methodology consulting to deploy design methods and best practices such as development of physical implementation design constraints that enable best optimization results
- Applying new tool features through project-based design assistance, such as:
  - Design Compiler® Ultra: Library-aware mapping and structuring, data path optimization and critical path re-synthesis
  - Design Compiler Graphical: Topographical technology for accurate correlation to post-layout performance, power and area (PPA) and virtual global routing technology to predict wire routing congestion during RTL synthesis
  - IC Compiler/IC Compiler II: Concurrent multi-corner, multi-mode optimization, advanced clock tree synthesis including concurrent clock and data optimization (CCD) and multi-source clocking, post-route optimization, multi-voltage power optimization, final stage leakage recovery, UPF Model generation, ODL and TIO for managing hierarchical design, bus routing, double patterning technology (DPT) and FINFET support, minimum physical impact ECO flow, advanced routing algorithms, concurrent DFM optimizations and multithreading
  - PrimeTime®/StarRC™: HSPICE®-accurate analysis, CCS modeling, automated hold fixing, BAM/ETM-based hierarchical static timing analysis, advanced on-chip variation (AOCV), crosstalk delay/crosstalk noise, IR drop analysis, SI signoff, comprehensive power analysis extension, variation-aware statistical timing, hyperscale technology, DPT and FINFET modeling
  - Verification Compiler™: Accelerate verification schedule by deploying static and dynamic verification solutions including VC LP, VC Formal Coverage Analyzer, Verification IP, UVM and coverage closure methodologies

To get more information on how we can customize our services for you, please contact Synopsys Professional Services or call your local sales representative.

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