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SystemVerilog UVM Testbench Assistance

Highlights

- *Optimize testbench architecture for UVM and VMM*
- *Accelerate the development of a working SystemVerilog testbench*
- *Document verification plan and functional coverage map*
- *Integrate SystemVerilog-enabled verification IP (VIP)*
- *Quickly ramp engineering team's practical knowledge of SystemVerilog by applying the latest verification design methodologies*

Overview

With escalating system-on-chip (SoC) size and complexity, applying verification methods that rely on the writing of directed tests leads to insufficient test coverage because the number of states and test conditions is simply too large to code by hand. SystemVerilog enables new and effective verification methodologies to be deployed, such as constrained random verification that takes advantage of functional coverage technology and compute resources to provide more testing with less test code development. Automated testbenches in SystemVerilog support constrained random and other advanced verification methodologies, providing significant gains in design productivity and minimizing the risks of functional bugs.

SystemVerilog Testbench Assistance services from Synopsys help engineers and designers take full advantage of the SystemVerilog language to build a scalable and reuse-oriented testbench that verifies a device-under-test (DUT) with coverage-driven random stimulus. To ensure a high-quality design environment, Synopsys verification specialists leverage Synopsys' VCS® verification solution with Universal Verification Methodology (UVM) Standard or the Synopsys and ARM® coauthored Verification Methodology Manual (VMM) for SystemVerilog. Use of UVM helps improve interoperability and makes it easier to reuse verification components.

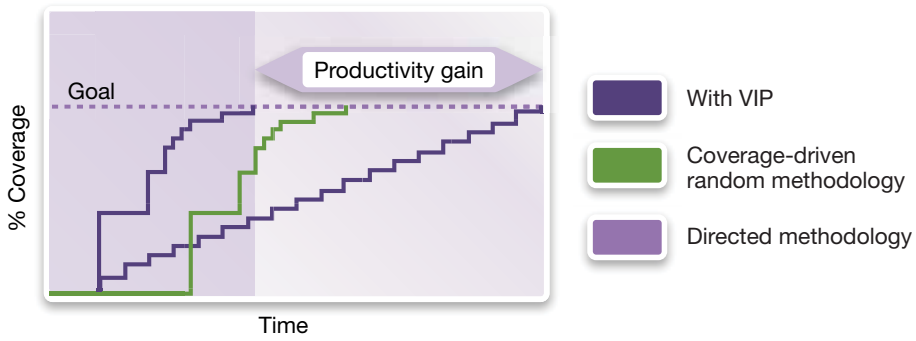

Figure 1: After initial environment setup, significant productivity gains can be realized with coverage-driven random verification methodology and integration of verification IP into testbenches.

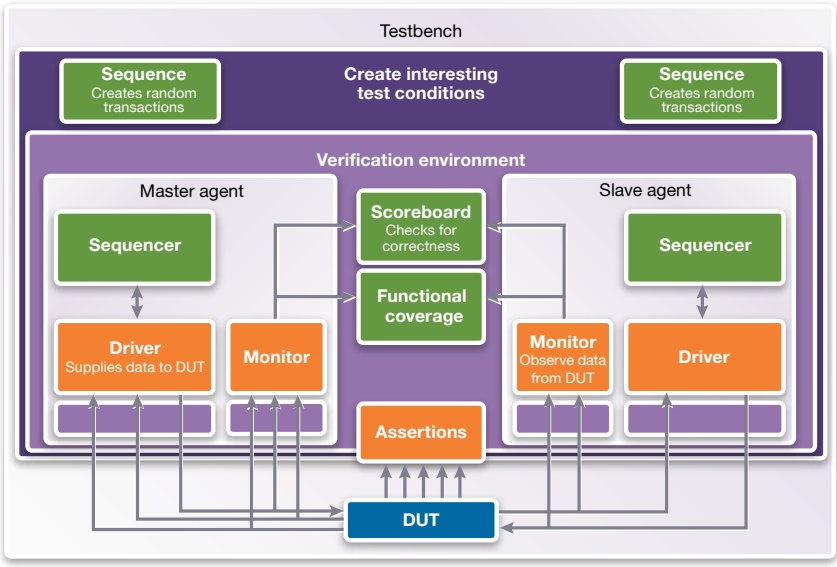

Figure 2: UVM Testbench Architecture

SystemVerilog Testbench Infrastructure

In addition to advancing testbench development, working with Synopsys consultants creates an ideal environment for knowledge sharing, giving verification engineers and designers insight into how to best utilize SystemVerilog's complete testbench infrastructure, including:

- Classes and object-oriented programming
- Constrained-random stimulus
- Functional coverage
- Process control
- Inter-process communication
- Synchronization: semaphores, mailbox, enhanced events
- Dynamic and associative arrays/lists
- New Direct Procedural Interface for connecting with C/C++ code

SystemVerilog Testbench Assistance

Synopsys' SystemVerilog Testbench Assistance offers dedicated verification specialists to help:

- Build a UVM-compliant layered testbench architecture to take full advantage of reuse and automation
- Document a robust verification plan, including:
  - Methodology summary
  - Functional verification requirements
  - Configuration requirements
  - Stimulus requirements
  - Checking requirements
  - Coverage requirements
  - Testbench environment
  - Directed and random testcase definitions
  - Coverage information that includes list of features verified and coverage score
- Construct bus functional models with both drivers and monitors
- Integrate VIP
- Build and integrate scoreboards to indicate if DUT is functioning correctly
- Measure and analyze coverage data, including code assertions, and functional coverage
- Create custom assertions or integrate existing library assertions to check correctness
- Build and integrate scoreboards to indicate if DUT is functioning correctly
- Create constrained-random test cases to target DUT features
- Create cover groups specific to the DUT's features

Synopsys consultants utilize Synopsys' industry-leading SystemVerilog technology, including VCS' Native Testbench (NTB) technology that provides built-in native-compiled support for full-featured SystemVerilog testbenches as well as the industry's most comprehensive VIP library. With extensive knowledge of the most advanced verification methodology and more than a hundred successful SystemVerilog testbench deployment engagements, Synopsys is uniquely capable of assisting you to meet your verification environment goals.

Customer Education Services

Synopsys' Customer Education classes teach engineers and designers how to make the most of the investment in Synopsys tools. The hands-on UVM Workshop will help create a better, more robust and reusable verification environment. Engineers and designers will learn how to:

- Develop UVM 1.1 and UVM 1.2 compliant SystemVerilog testbench environments
- Develop stimulus generators, device drivers, monitors and scoreboards with functional coverage
- Use UVM configuration database in test classes to manage component operation and stimulus generation
- Use UVM callbacks to minimize coding effort in making changes to existing testbenches
- Use UVM factory to change test behavior without recompilation
- Model registers in UVM to simplify accessing and testing of device registers

For more information about Synopsys' complete portfolio of consulting and design services, including SystemVerilog Language and Methodology Jumpstart, visit www.synopsys.com/sps or contact your local Synopsys sales representative at 650.584.5000.

For more information on Synopsys Customer Education please visit www.synopsys.com/Support/Training.

For more information about Synopsys' SystemVerilog tool flow, visit www.synopsys.com/SystemVerilog.

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