SoC Integration and Verification

Highlights
- Configure and integrate IP blocks and subsystems
- Employ design best practices to accelerate architecture to RTL implementation
- Apply latest methods to maximize your verification productivity

Applying Best Design Practices and Methodologies to Achieve Rapid Design Closure

The growing number and complexity of IP blocks and subsystems in today’s SoC designs challenge even the most experienced design teams, especially when the IP is based on a protocol that is new or otherwise unfamiliar to the team. Synopsys Professional Services has the expertise and experience to assist you in every stage of SoC design, including design feasibility and performance estimates, SoC configuration, integration, and verification.

SoC Integration

The quality of the configuration and integration of complex IP blocks can have a significant impact on a SoC’s development schedule and performance. Synopsys design consultants are skilled in SoC configuration and integration, and possess extensive knowledge of DesignWare® Interface IP. We work directly with system-level designers to ensure that design specifications accurately capture design intent at both the block and chip levels, helping to minimize iterations between the architecture and RTL implementation. We can then assist your team in translating the SoC specification into a high-quality RTL description following best practices pioneered by Synopsys.

SoC Verification

Verification remains the most significant bottleneck in getting advanced SoCs to market. Traditional verification methods cannot scale with today’s chip complexity. The development of an independent verification plan, protocol expertise, and efficient use of verification IP (VIP) are keys to minimizing functional bugs. Synopsys verification experts help you take advantage of advanced techniques and rapidly deploy them across project teams.

Our consultants share Synopsys’ Verification Continuum™ Platform tools expertise and apply best practices based on proven methodologies including UVM for SystemVerilog. Creating a design environment with UVM-compliant building blocks takes less time, eases cross-site collaboration and maximizes test bench re-use for future projects.

By helping you employ the best design practices and latest design methodologies, Synopsys Professional Services enables you to improve predictability of your project schedule and achieve significant gains in overall design and verification productivity throughout the entire design process.
SoC Integration and Verification Services

Synopsys' services include assistance with:

- Design feasibility, analyzing power, performance, area, complexity, design effort, risks, etc.
- Creating functional specifications based on design requirements
- Building, configuring and integrating complex IP blocks and subsystems, including controller and PHY integration for protocols such as USB, PCI Express®, DDR, HDMI and SATA
- DesignWare IP and processor core hardening
- Top-level SoC integration
- Verification planning including architecture for reuse
- Low power static verification
- Formal verification
- Deployment of advanced verification methodologies such as UVM
- Testbench generation
- Integration of protocol-specific VIP

To get more information on how we can customize our services for you, please contact Synopsys Professional Services or call your local sales representative.