SYNOPSYS®
Silicon to Software™

Physical Design Assistance

Highlights

- *Complement your design team experts with leading-edge physical design expertise*
- *Adopt design best practices and new methodologies*
- *Dedicated project assistance from synthesis through tape-out*

Proven Flows and Implementation Experience to Optimize Your Block Or Chip

With each new process node, getting your block or chip design optimized, signed off and into volume production becomes more and more difficult, especially as competitive pressures increase and market windows shrink. Leveraging the integration benefits offered by leading-edge process technologies, requires detailed knowledge of the strong interdependencies between timing, signal integrity, power distribution, power consumption and testability that amplify the challenges in physical design. The risk and expense of a long implementation cycle to meet your performance, power and area (PPA) goals can impact your time-to-market (TTM) and cost.

Through hundreds of projects and more than 20 years working on our customers' most challenging projects, Synopsys Professional Services has built up leading-edge expertise to help you achieve optimized block- or chip-level implementation of your physical design in the fastest timeframe possible. Our consultants use their extensive experience with Synopsys' world-class tools, Galaxy™ Design Platform and RTL-to-GDSII flows, including the production-proven Lynx Design System.

We deliver project support from the earliest phase of design planning through tape-out, identifying and resolving bottlenecks, and transferring methodology and best practices throughout the engagement. From block-level optimization, hierarchical design implementation, low-power design and optimization, full-chip implementation, IP integration, constraints management to design closure and chip finishing, Synopsys experts can help you meet your goals.

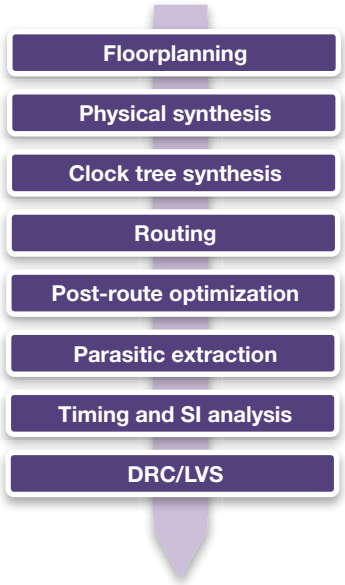

Figure 1: Specialists assist your project team throughout the different phases of physical design

Physical Design Assistance

Synopsys' services include assistance with:

- Library data, design RTL, IP block and design constraints qualification
- Hierarchical constraints budgeting and design planning
- Clock tree performance and power optimization
- Block- and chip-level power planning and optimization
- Routing closure and post-route optimization
- Design closure and sign-off for static timing, EM/IR and signal integrity
- Parasitic extraction and In-Design physical verification
- Block and chip finishing to sign-off and tape-out
- RTL-to-GDSII or netlist–to-GDSII handoff
- Exporting demonstrated methods and baseline scripts for follow-on project use
- Advanced node methodology updates for faster design closure including double patterning and sub-20nm FINFET technology
- Optimizing and hardening high performance cores from leading suppliers including ARM® and Imagination Technologies®

Synopsys assists customers in implementing more than a hundred successful designs every year. These designs span a broad spectrum of applications, chip size, complexity and process technology. This extensive resume of experience enables our consultants to transfer design best practices and deploy new methodology that help address your specific challenges and achieve PPA and TTM requirements.

To get more information on how we can customize our services for you, please contact Synopsys Professional Services or call your local sales representative.

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