SYNOPSYS®
Silicon to Software™

FPGA-Based Prototyping

Highlights

- Develop FPGA-based prototyping methodology for your ASIC design flow
- Map ASIC-targeted RTL to HAPS® series systems
- Optimize setup for software development and RTL debug

Enable Software Development Earlier With Physical Prototypes

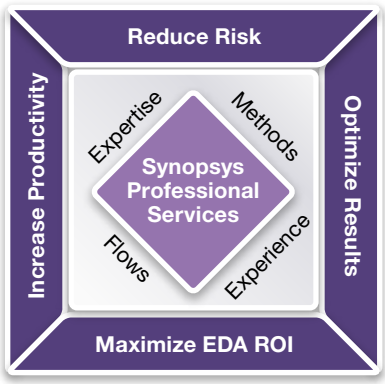
Synopsys' FPGA-based prototyping solution provides an integrated and comprehensive prototyping flow for at-speed verification of FPGAs and ASICs. Synopsys' FPGA-based prototyping software and hardware are ideal for IP and SoC design and verification teams who want to quickly prototype their ASIC on advanced FPGA devices.

Synopsys consultants provide the methodology and implementation expertise to enable deployment of a prototyping solution that efficiently maps your ASIC-targeted RTL to a Synopsys' HAPS® (High Performance ASIC Prototyping System) series prototyping system using ProtoCompiler software that includes automation features for ASIC migration, multi-FPGA partitioning, FPGA synthesis and debug. Together, our suite of tightly integrated and easy-to-use products and services expertise dramatically accelerate software development, hardware/software integration and pre-silicon system validation for individual IP blocks, processor subsystems and complete SoCs. Our engineers collaborate with your design team to define the flow and assist with the prototype implementation. The focus is on creating a robust, reusable prototyping flow that maps your SoC design into hardware enabling "real world" testing and software integration in advance of ASIC availability.

FPGA-based Prototyping Services

Synopsys' services include assistance with:

- Developing your prototyping methodology
- Test environment and integration assistance
- Adapting your ASIC-targeted RTL for FPGA(s) (e.g., migrating memories, clocks and IP)
- Configuring HAPS hardware (e.g., mapping standard interfaces and connectivity)
- Optimizing your FPGA-based prototyping flow setup for RTL debug
- DesignWare® IP integration
- Advise on HAPS daughter board design
- Complete IP block integration into the SoC system through configuration, programming, and chaining support



- Connecting the prototypes to external hardware models and verification tools

FPGA-based Prototyping Jumpstart

In addition to FPGA-based prototyping services, Synopsys consultants can provide a project jumpstart for customers who are new to the HAPS system. A typical jumpstart includes five days of on-site services to assist you in setting up a comprehensive FPGA-based prototyping flow customized for your design environment. The collaborative, hands-on deployment model accelerates the integration of prototypes into your overall verification plan while advancing your design team's knowledge of FPGA-based prototyping methodologies and implementation

Jumpstart engagements may include:

- Hands-on training that covers key tool features and methodologies using a sample design
- A review of your verification plan and prototyping goals to assist you in creating a project plan that specifies the appropriate setup and configuration required. Portions of your actual RTL code can be used to setup and illustrate the key aspects of the prototyping flow
- Using the HAPS hardware available at your site, your engineers will get hands-on experience configuring the hardware

To get more information on how we can customize our services for you, please contact Synopsys Professional Services or call your local sales representative.

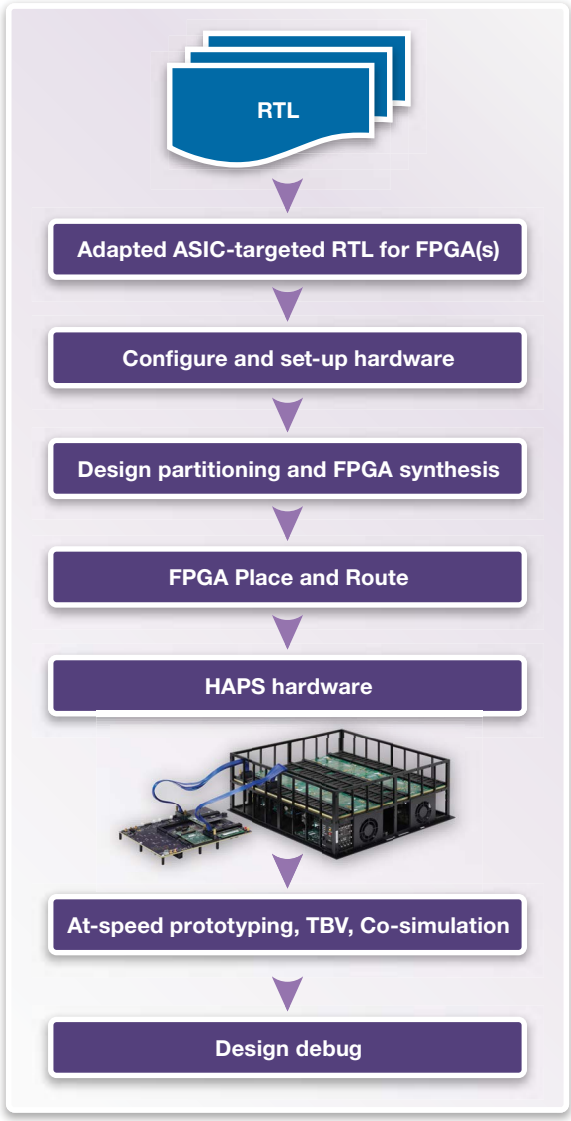


Figure 1: Synopsys' FPGA-based prototyping services include assistance with implementing an entire prototyping methodology – from RTL development, through getting the design into HAPS hardware, to actual silicon.

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Synopsys, Inc. • 690 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

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