

# Design Flow Deployment

## Highlights

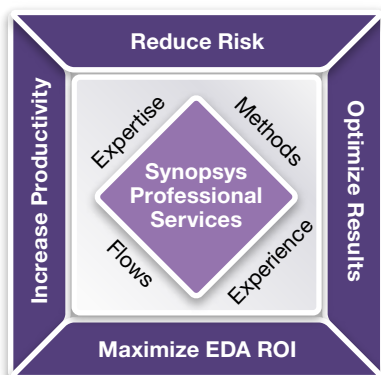
- ▶ Leverage expertise and design flows that are tape-out proven at the most advanced process nodes
- ▶ Develop and optimize flows with the latest technologies and design techniques
- ▶ Customize/configure your Lynx Design System deployment

## Optimize Your SoC/ASIC Design Flow to Address Your Latest Chip Design Challenges

Today's nanometer design geometries put tremendous pressure on physical design teams to maintain advanced design flows to achieve the required level of predictability and productivity in the chip design process. Timing and design closure remain a major challenge, but power management and low power design challenges have become top tier issues as well, along with increasingly interdependent effects of signal integrity, manufacturability and testability. ASIC and SoC design flows that were stretched to their limits to produce 90- or even 65-nm designs likely will not work at 28-nm and below without major enhancements.

Extensive experience with advanced physical design, expertise with Synopsys' Galaxy™ Design and Verification Continuum™ Platforms and significant investment in building and maintaining leading-edge EDA design flows in our own design centers, make Synopsys Professional Services uniquely qualified to help optimize your design flow for the challenges of implementing and verifying even the most advanced ASIC and SoC designs.

Because we're Synopsys, we're continually monitoring new tool releases and applying their most advanced features to our leading customers' design flows. And since Synopsys co-developed the reference flows for many of the leading foundries and IP providers including ARM®, GLOBALFOUNDRIES®, IBM®, Imagination Technologies™, Intel®, Samsung, SMIC, TSMC® and UMC®, we are the natural choice to customize and deploy them into your production design environment.



Now, with Synopsys' Lynx Design System, you can deploy a complete, tape-out-proven RTL-to-GDSII flow that helps you address both design- and project-related bottlenecks. Our SoC design consultants are experienced users of Lynx and can help you accelerate its deployment or customize it as necessary to meet your unique design environment requirements.

Whether you're at the beginning or in the middle of your EDA, SoC or ASIC design project, whether you need a minor upgrade to your design flow or a complete production-ready design system to migrate to a new nanometer design node, Synopsys Professional Services will help you eliminate the bottlenecks that impact your design productivity.

### Design Flow Deployment Services

Synopsys' services include assistance with:

- ▶ Assessment of your existing design flow, design environment and design methodology
- ▶ Implementation of production-ready sub-flows for project-specific challenges such as timing, signal integrity, low power and design-for-test
- ▶ Deployment of complete design flows to ease new technology node migrations at 65-nm, 45/40-nm, 32-nm, 28-nm, 22/20-nm, 16/14-nm and 10-nm
- ▶ Instantiation of customer-specific implementation methodologies such as low power, hierarchical or "virtual flat" design
- ▶ Incorporation of new verification methods such as low power static verification, formal verification, assertions, functional coverage, and testbench automation into an existing environment
- ▶ Deployment and customization of the Lynx Design System for customer-specific design environments, methodologies and process nodes
- ▶ Validation of a new design flow or sub-flow with a "pipe-cleaner" design and or test chip

**To get more information on how we can customize our services for you, please contact [Synopsys Professional Services](#) or call your [local sales representative](#).**