SYNOPSYS®

SUCCESS STORY

Micron Breaks the Memory Wall with 3X Faster Emulation Performance

"Micron optimized memory modeling and data movement to enable faster system validation and software bring-up for increasingly complex AI and data-centric designs."

Micron's Challenge

As AI, data center, and software-defined systems continue to grow in complexity, Micron faces increasing challenges to validate complete hardware and software systems before silicon availability. Modern designs incorporate massive memory subsystems, including high-capacity NAND, HBM, and LPDDR memories, creating unprecedented demands on verification environments.

While hardware emulation platforms already provide the compute performance required for system validation, memory capacity and bandwidth increasingly became the limiting factors. The team encountered what is commonly referred to as the "memory wall," where compute resources could process workloads faster than memory systems could supply data, creating bottlenecks that slowed verification throughput.

For Micron engineers, the challenge was clear: improve memory subsystem performance within the emulation environment so verification teams could maintain productivity, accelerate software bring-up, and validate increasingly complex systems at scale.

Micron's Solution

Validation engineers developed a NAND flash use model built around its proprietary NAND architecture and bus functional model (BFM). To enable high-performance memory modeling within its verification environment, the company leveraged Synopsys ZeBu® emulation technology, including the ZeBu memory transactor to connect hardware models to host memory.

The architecture incorporated a data-flow state machine between the BFM and the memory transactor to ensure efficient movement of data and prevent bottlenecks. With this framework in place, Micron systematically analyzed and optimized memory behavior within the emulation environment.

The team focused on three primary areas of optimization:

First, they minimized unnecessary data movement between the emulator and host system. This included keeping frequently accessed resources in hardware, batching data transfers into larger transactions, accelerating data loading through backdoor access methods, and tuning cache policies to match workload requirements.

Second, the team increased throughput through greater parallelism and pipelining. The team optimized timing behavior, replaced emulator-unfriendly delays with more efficient clock-based mechanisms, leveraged cycle-accurate interfaces where appropriate, and pipelined memory operations to reduce stalls and improve concurrency.

Third, they adopted a data-driven performance optimization methodology. Using profiling tools and performance metrics, engineers identified bottlenecks, analyzed critical timing paths, and tuned queue depths and cache configurations to focus engineering effort on changes that delivered measurable runtime improvements.

> *"Micron achieved **more than a 3x improvement in emulation performance,** significantly accelerating verification throughput across key workloads."*

Key Benefits of Micron's Solution Using Synopsys Technologies

By leveraging Synopsys ZeBu emulation and memory transactor technology, the validation teams gained the ability to model and analyze large-scale memory systems more efficiently while maintaining system-level verification fidelity.

The solution enabled:

- Faster memory access and reduced data-transfer overhead between emulator and host resources
- Improved utilization of emulation infrastructure through optimized caching, pipelining, and parallel processing techniques
- Greater visibility into performance bottlenecks through profiling and runtime analysis
- More efficient validation of hardware and software interactions before silicon availability
- A scalable framework for addressing the growing verification demands of AI and data-centric system designs

Most importantly, the Synopsys platform provided the foundation for Micron to systematically evaluate optimization strategies and focus on the changes that delivered the greatest impact on overall verification performance.

Micron's Results

Micron's optimization effort demonstrated that memory modeling efficiency can have a profound effect on hardware-assisted verification (HAV) performance.

Through profiling and analysis, the team discovered that hardware memory footprint was not the primary performance constraint. Instead, runtime improvements were driven by reducing unnecessary data movement, optimizing timing behavior, tuning cache configurations, and addressing critical performance bottlenecks.

As a result, Micron achieved **more than a 3x improvement in emulation performance,** significantly accelerating verification throughput across key workloads.

Beyond the performance gains, the project demonstrated how optimized memory models and interface technologies can help engineering teams accelerate software bring-up, improve system validation efficiency, and reduce development risk before first silicon. As system complexity continues to rise, Micron's work highlights the critical role that Synopsys ZeBu technology can play in overcoming memory-related bottlenecks and enabling faster, more effective HAV.