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SUCCESS STORY

Intel Accelerates Memory Subsystem Validation with a Reusable Framework

"By replacing fragmented, project-specific approaches with a repeatable methodology powered by Synopsys technologies, Intel increased productivity, reduced risk, and enabled faster validation of next-generation memory systems."

intel

Intel's Challenge

As AI-driven and data-intensive systems have increased the complexity of memory subsystem validation, Intel's validation teams needed a faster and more scalable approach to validate DDR, LPDDR, and HBM memory technologies. Existing validation environments relied on project-specific transactor implementations that had evolved independently across programs, creating performance bottlenecks, inconsistent debug methodologies, and limited reuse. These fragmented approaches increased maintenance effort, introduced schedule risk, and often required teams to repeatedly solve similar integration and debugging challenges.

Intel's Solution

Intel partnered with Synopsys to establish a standardized, reusable validation framework based on Synopsys DFI Transactors. Together, the two teams developed an eight-phase methodology spanning integration, validation, deployment, and automation. They standardized integration practices, documented best practices, and created a unified framework capable of supporting multiple memory technologies, including DDR, LPDDR, and HBM.

The solution also leveraged the built-in observability and analysis capabilities of Synopsys transactors, providing engineers with deeper visibility into system behavior and enabling faster root-cause analysis during bring-up and debug. By transforming project-specific knowledge into a repeatable methodology, Intel created a foundation that could be reused across future programs.

> *"Intel achieved a **2.5× improvement** in validation throughput, and a **3× reduction** in bring-up and debug time. The framework has since been reused across multiple programs, providing a **scalable** and **future-ready foundation** for memory subsystem validation."*

Key Benefits of Intel's Solution Using Synopsys Technologies

By adopting Synopsys DFI Transactors, validation engineers significantly improved validation efficiency and consistency. The solution delivered optimized emulation performance, reducing infrastructure bottlenecks and enabling faster execution. Enhanced observability improved debug productivity by helping engineers quickly identify and resolve issues. A common validation framework simplified support for multiple memory technologies while reducing dependence on specialized expertise.

The standardized methodology also aligned Intel's validation environment with JEDEC standards and industry-supported infrastructure, improving maintainability and positioning teams to more easily support future memory innovations. Most importantly, the framework enabled successful reuse across multiple projects, reducing duplicated effort and creating a scalable validation ecosystem.

Intel's Results

The implementation produced measurable business and engineering benefits. Engineers achieved a 2.5x improvement in validation throughput, significantly accelerating execution and reducing emulator bottlenecks. The combination of standardized integration practices, improved observability, and reusable debug methodologies resulted in a 3x reduction in bring-up and debug time. The framework has since been reused across multiple IP and SoC programs, providing a scalable and future-ready foundation for memory subsystem validation.

By replacing fragmented, project-specific approaches with a repeatable methodology powered by Synopsys technologies, Intel increased productivity, reduced risk, and enabled faster validation of next-generation memory systems.