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WHITE PAPER

Achieving Successful Timing, Power, and Physical Signoff for Multi-Die Designs

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Overview

Multi-die designs using 2.5D and 3D technologies are increasingly important for a wide range of electronics applications, including high-performance computing (HPC), artificial intelligence (AI), automotive, and mobile. The multi-die architecture enables designers to mix dies from different foundries and technology nodes, including existing dies from previous projects. The resulting density and interconnect speeds are much greater than those achievable with traditional discrete dies. Of course, like any advanced technologies, multi-die designs present new issues to be addressed. This white paper focuses on the timing, power, and physical signoff challenges of multi-die designs, along with advanced electronic design automation (EDA) solutions available today.

Background on Multi-Die Design

A multi-die package is one in which multiple homogeneous or heterogeneous dies are contained within a single package. The ability to mix and match dies gives system-on-chip (SoC) designers a great deal of flexibility. In return for adopting this new architecture, designers achieve lower power, higher communication bandwidth, and reduced floorspace. In addition to these benefits, two industry trends are driving the growing adoption:

- Disaggregation of a large monolithic SoC into multiple dies
- Aggregation of discrete ICs from a printed circuit board (PCB) into a single package

For both disaggregation and aggregation, there are several compelling advantages to multi-die designs. Much higher I/O densities are achievable, helping to increase throughput. Products can be assembled much more quickly from existing parts, especially variants targeted for specific applications, enabling a more flexible solutions portfolio. Multi-die designs shorten time-to-market (TTM) while reducing project risk by reusing existing, proven dies. This is particularly salient when aggregating components such as analog blocks that will not benefit from more advanced and more expensive manufacturing nodes.

Synopsys offers the industry's most comprehensive and scalable multi-die solution, for fast heterogeneous integration. The solution, consisting of comprehensive EDA and IP products, enables early architecture exploration, rapid software development and validation, efficient die/package co-design, robust and secure die-to-die connectivity, and improved silicon health and reliability. Production-hardened design engines and golden signoff and verification technologies minimize risk and accelerate the path toward an optimal system.

Multi-Die Signoff Overview

Clearly, multi-die signoff is impossible with traditional 2D timing, checking, and power analysis tools. Signals that cross between dies pass through multiple stacked layers, including interposers and substrates, and the delays through these layers must be considered for static timing analysis. This places new requirements on both physical verification and parasitic extraction. In addition, power calculations are more complex since they must combine the results for all dies. Multi-die design also requires innovation for design rule checking (DRC), layout versus schematic (LVS) verification, and other physical checks. Accurate multi-die signoff requires the entire stack to be considered. Trying to take shortcuts inevitably results in very expensive chip spins.

The Synopsys StarRC™ solution is the EDA industry's gold standard for parasitic extraction, generating output files in the Standard Parasitic Exchange Format (SPEF). It leverages Synopsys StarRC's Interconnect Technology Format (ITF) to create a virtual interface die stack for inter-die coupling. The extracted parasitics are used by Synopsys PrimeTime™, the gold standard in static timing analysis and the Synopsys PrimePower full-chip design power analysis solution.

Independently, DRC and LVS checks are performed by the Synopsys IC Validator™ physical verification high-performance signoff solution. Timing, power, and physical signoff is fully integrated with Synopsys 3DIC Compiler, a unified exploration-to-signoff platform. The combination of these solutions creates the industry's only comprehensive flow for multi-die signoff, as shown in Figure 1.

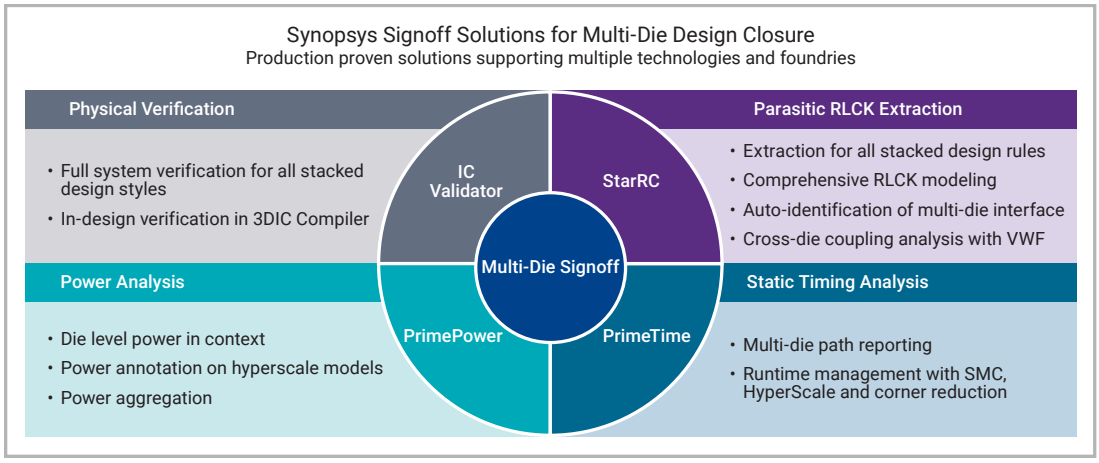

Figure 1: Synopsys multi-die signoff solution

Multi-Die Extraction and Timing Signoff

Static timing analysis (STA) is performed on the parasitics extracted from the die layout. Timing signoff of multi-die designs in Synopsys PrimeTime relies on accurate extraction by Synopsys StarRC. This requires the ability to handle all parts of the multi-die package, including through-silicon vias (TSVs), TSV coupling, micro bump, interposer, stacking, and through-dielectric vias.

With parasitics extracted for all dies and all parts of the package, STA can account for timing paths that cross dies as well as those internal to a single die. As shown in Figure 2, there are many additional capabilities in the Synopsys solution to provide timing results that match the final silicon. Synopsys StarRC uses a highly accurate RLCK model that includes resistance (R), inductance (L), capacitance (C), and mutual inductance (K) components, well beyond traditional R and C values. Other key features include:

- Auto generation of multiple placement specific Virtual Interface Blocks (VIBs)
- Auto technology and layer mapping for ease of use
- Merge of all VIB individual SPEFs into one SPEF for smooth full multi-die STA
- Support for the latest 3Dblox standard for 3DIC packaging technologies

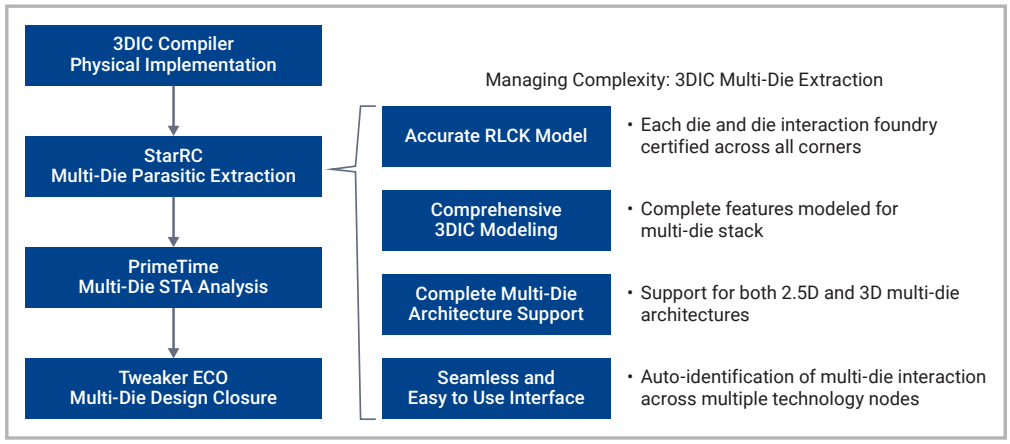

Figure 2: Synopsys multi-die timing signoff flow

There is yet another challenge in multi-die STA: worst-case and best-case timing paths may cross between two dies at very different process, voltage, and temperature (PVT) corners. Whereas paths within a single die need consider only N corners, multi-die paths must account for all possible combinations of N corners on one die and M corners on the other die. In the worst case, this means that (M x N) PVT corners must be considered. This can lead to a long turnaround time and excessive computer resource consumption for large multi-die designs.

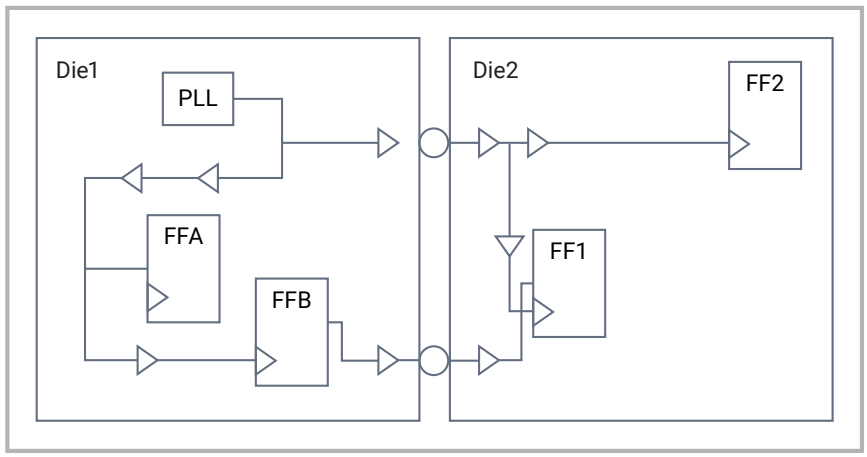

Figure 3: Multi-die STA across multiple PVT corners

To eliminate this issue, Synopsys PrimeTime uses HyperScale technology and distributed multi-scenario analysis. This enables efficient die modeling and reduction of the overall design model, especially when considering cross-die timing paths only, with reduced turnaround time at the top level of the multi-die stack. The result is highly scalable STA for multiple PVT corners.

Multi-Die Power Signoff

The parasitics extracted by Synopsys StarRC are used for power analysis and signoff as well as STA.
Synopsys PrimePower calculates power for the entire multi-die stack using the three-step flow shown in Figure 4:

1. Individual die power analysis is performed in the system context. This analysis can be done for the full chip, or for separate blocks and then added together.
2. Power is annotated to the hyperscale models.
3. Power is aggregated for all dies and, if there is interface logic between the dies, that power is also computed and added.

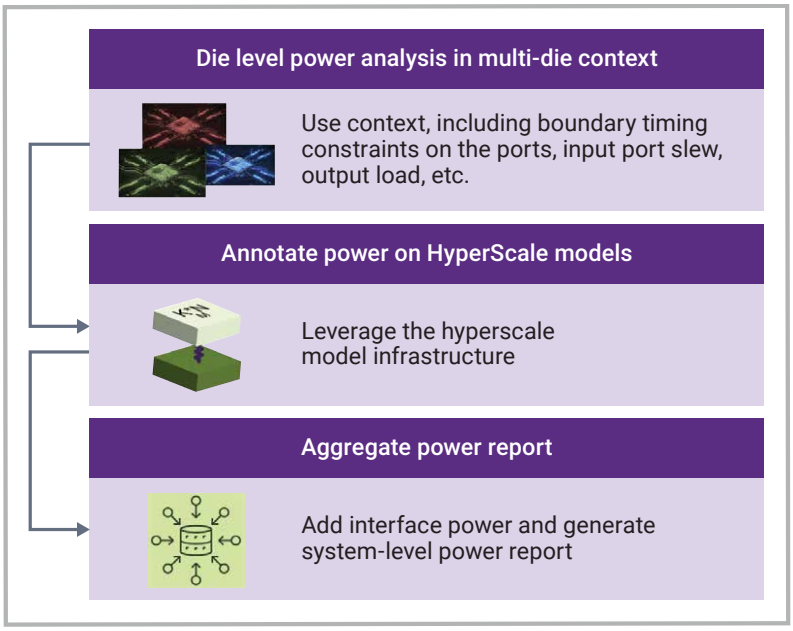

Figure 4: Synopsys multi-die power signoff flow

Thermal analysis, which is closely related to power, is especially important for multi-die designs since stacked dies concentrate heat in a smaller footprint. The Synopsys solution provides tight integration with Ansys products, which are regarded as the industry standard for thermal management.

Multi-Die Physical Signoff

In a multi-die design, DRC and LVS are performed as usual on the individual dies. However, it is critical that the structures connecting the dies be checked as well. Synopsys IC Validator enables DRC and LVS checking between the dies for all 2.5 and 3D designs. Figure 4 shows examples of the checks performed, which include:

- Inter-die DRC
  - Die placement and bump alignment
  - Die-to-die spacing and die enclosure
  - Center to center spacing between bumps
  - Floating bump shapes
  - Enclosure of bump shapes
- Inter-die LVS
  - Inter-die text check
  - Extra and missing text
  - Mismatching bump text
  - Inter-die connectivity check
  - Shorts and opens

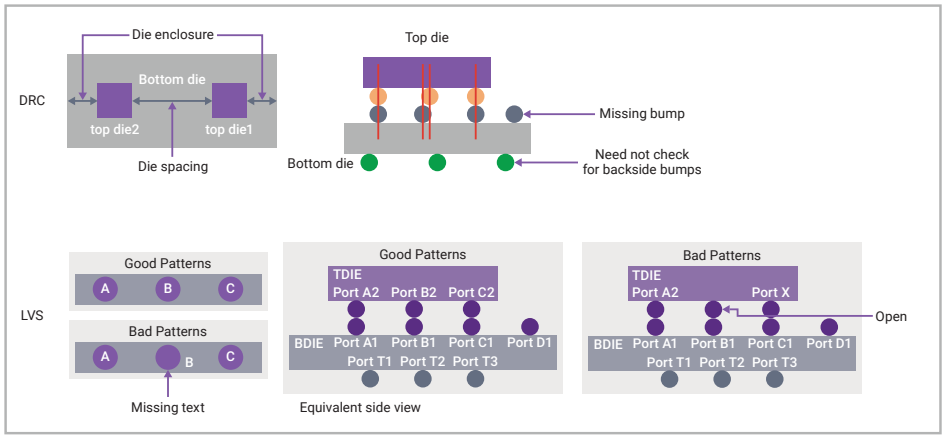

Figure 5: Examples of Synopsys multi-die physical signoff checks

Users can run multi-die DRC and LVS from within Synopsys 3DIC Compiler with a single click. A 3Dblox description is generated automatically, and Synopsys IC validator combines this with the foundry runsets to perform the checks. Synopsys 3DIC Compiler allows users to design a multi-die device and run in-design verification, as shown in Figure 5. A 3D view allows them to move around and see which die is failing a DRC or LVS check. Users can split the inter-die results and complete debug in the individual die layout.

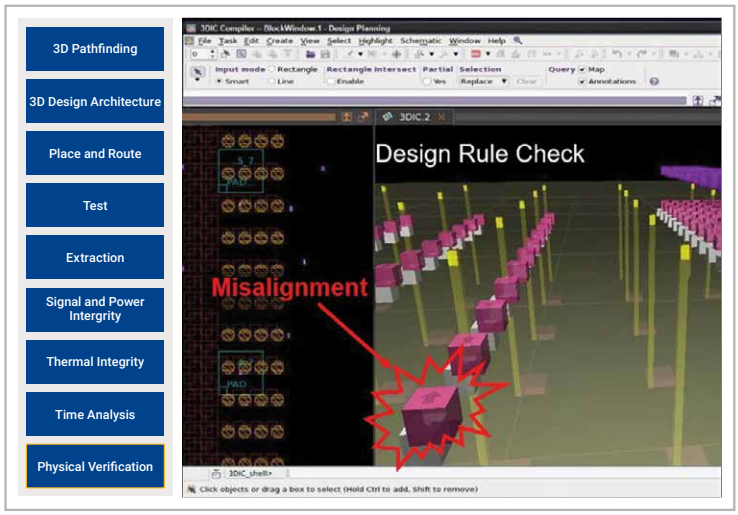

Figure 6: InDesign multi-die DRC/LVS verification in Synopsys 3DIC Compiler

Summary

Multi-die designs are becoming increasingly common, driven by both disaggregation of large dies and aggregation of multiple discrete chips into a single package. This approach provides many advantages in terms of greater design flexibility, increased density, lower power, and higher communication bandwidth. The traditional 2D EDA flow, including timing, power, and physical signoff, does not suffice for multi-die designs. Parasitic extraction must consider delays through stacked layers within the package. Power analysis must consider the results for all dies. Physical checks such as DRC and LVS must consider the entire die stack.

As multi-die adoption grows, success depends on an EDA tool flow fully capable of supporting signoff for all types of multi-die designs. Synopsys provides the industry's best solution. Parasitic extraction with Synopsys StarRC, timing analysis with Synopsys PrimeTime, power analysis with PrimePower, and physical verification with Synopsys IC Validator all handle multi-die packages accurately and efficiently. Designers and verification engineers can develop large, complex multi-die designs without fear of surprises when the assembled parts arrive in the bringup lab.