Foundation IP for GLOBALFOUNDRIES 55BCD

Highlights

- Silicon-proven, shipping in volume production
- Broad portfolio of low-power, high-speed and high-density embedded memories and logic libraries
- Largest standard cell library with over 1,500 cells
- Optimized IO design for reliability and versatility in wire bond applications
- Integrated test and repair solution delivers higher test quality and yield, while lowering overall chip area
- Auto Grade-0 compliance

Target Applications

- PMICs
- Automotive
- Consumer
- Smart Mobile
- IoT

Technology

- GLOBALFOUNDRIES 55BCD (GF55BCD)

Overview

Synopsys Foundation IP delivers a comprehensive portfolio of high-speed (HS), high-density (HD), and low-power (LP) Embedded Memories, Logic Libraries, and Input/Output (IO) Libraries, extensively validated in silicon with billions of units shipped in volume production. These proven solutions help reduce project risk and accelerate time-to-market for advanced designs.

For GLOBALFOUNDRIES' 55BCD process, Synopsys Foundation IP provides a comprehensive suite of Automotive Grade-0 compliant standard cells, SRAM compilers, Register Files (RFs), Read-only Memories (ROMs), Power Optimization Kits (POKs), and IOs. This complete set of components enables designers to efficiently implement complex digital solutions on the 55BCD platform. Integrated power management features allow system-on-chip (SoC) designers to balance power, performance and area (PPA), generating optimal configurations. Such advanced control is crucial at 55nm, where increased design and process complexity require sophisticated management of trade-offs to meet stringent product requirements and tight time-to-market schedules.

Synopsys Embedded Memory IP in GF55BCD

The Synopsys Memory Compilers in GF55BCD feature HD SRAM architecture, as shown in the table below. These HD memory compilers are optimized to generate memories with minimal area and power consumption—both static and dynamic—enabling designers to meet aggressive critical path requirements while maintaining lower power consumption.

	HD Single Port (SP) SRAM	HD One Port (1P) RF	HD Via ROM
Total bits	256-1.25M	128-128K	2K-1M
Word range	32-16K	16-1K	512-64K
IO range	8-320	8-256	4-80
Column Mux	4,8,16	2,4	16,32,64
Bank	1,2,4,8	1,2	1,2,4,8
Redundancy	Column	Column	None
Transistor Vt periphery	Optional-standard or high	Optional-standard or high	Optional-standard or high

Table 1: Synopsys Memory Compiler IP portfolio in GF55BCD

Key Features

The Synopsys Memory Compilers offer multiple levels of power management such as Light Sleep, Deep Sleep and Shut Down. These features enable array biasing to retain data with partial or full periphery shut down, and a complete shut down without data retention.

Key power-saving techniques include:

- Source biasing
- Integrated power gating using a fine-grained approach
- Multiple threshold voltages

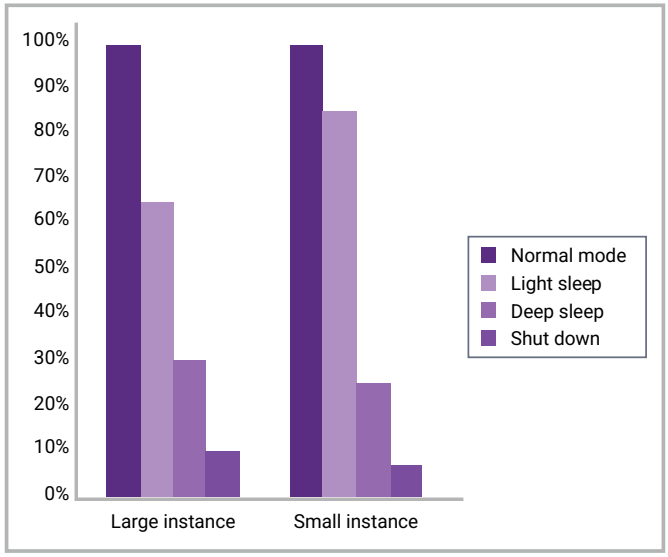

Figure 1: Synopsys Memory Compiler IP standby power savings with advanced power management features

Synopsys Logic Library IP in GF55BCD

To support a variety of applications, Synopsys Logic Libraries in GF 55BCD platform offer wide range of core device architectures, as well as triple-gate oxide (TGO) libraries to enable IO-voltage operating and IO-to-core voltage shifting. The detailed logic library portfolio is presented on the table below.

Library Architecture	Device	DNWELL	VDD	Junction Temp	Gate Density (post-shrink)
High-Performance (HP) 12 Track*	LVT*	Yes	1.2V +/- 10%	-40°C ~ 175°C	TBD
	RVT*				
	HVT*				
High-Density (HD) 9 Track	LVT*	Yes			1015.26KG/mm2
	RVT				
	HVT				
Ultra-High Density (UHD) 7 Track	LVT*	Yes			1305.34KG/mm2
	RVT				
	HVT				
Triple-Gate Oxide (TGO) 11 Track	DG	Yes	LV lib: 1.2V +/- 10% DG: 3.3V and 5V +/- 10%	-40°C ~ 175°C	200.94KG/mm2
NOTE: 12T and LVT libraries release TBD					

Table 2: Synopsys Logic Libraries portfolio in GF55BCG

Key Features

Base Library Architectures

- High-Performance (HP or 12 tracks) with over 1,500 cells in 3 Vts
- High-Density (HD or 9 tracks) with over 1,500 cells in 3 Vts
- Ultra-High Density (UHD or 7 tracks) with over 800 cells in 3 Vts
- 5V Triple-Gate Oxide (TGO or 11 tracks) with 200 cells, support 1.2V/3.3V/5V operating and shifting

Power Optimization Kits

- Power-gating cells for sleep and shut down modes
- Up, down, up/down level-shifters with and without isolation
- Dedicated isolation cells
- Retention flip-flops for standby/sleep mode with always-on cells

Engineering Change Order (ECO) Library Kits

- Fast metal-only design modifications, reduce re-mask cost

High Performance Core Design Kit (HPC DK)

- Additional Multibit Flops and DICE Flops

Key Benefits

Maximum Performance

- Fastest library architecture for CPU cores
- Achieve timing closure without sacrificing area or power

Maximum Density

- Highest density architecture
- Hand-crafted for highest routing density and utilization
- Deep cell set (over 1400) of functions and drive strengths in base library

Minimum Power

- POK with over 200 cells
- Supports low-power EDA flows with Common Power Format (CPF) and Unified Power Format (UPF)

Comprehensive Solution

- Electrically, physically and EDA-view aligned with memory products
- Advance timing and power models for accurate & reliable timing and power analyze

Synopsys IO Libraries in GF55BCD

Synopsys Foundation IP for GF55BCD includes IO Libraries that provide designers with the flexibility on IO ring creation while delivering superior PPA for their SoCs.

Key Features

- Higher operating frequency, supporting up to 100MHz
- Programmable IO voltages: 3.3V and 5V
- Programmable drive strengths
- Open drain output mode support
- Programmable input Schmitt trigger
- Programmable input options: weak pullup/down and bus keeper
- NAND-tree structure for boundary scan
- Independent core and IO power sequencing support

Additionally, the solution includes enhanced latch-up, HBM and CDM protection, ensuring reliable IO operation across a wide range of applications, including consumer electronics and automotive. The IO libraries are available in both vertical and horizontal orientations and support wire bond packaging.

Category	GPIO1	GPIO2
Core Voltage	1.2V	5V/3.3V
IO Voltage	5V/3.3V	
Latch-up	+/- 100mA @ 175°C	
HBM	2KV	
CDM	6.5A	
Drive Strength	4mA/8mA/12mA/16mA	
Inline/Staggered	Both	

Summary

The Synopsys Foundation IP portfolio for GLOBALFOUNDRIES 55BCD has been silicon-proven to address the increasingly complex design requirements that are placed on physical IP at advanced process nodes. The Synopsys power-optimized Embedded Memories for advanced processes minimize both static and dynamic power consumption. The Synopsys Logic Libraries contain over 1,500 base library cells with multiple cell variants and drive strengths to quickly achieve timing closure with minimum area and power. The Synopsys IOs are optimized for reliability and versatility in wire bond applications.

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.