HBM4 PHY

Highlights

- Supports JEDEC standard HBM4 DRAMs
- 32 independent 64-bit memory channels
- Pseudo-channel operation to enable up to 64 32-bit pseudo-channels with 2048-bit PHY
- Up to 4 trained frequencies with <5us switching time
- DFI 5.1-compatible controller interface
- PHY independent training capability
- Comprehensive set of design-for-test (DFT) features

Target Applications

- Data center and networking
- High performance computing (HPC)
- Artificial intelligence (AI)
- High-end graphics

Technology

- Leading FinFET process technologies

Overview

Synopsys offers a complete HBM4 PHY IP solution for high-performance computing (HPC), AI, graphics, and networking ASIC, Application-Specific Standard Product (ASSP), and SoC applications requiring high-bandwidth HBM4 DRAM interfaces operating at up to 12 Gbps per data pin. The Synopsys HBM4 PHY delivers superior power efficiency compared to other off-chip memory interface solutions and supports up to four active operating states for dynamic frequency scaling. To minimize area, the PHY uses an optimized micro bump array, and support for longer channel lengths allows greater flexibility in PHY placement on the SoC without impacting performance. Combined with Synopsys HBM4 Controller IP and HBM4 memory model VIP, the PHY provides a complete HBM4 interface solution. The Synopsys HBM4 PHY is provided as a hard PHY delivered as GDSII, which includes integrated application-specific HBM4 I/0s required for HBM4 signaling. The design is optimized for high performance, low latency, small area, low power, and ease of integration.
The hard PHY is easily assembled into a complete 2048-bit HBM4 PHY.
It consists of RTL-based PHY Utility Block (PUB) which includes PHY training circuitry, configuration registers, and BIST control. It features a DFI 5.1-compatible interface to the memory controller, supporting DFI 1:4:8 clock ratio, and includes metal-insulator-metal (MIM) power decoupling.

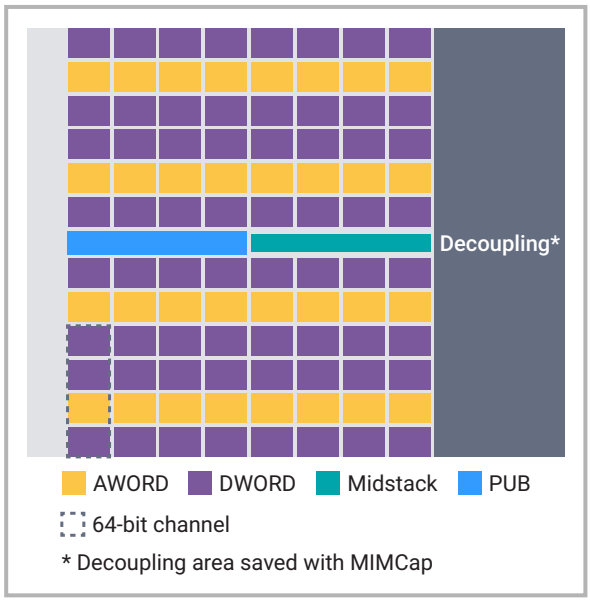

Figure 1: Synopsys HBM4 PHY block diagram

Key Features

- Low latency, small area, low power
- Compatible with JEDEC standard HBM4 DRAMs
- Supporting HBM4 DRAM Data rates
- 8H, 12H and 16H HBM4 DRAM stacks supported
- Support for fast switching between up to 4 frequencies
- Product subcomponents designed to precisely control timing critical delay and skews
- Controller DFI-compatible interface (DFI v5.1 Addendum 2)
  - PHY supports DFI 1:2:4 and DFI 1:4:8 modes (PHY:SDRAM clock ratios)
- Includes 1 phase-locked loop (PLL) per PHY and digital delay lines necessary to meet timing specifications
  - PLL allows bypass mode that enables PHY to be run at low speeds
- Separate transmit DQ and transmit DQS as well as transmit Row/Col and transmit CK delay lines
  - Allows de-skew of transmit DQS/CK vs. transmit DQ/Row- Col, respectively
- Includes separate receive DQS delay lines for both rising and falling edge of DQS
- Supports 64 pseudo-channel HBM4 DRAM systems
- Boot time impedance calibration
- Programmable I/O drive strength matching the HBM4 DRAM
- Delay line VT compensation
- Time axis data eye training
  - Internal finite state machine (FSM) allows automated training to optimum setting
  - Alternative software hooks included to allow external software to program optimum setting
- PHY VREF can either be supplied externally through a bump or use an internal VREF generator that can provide a programmable VREF for use internal to the PHY
  - Internal VREF generator is programmable from 0 to VDDQL
- Physical implementation of the top-level HBM PHY hard macro is designed to be compatible with a face centered rectangular (FCR) micro bump pattern similar to the HBM4 micro bump pattern
  - Permits shortest 2.5D routes between PHY and HBM4 DRAMs for highest signal integrity
- Area optimized micro bump pattern for smaller PHY area
- Enhanced power savings support that includes:
  - Per-channel DFI_LP
  - PHY leakage mode with fast exit (<5us)
  - PHY controls to support DRAM retention mode
- Arm® AMBA® APB interface for configuration register access
- Test data register (TDR) interface for configuration register access
- Multiple test modes
  - Delay line oscillator test mode
  - Mux-scan ATPG
- At-speed loopback testing on both the address and data channels
- Pre-hardened HBM PHYs are available in select process technologies
- Services available for custom PHY hardening requirements
- 2.5D Interposer reference designs available

Deliverables

- Executable run installation file, including GDSII, LEF Files, LVS netlists, .lib/.db timing models, Verilog model, DRC/LVS log files, I/O IBIS model, I/O HSPICE netlist, parameterized Verilog top-level PHY netlist files, sample verification environment, PHY data book, physical implementation guide, application notes, verification guide, installation guide, implementation checklist
- The PHY Utility Block includes Verilog code, synthesis/STA constraints and scripts, sample verification environment, data book

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

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