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Modeling Silicon Photonics Process Parameter Variations in Synopsys OptoCompiler-OptSim

Author

Jigesh K. Patel
Technical Marketing Manager, Custom Design and Manufacturing Group, Synopsys

Silicon photonics (SiPh) refers to the enablement of photonic integrated circuits (PIC) over silicon wafer. SiPh enables compatibility with existing CMOS manufacturing infrastructure for large-scale integration and brings the associated benefits to the photonics, namely, lower footprint, lower thermal effects, and co-packaging of electronics and photonics on the same chip. One of the side-effects of nanometer regime scaling in modern semiconductor technologies is that the impact of local (i.e., within die) variations has increased; and, efforts to reduce manufacturing variations can impose capital-intensive penalties. With the process nodes becoming smaller, corner design approaches, typically used in digital (electronic) designs, alone are not sufficient. This is especially true for the photonic designs which are more analog-like. As a result, PIC designers are tasked with the inclusion of stochastic nature of process variations into their design process and finding ways of minimizing the impact.

Process parameter variations can be included as part of the electronic-photonic design automation (EPDA) in Synopsys OptoCompiler-OptSim. We begin by a high-level classification of process variations. Next, we describe two of the approaches electronic-photonic circuit simulations can account for Monte Carlo process parameter variations during the design stage. Two case studies are presented as illustrations of each approach.

Classifying Behavior of the Process Parameter Variations

One of the ways of classifying variations in process parameters is based on the spatial scope of their influence [1-2]. Figure 1 shows types and scope of the process variations of interest.

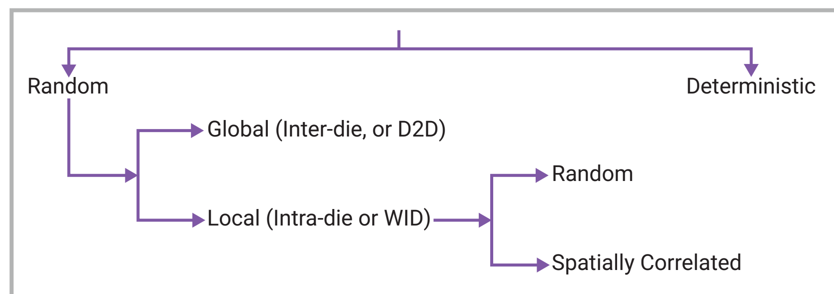

Figure 1: Independent and Correlated Process Parameter Variations in Silicon Photonics

The deterministic variations are systematic contributions from the same steps in the manufacturing process. Some of these variations can be corrected to most extent, for example, optical proximity corrections (OPC) in photolithography.

The random variations are a result of varying number of causes during the manufacturing process. Variations that affect all devices on the chip the same way are considered global. Variations from fab-to-fab, lot-to-lot, wafer-to-wafer and die-to-die (D2D) all contribute to the global variations.

The within-die (WID) variations are local to the chip and can be purely random (i.e., independent) or spatially correlated (i.e., location dependent). Typically, these local variations contribute the most to the overall process variations.

Summarizing the above, process parameter variations in a parameter α can be modeled as:

$$\alpha = \alpha_0 + \alpha_{D2D} + \alpha_{WID,\ random} + \alpha_{WID,\ correlated}$$

where α_0 is the nominal value of the parameter α. Last three terms in the above expression represent die-to-die and within-die variations.

The mean and variance of α are:

Mean:

$$m_\alpha = \alpha_0$$

Variance:

$$\sigma^2_\alpha = \sigma^2_{\alpha D2D} + \sigma^2_{\alpha WID,\ random} + \sigma^2_{\alpha WID,\ correlated}$$

Next, we illustrate two of the ways a designer can account for above variations in Synopsys OptoCompiler-OptSim EPDA design flow.

Monte Carlo Process Variation and Corner Analyses in Synopsys OptoCompiler-OptSim

The process parameter variations can be incorporated in Synopsys OptoCompiler-OptSim during simulation either via parameter definitions in a PrimeWave testbench or via sub-circuit instances of the model with process variations.

Defining Parameters Using Statistical Expressions

As an example of the former, let's consider a 6-stage lattice filter design of Figure 2. Each of the two hierarchies of Figure 2(a) is implemented as a 3-stage filter. In this example, the gap G between the straight and curved waveguide, and width D of the delay element (Figure 2(c)) are defined in the PrimeWave testbench.

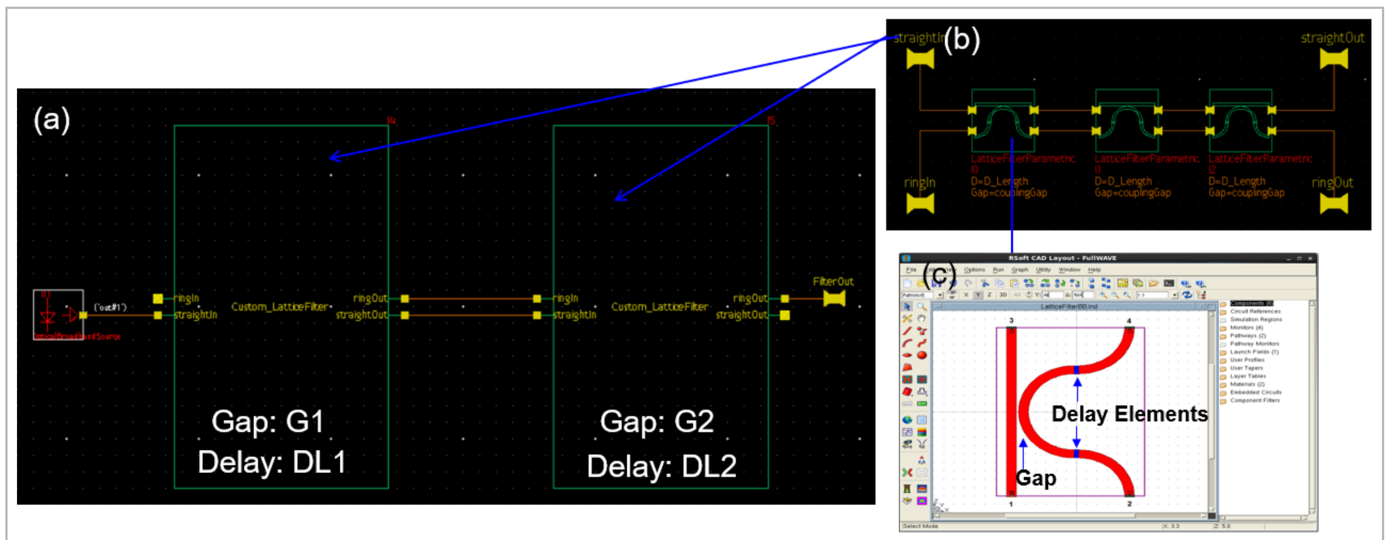

Figure 2: Schematic of a 6-stage lattice filter (a). Each hierarchy comprises of three stages (b) where each stage is implemented as parametric custom photonic block (c)

Defining parameter G via a statistical expression, say, GAUSS(1µm,0.025µm) would imply that gap G follows a Gaussian distribution with 1µm mean and a 3σ deviation of 0.025µm relative to the mean. Process correlation can be specified via intermediate variable definitions. For example:

G1=GAUSS(0.1µm,0.025µm)

G_Correlated = G1

G_wafer_to_wafer = AGAUSS(0.0,0.01µm)

With the above definition, all the model instances that use parameters G1 or G2 will carry independent random values. On the other hand, G_Correlated will be evaluated once and the same value will be carried over to all occurrences of variable G_Correlated.
If G_wafer_to_wafer represents another random variable with zero mean and absolute 3σ deviation of 0.01µm, an expression like G2 = G1 + G_Correlated + G_wafer_to_wafer would account for local and global random variations in design parameter gap of the second hierarchy of Figure 2(a).

Figure 3 shows results of a Monte Carlo simulation run with correlated statistics for filter design parameters gap and delay length.

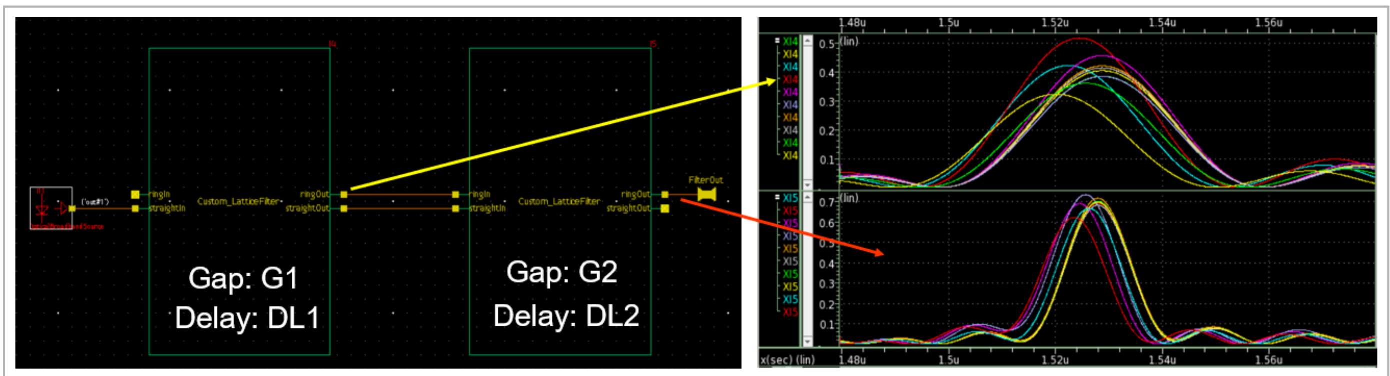

Figure 3: Filter response after 3- (upper right) and 6- (lower right) stages of lattice filters accounting for process parameter variations in gap and delay length

The plots show deviations in the filter response after 3- and 6-stages due to process parameter variations.

Using Sub-Circuit Definitions

Another way of including process parameter variations is using sub-circuit definitions for the devices used in a PIC. A sub-circuit defines statistics for the model parameters of interest. An example of a sub-circuit for a waveguide model with Monte Carlo variations in its width is shown in Figure 4.

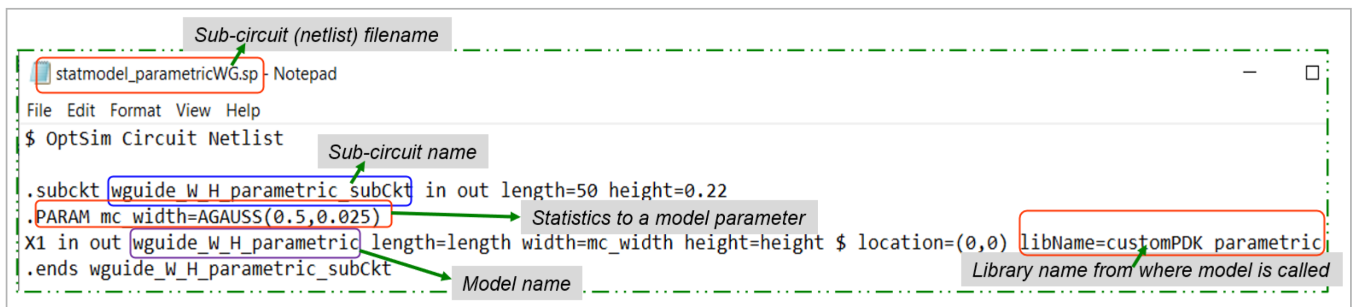

Figure 4: Example of a sub-circuit definition with process parameter variations

Conceptually, a sub-circuit is like a design hierarchy where statistics are passed from the outer hierarchy to the model inside the hierarchy. A collection of such sub-circuits can serve as a library of components with process parameters that can be shared with design partners or can be used as models during schematic creation in Synopsys OptoCompiler, an example of the latter is illustrated in Figure 5.

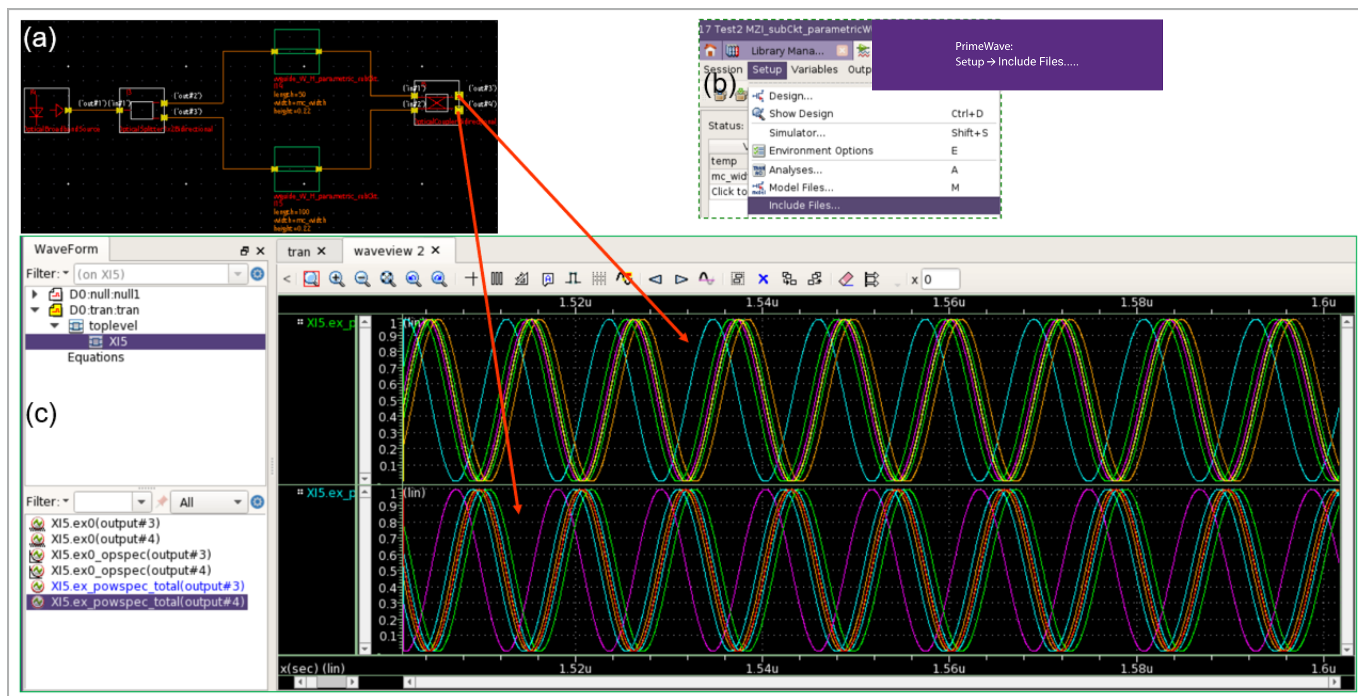

Figure 5: (a) A Mach-Zehnder Interferometer (MZI) comprising of two waveguide sub-circuits (b) including sub-circuit file of Figure 4 during run time and (c) MZI response due to process parameter variations

As shown in Figure 5(a), a broadband source shines light on a Mach-Zehnder Interferometer (MZI) implemented using two sub-circuits of a parametric waveguide. The waveguide width incorporates Monte Carlo variations due to manufacturing processes. As shown in Figure 5(b), the sub-circuit netlist file is included in the simulation via PrimeWave's Setup—>Include Files option of Synopsys OptoCompiler. Figure 5(c) shows effect of process variations in the MZI response at the constructive and destructive interference ports.

Summary

The estimation of yield and optimization of PIC design require ability to accurately account for variations in the SiPh technological parameters. These variations can be systematic (i.e., deterministic) or non-systematic (i.e., random). The spatial scales of variations include die-to-die (or global) variations, and intra-die (or local) variations. The intra-die variations can further be divided into spatially correlated and independent variations. The Synopsys EPDA offers powerful, EDA-like Monte Carlo and corner analyses to account for all these variations within Synopsys OptoCompiler-OptSim environment making design experience closer to the traditional CMOS chip design.

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