SYNOPSYS®
Silicon to Software™

RSoft Application: Estimation of Silicon Photonics Foundry Yield

Travelling-Wave Mach-Zehnder Modulator Photonic Integrated Chip

Overview

A photonic foundry needed to estimate the number of chips that would pass quality control checks despite the influence of foundry process variations.

The Challenge

Photonic chip fabrication is subject to wafer-to-wafer (WTW) and run-to-run (RTR) process variations. Multi-project wafer (MPW) runs are expensive and sensitive to yield. Accurate yield estimates require complex, multivariable stochastic analyses of electro-optic and thermal effects. The RSoft™ OptSim Circuit™ tool is an ideal solution for this design challenge.

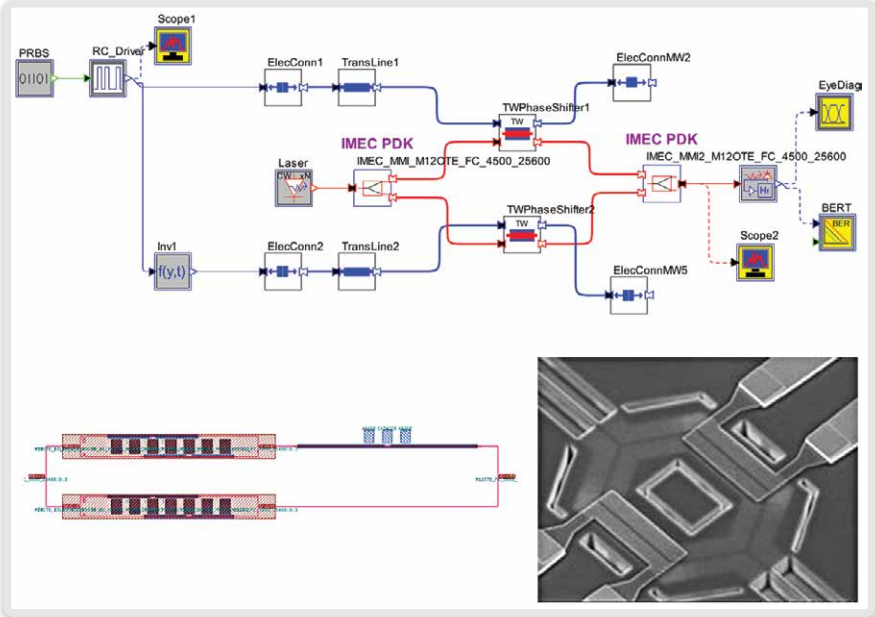

Figure 1. Top: OptSim Circuit schematic of TW-MZM PIC; Bottom left: TW-MZM PIC layout; Bottom right: fabricated chip

The Solution

OptSim Circuit provides intuitive, parametric Monte Carlo analyses with a choice of distributions in which the interplay of electrical, optical and thermal effects are modeled. Resulting designs within acceptable performance bounds provide an accurate estimate of yield.

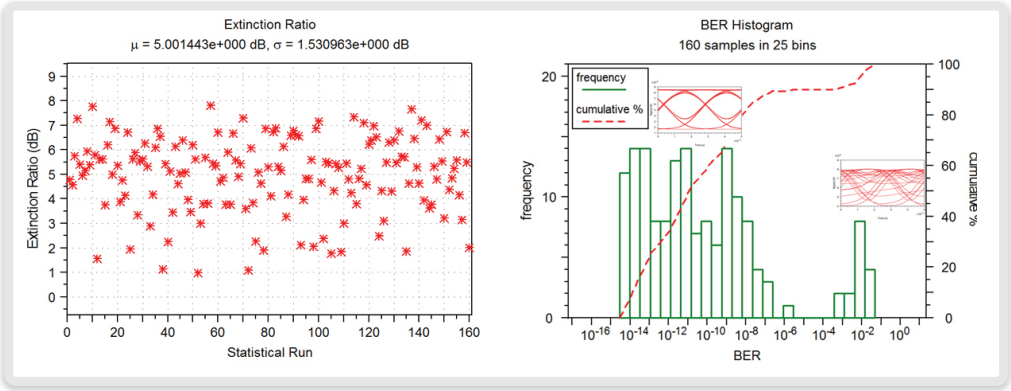

Figure 2. OptSim Circuit stochastic analysis of yield estimate with extinction ratio (left) and back-to-back BER (right)

The Result

Figure 1 shows a Travelling-Wave Mach Zehnder Modulator (TW-MZM) photonic integrated circuit (PIC) analyzed in OptSim Circuit. WTW and RTR variations cause impedance mismatch between electrode and load. In Figure 2, stochastic analysis completed in OptSim Circuit gives an estimation of yield with acceptable extinction ratio and back-to-back bit-error-rate (BER).

For more information, please contact Synopsys' Optical Solutions Group at (626) 795-9101, visit http://optics.synopsys.com/rsoft/, or send an e-mail to rsoft_sales@synopsys.com.

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