

Accurate System Voltage and Timing Margin Simulation in High-Speed I/O System Designs

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Abstract—Accurate analysis of system timing and voltage margin including deterministic and random jitter is crucial in high-speed I/O system designs. Traditional SPICE-based simulation techniques can precisely simulate various deterministic jitter sources, such as intersymbol interference (ISI) and crosstalk from passive channels. The inclusion of random jitter in SPICE simulations, however, results in long simulation time. Innovative simulation techniques based on a statistical simulation framework have been recently introduced to cosimulate deterministic and random jitter effects efficiently. This paper presents new improvements on this statistical simulation framework. In particular, we introduce an accurate jitter modeling technique which accounts for bounded jitter with arbitrary spectrum in addition to Gaussian jitter. We also present a rigorous approach to model duty cycle distortion (DCD). A number of I/O systems are considered as examples to validate the proposed modeling methodology.

Index Terms—Bit error rate (BER) simulation, high-speed link, jitter modeling, random jitter, statistical analysis, statistical eye, system margin simulation.

I. INTRODUCTION

UNTIL recently, input/output (I/O) system analysis focused on characterizing impact of deterministic jitter sources such as intersymbol interference (ISI), crosstalk, driver skew, and receiver sampling offset. The impact of random jitter sources such as supply noise, thermal noise, and reference clock jitter is difficult to evaluate during the design phase and thus typically determined experimentally. In modern high-speed I/O designs with ever shrinking timing budget, it is crucial to characterize the effects of both deterministic and random jitter sources on system performance. Recently, several new approaches are developed to estimate the overall system bit error rate (BER) with deterministic and random jitter effects [1]–[7]. The most popular approaches are based on a statistical eye consisting of the ISI probability distributions at different sampling phases [1]–[5]. The majority of these techniques assume a white random jitter spectrum, and the clock-data recovery (CDR) phase dither is often ignored [1]–[3], [5].

Manuscript received August 31, 2007; revised January 15, 2008. First published May 02, 2008; current version published November 28, 2008. This work was recommended for publication by Associate Editor P. Franzon upon evaluation of the reviewers comments.

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Digital Object Identifier 10.1109/TADVP.2008.923388

The statistical simulation technique described in [4] resolves many of these issues: colored random jitter is modeled using autocorrelation, and CDR is modeled using a Markov chain to include the channel and any jitter effects. On the other hand, popular statistical approach such as StatEye ignores the effects of channel and jitter on CDR dither and simply models CDR as part of receiver sampling jitter, resulting in inaccurate predictions of the overall system performance [3]. This paper presents accuracy improvements to the method proposed in [4]. Specifically, a new general formulation is introduced to model both white and colored bounded jitter in addition to Gaussian jitter. Furthermore, a rigorous approach to model DCD is presented. In contrast, DCD has previously been modeled in [5] using a perturbation approach which assumes that the DCD amount is relatively small compared to the length of the channel response.

The rest of paper is organized as follows. Section II describes the overall BER estimation methodology based on a statistical framework. Section III presents the detailed formulation, incorporating transmitter and receiver jitter. Section IV introduces a novel transmitter DCD model. Section V shows model validation with link measurements. Section VI summarizes the paper.

II. STATISTICAL SYSTEM-LEVEL LINK BER MODELING

In this section, a general statistical formulation to simulate the link BER is presented. Assuming linear time invariance (LTI) throughout the rest of this paper, the output signal of a channel without transmitter and receiver jitter is given by

$$y(t) = \sum_k b_k p(t - kT) = \sum_k (b_k - b_{k-1}) s(t - kT) \quad (1)$$

where $p(t)$ and $s(t)$ are the channel pulse and step responses respectively, k is the input symbol index, T is the symbol time, and b_k is the output of the transmitter. The pulse and step responses can be derived from the S-parameter of the passive channel. With the transmitter jitter, ε_k^{TX} , the output of the channel becomes

$$y(t) = \sum_k (b_k - b_{k-1}) s(t - \varepsilon_k^{TX} - kT). \quad (2)$$

After sampling at $t = mT + \varepsilon_m^{RX}$, where ε_m^{RX} is the receiver jitter, the sampled signal y_m is given by

$$y_m = \sum_k (b_k - b_{k-1}) s(\varepsilon_m^{RX} - \varepsilon_k^{TX} + (m - k)T). \quad (3)$$

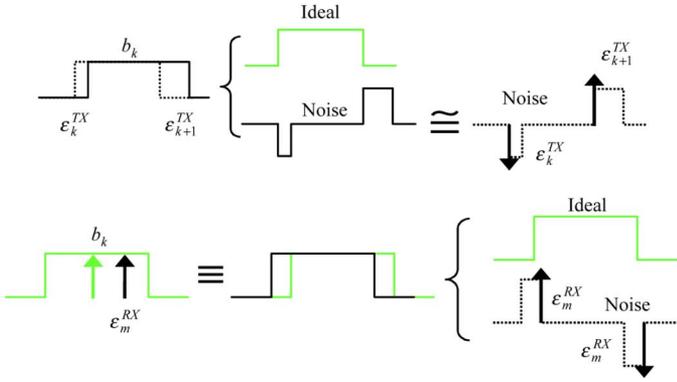


Fig. 1. Transmitter and receiver jitter models.

Note that ε_m^{RX} is not a function of the index k as it does not alter the transmitted signal whereas ε_k^{TX} is.

As in [5], the transmitter and receiver jitter¹ are modeled as impulses at the edge times as shown in Fig. 1. Both jitter components can thus be mapped into effective voltage noise at the input of the sampler using Taylor series expansion as follows:

$$\begin{aligned}
 y_m &\cong \sum_k (b_k - b_{k-1}) s((m-k)T) \\
 &\quad + \sum_k (b_{k-1} - b_k) \varepsilon_k^{TX} h_{m-k} \\
 &\quad + \varepsilon_m^{RX} \sum_k (b_k - b_{k-1}) h_{m-k} \\
 &= \sum_k b_k p_{m-k} + n^{TX} + n^{RX} \\
 &= y_0 + ISI + n^{TX} + n^{RX}
 \end{aligned} \tag{4}$$

where h_m is the data-rate sampled impulse response of the channel, y_0 is the received signal without ISI, ISI is the amount of ISI at sample time mT , and n^{TX} and n^{RX} represent the effective voltage noise for transmitter and receiver timing jitter, respectively.²

¹Receiver jitter could be alternatively modeled using conditional PDFs of timing jitter similar to the CDR phase distribution modeling shown in (7).

²Other noise sources such as thermal noise and crosstalk can be accounted for in (4) as additional terms.

Based on (4), BER is computed using the following expression:

$$\begin{aligned}
 \text{BER}(v_{\text{REF}}) &= P(\text{ISI} + n^{TX} + n^{RX} < v_{\text{REF}} - y_0 | 1) P_1 \\
 &\quad + P(\text{ISI} + n^{TX} + n^{RX} > v_{\text{REF}} - y_0 | 0) P_0
 \end{aligned} \tag{5}$$

where v_{REF} is the reference voltage which is typically nonzero for single-ended signaling I/Os, and P_1 and P_0 are the probabilities of the input bit being 1 and 0, respectively. The random variables ISI , n^{TX} , and n^{RX} are correlated since they are all functions of symbol pattern b_k and the channel impulse response. Although the exact method for BER calculation should take the correlation between ISI , n^{TX} , and n^{RX} into account by averaging the error probability over all possible bit patterns, it is assumed that they are independent to simplify the computation. With this assumption, PDFs of ISI , n^{TX} , and n^{RX} are convolved and the resulting PDF is used to calculate BER.

If n^{TX} and n^{RX} are unbounded, n^{TX} and n^{RX} may each be represented as a sum of independent Gaussian and bounded random variables. Let ζ^{Bounded} be the bounded distribution which is obtained by convolving ISI and any bounded random variables of n^{TX} and n^{RX} , and ζ^{Gaussian} be the final Gaussian random variables from n^{TX} and n^{RX} . Then, BER is given by (6), shown at the bottom of the page where P^{Gaussian} and P^{Bounded} are the Gaussian and bounded PDFs of the effective voltage noise, respectively, σ is the variance of ζ^{Gaussian} , and $Q(x)$ is the Q-function. The BER eye diagram shown in Fig. 2 is calculated by sweeping (6) over the sampling phase and the reference voltage. The time and voltage domain bathtubs can then be readily obtained from horizontal and vertical slices of the BER eye diagram.

In link applications with a CDR, the CDR dither can be modeled as a statistical sampling distribution [5]. Given the sampling distribution P^{CDR} and the distribution of receiver jitter, the overall system BER is the sum of the conditional BERs at each phase

$$\text{BER} = \sum_{\phi} \text{BER}_{\phi}(y_m | \phi) P^{\text{CDR}}(\phi) \tag{7}$$

where ϕ is the phase index and BER_{ϕ} is the link BER at ϕ .

$$\begin{aligned}
 \text{BER}(v_{\text{REF}}) &= P(\zeta^{\text{Gaussian}} + \zeta^{\text{Bounded}} < v_{\text{REF}} - y_0 | 1) P_1 \\
 &\quad + P(\zeta^{\text{Gaussian}} + \zeta^{\text{Bounded}} > v_{\text{REF}} - y_0 | 0) P_0 \\
 &\cong P_1 \sum_v P^{\text{Gaussian}}(\zeta^{\text{Gaussian}} < v_{\text{REF}} - y_0 - v | 1) P^{\text{Bounded}}(v) \\
 &\quad + P_0 \sum_v P^{\text{Gaussian}}(\zeta^{\text{Gaussian}} > v_{\text{REF}} - y_0 - v | 0) P^{\text{Bounded}}(v) \\
 &= \sum_v \left(P_1 Q\left(\frac{v + y_0 - v_{\text{REF}}}{\sigma}\right) \right) \\
 &\quad + \left(+P_0 Q\left(\frac{-v - y_0 + v_{\text{REF}}}{\sigma}\right) \right) P^{\text{Bounded}}(v)
 \end{aligned} \tag{6}$$

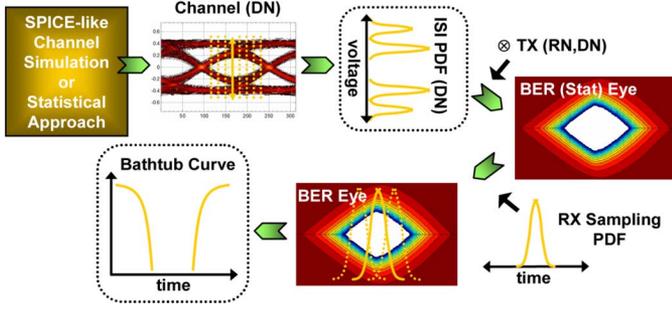


Fig. 2. Flowchart of BER calculation using statistical eye.

The overall process of BER calculation is illustrated in Fig. 2. First, the effects of ISI, jitter, and other noise sources are separated. Assuming random input data patterns and symmetric rising and falling edges [1]–[5], [8], the ISI PDF is calculated by convolving ISI components in the SBR. This approach features fast computation and accurate results. For more general systems that do not satisfy the random pattern and symmetric edges assumptions, a fast time-domain simulation technique such as multiple edge response is needed to estimate the ISI distribution [8]. Once the ISI PDFs have been calculated for each phase, they are convolved with the effective voltage noise to generate the BER eye diagram. The link BER is then calculated based on the BER eye diagram and CDR phase distribution.

III. TRANSMITTER AND RECEIVER JITTER MODEL

In the previous section, the statistical formulation was presented to account for jitter in BER calculation. In this section, the models for transmitter and receiver jitter are described. Previous statistical methodologies [1]–[5] have different models for random jitter. Most of them, [1]–[3], [5], ignore jitter spectrum while [4] models colored Gaussian random jitter. This section generalizes the method in [4] to handle bounded jitter with arbitrary spectrum.

The effective voltage noise of receiver jitter in (4) can be rewritten as

$$n^{RX} = \varepsilon_m^{RX} \sum_k b_k (h_{m-k} - h_{m-k-1}) = \varepsilon_m^{RX} \vec{a}^T \mathbf{W} \vec{h}_{RX} \quad (8)$$

where \vec{h}_{RX} is $[\dots, h_{m-k} - h_{m-k-1}, \dots]^T$, \vec{a} is a random symbol pattern vector, and \mathbf{W} is constructed from the transmitter equalizer taps \vec{w}

$$\mathbf{W} = \begin{bmatrix} \vec{w} & 0 & \dots & 0 \\ 0 & \vec{w} & 0 & \dots \\ \dots & 0 & \vec{w} & 0 \\ 0 & \dots & \dots & \vec{w} \end{bmatrix} \quad (9)$$

and $\vec{a}^T \mathbf{W}$ is the output of the transmitter equalizer.

Since the effective voltage noise is a function of \vec{a} and ε_m^{RX} , which are independent of each other, its PDF is expressed by

$$P_{n^{RX}} = P(\varepsilon_m^{RX}) P(\vec{a}^T \mathbf{W} \vec{h}_{RX}) \quad (10)$$

$P(\vec{a}^T \mathbf{W} \vec{h}_{RX})$ can be calculated by convolving the data rate sampled points of the impulse response similar to the case for the ISI PDF calculation discussed in the previous section. When ε_m^{RX} is bounded, the final PDF of n^{RX} is obtained by multiplying $P(\vec{a}^T \mathbf{W} \vec{h}_{RX})$ by $P(\varepsilon_m^{RX})$. On the other hand, when ε_m^{RX} is unbounded Gaussian, we can approximate it as a single Gaussian random variable with variance of $E_{\varepsilon_{RX}} \vec{h}_{RX}^T \mathbf{W}^T \mathbf{W} \vec{h}_{RX}$ where $E_{\varepsilon_{RX}}$ is the receiver jitter variance [4].

The transmitter jitter modeling is more complicated than receiver jitter since the effective voltage noise, n^{TX} , due to the transmitter jitter is colored by the channel impulse response as shown in (4). Therefore, the method presented above for receiver jitter is not applicable. To derive the model for n^{TX} , the transmitter jitter in (4) is rewritten as

$$\begin{aligned} n^{TX} &= \sum_k (b_k - b_{k-1}) \varepsilon_k^{TX} h_{m-k} \\ &= \sum_{k=N_{pre}}^{-N_{post}} b_k (\varepsilon_k^{TX} h_{m-k} - \varepsilon_{k+1}^{TX} h_{m-k-1}) \\ &= \vec{a}^T \mathbf{W} \mathbf{H} \vec{\varepsilon}^{TX} \end{aligned} \quad (11)$$

where \mathbf{H} is constructed from the data rate sampled channel impulse response h_n , shown in (12) at the bottom of the page, where N_{pre} and N_{post} are the numbers of precursors and postcursors in the channel impulse response. There is no general formulation for calculating PDF of n^{TX} for deterministic jitter. However, if the jitter spectrum of ε^{TX} is sufficiently low such that all jitter terms in $\vec{\varepsilon}^{TX}$ are similar, ε^{TX} can be treated as receiver jitter. The dominant high-frequency transmitter jitter is DCD and it is covered in Section IV. For the rest of this section, the formulation for modeling of transmitter random jitter is discussed.

When the transmitter random jitter ε^{TX} is colored, it can be approximated as a white discrete random process filtered by a coloring filter $h_{color,n}$ as follows [10]:

$$\varepsilon_k^{TX} = \sum_n h_{color}(n) \varepsilon_W(k-n) = \vec{h}_{color}^T \vec{\varepsilon}_W \quad (13)$$

$$\mathbf{H} = \begin{bmatrix} -h_{-N_{pre}-1+m} & h_{-N_{pre}+m} & & 0 \\ & -h_{-N_{pre}+m} & h_{-N_{pre}+1+m} & \\ & & \dots & \\ 0 & & & h_{N_{post}+m-1} & h_{N_{post}+m} \end{bmatrix}. \quad (12)$$

where $\vec{\varepsilon}_W$ is a white random variable vector. Substituting (13) into (11), we have

$$\begin{aligned} n^{TX} &= \vec{a}^T \mathbf{W} \mathbf{H} \begin{bmatrix} \vec{h}_{\text{color}}^T & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \vec{h}_{\text{color}}^T & \cdots & \mathbf{0} \\ \mathbf{0} & \cdots & \vec{h}_{\text{color}}^T & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \vec{h}_{\text{color}}^T \end{bmatrix} \begin{bmatrix} \vdots \\ \varepsilon_i \\ \vdots \\ \vdots \end{bmatrix}_W \\ &= \vec{a}^T \mathbf{M} \vec{\varepsilon}_W. \end{aligned} \quad (14)$$

It can be shown that the variance of n^{TX} is $E_\varepsilon \sum \lambda_n^2$ where λ_n is the singular value of \mathbf{M} and E_ε is the variance of $\vec{\varepsilon}_W$. The brute force approach to compute PDF of n^{TX} is to average all conditional PDFs with respect to \vec{a} . However, this approach is impractical since the size of \vec{a} can be very large due to the long channel impulse response time. Fast algorithms are introduced in [4] and [11] for specific cases. For example, [4] assumes jitter has a Gaussian distribution, while [11] assumes that transmitter jitter is white and bounded and that transmitted symbols are independent.

A faster method to calculate the PDF of n^{TX} for more general cases is based on the singular value decomposition of \mathbf{M}

$$\begin{aligned} n^{TX} &= \vec{a}^T \mathbf{M} \vec{\varepsilon}_W = \vec{a}^T \mathbf{U} \mathbf{\Lambda} \mathbf{V} \vec{\varepsilon}_W \\ &= \sum_n (\vec{a}^T \vec{u}_n) \lambda_n (\vec{v}_n^T \vec{\varepsilon}_W) = \sum_n X_n. \end{aligned} \quad (15)$$

In (15), \mathbf{U} and \mathbf{V} are orthogonal matrices whose n th column and row are \vec{u}_n and \vec{v}_n^T respectively. Matrix $\mathbf{\Lambda}$ is diagonal and its diagonal entries are $[\lambda_1, \dots, \lambda_{\text{Rank of } \mathbf{M}}]$. This equation expresses n^{TX} as the sum of dependent random variables X_n with variance $E_\varepsilon \lambda_n^2$. To simplify computation, the PDF of n^{TX} is approximated by assuming X_n being independent and simply convolving the PDFs of X_n . Note that the variance of the convolved PDFs is still $E_\varepsilon \sum \lambda_n^2$, the same as the variance of n^{TX} . This approximation usually results in a slightly higher BER and is used as an estimate of the PDF of n^{TX} . Moreover, we can also use the largest singular value, λ_1 , to produce a second approximation that usually yields a slightly lower BER. The difference between the two approximations provides a guideline to gauge the precision of n^{TX} PDF estimates: a large difference between the approximations indicates a poor PDF estimate. In typical lossy channels, we found that the \mathbf{M} matrix in (14) is dominated by one or two singular values. Fig. 3 and Fig. 4(a) demonstrate this characteristic. The channel impulse response is shown in Fig. 3, and the corresponding distribution of singular values is shown in Fig. 4(a). Using the dominant singular values to estimate of the PDF for n^{TX} is usually tight.

To speed up the computation, a single Gaussian random variable is used to approximate the combination of X_n that have small variances. Fig. 4(b) compares PDFs calculated using different methods for the sampled impulse response shown in Fig. 3. The Convolution line is the convolved PDFs of X_n . The Gaussian line is based on the approximate PDF where the bounded PDF using the first two dominant λ_n is convolved with the Gaussian PDF representing other small singular values. The

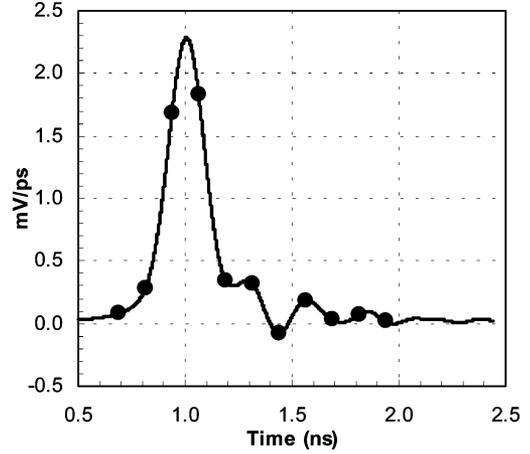


Fig. 3. Channel impulse response and its data rate sampled sequence.

Exact line is the exact PDF using the brute force method. The Maximum line is the PDF using the maximum λ_n . The approximated PDFs capture the shape of the high BER portions of the exact PDF. As expected, the low BER tails of the approximated PDFs exhibit some deviation from the target due to the various simplification assumptions made above, including assuming independence between X_n . The Gaussian approximation closely matches the PDF using all singular values demonstrating that it can be used to replace small singular values. The comparison of system-level margins using different PDF approximations is shown in Fig. 5. Gray curves are calculated using the largest singular value approximation while black curves are calculated using the independence approximation. Both results showed a good match indicating that the estimation is very tight.

IV. TRANSMITTER DUTY-CYCLE DISTORTION (DCD) MODELING

Nonidealities such as asymmetric rising and falling edges of the clock path result in deterministic jitter called duty-cycle distortion (DCD). Compared with other jitter components, DCD could be particularly detrimental since it directly modulates the width of the transmitted pulses. As shown in Fig. 6, transmitter DCD causes odd and even bits to have different bit widths and exhibit very different responses. The even bit is shorter, resulting in a smaller swing than the nominal bit response and a smaller eye. In addition, the larger odd bit creates bigger ISI, which exacerbates the reduced even bit eye (Fig. 7). Compared with TX DCD, RX DCD is usually less detrimental. RX DCD shifts the data and edge sampling locations for alternate bits. The modified sampling locations impacts the both the adaptation of the equalization and the CDR phase probability distribution. The rest of this section describes the details of transmitter DCD modeling.

In [5], TX DCD is modeled in a manner similar to random jitter as described in the previous section. The model in [5] approximates TX DCD as impulses at the edges of the ideal waveform as shown in Fig. 8. This model is equivalent to the approximation used for jitter in (3) and (4) and holds only for small DCD values. This paper presents a more rigorous approach which is applicable to large DCD values. This new approach captures impact of channel characteristics on DCD by

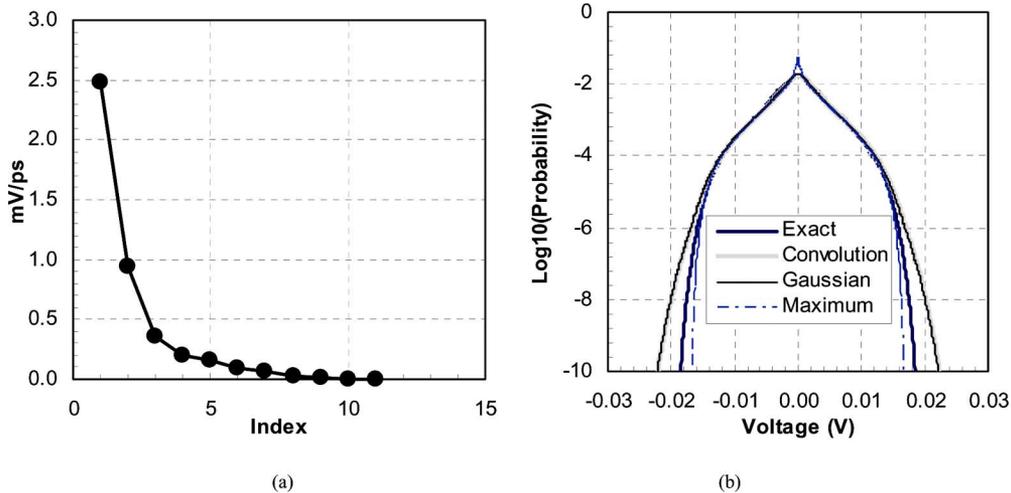


Fig. 4. (a) Distribution of λ_n and (b) PDFs of effective voltage noise using different methods at the eye center phase.

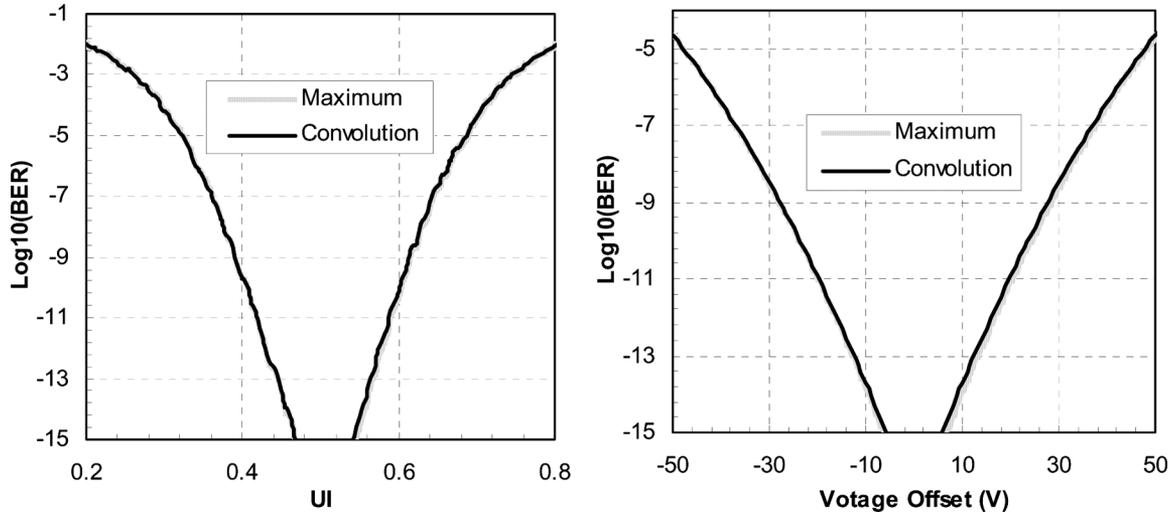


Fig. 5. Timing and voltage bathtubs calculated using different PDFs in Fig. 4.

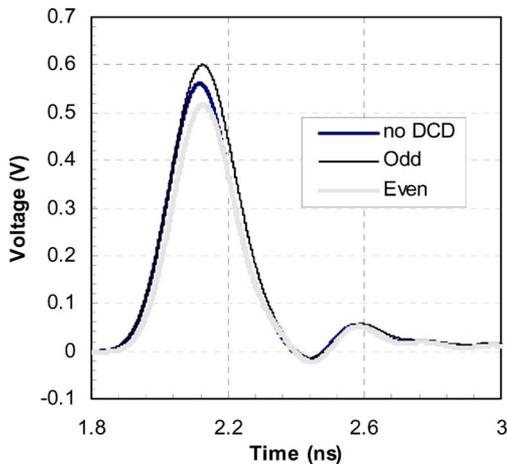


Fig. 6. Single bit responses with 10% TX DCD.

separately computing the SBRs for odd and even bits. Fig. 6 shows the SBR for a sample channel with 10% transmitter DCD.

Using the odd and even bit responses, the received signal is calculated by simply shifting and adding the corresponding

single bit responses. For example, the channel response to an input sequence b_k with b_0 bit at the even bit time is obtained by

$$y_m = \sum_{2k-1} b_{2k-1} p^{\text{odd}}((m-2k-1)T) + \sum_{2k} b_{2k} p^{\text{even}}((m-2k)T) \quad (16)$$

where p^{odd} and p^{even} are the odd and even bit responses, respectively. Equation (16) shows that the ISI contribution from the other bits on the current bit is interleaved among odd and even bits. Therefore, the ISI PDFs for odd and even bits are computed by first interlacing odd and even ISIs in time and then computing the PDFs as usual. Fig. 7 shows the ISI PDFs for an odd bit, an even bit (10% transmitter DCD), and an ideal bit (no DCD).

In the presence of DCD, the receiver sees two different eyes, one for odd bits and the other for even bits. After computing individual odd and even BER eyes based on the ISI calculations presented earlier, the final BER contour shown in Fig. 9 is then given by the average of the odd and even eyes. Note that the performance of the link is dominated by the worst case among

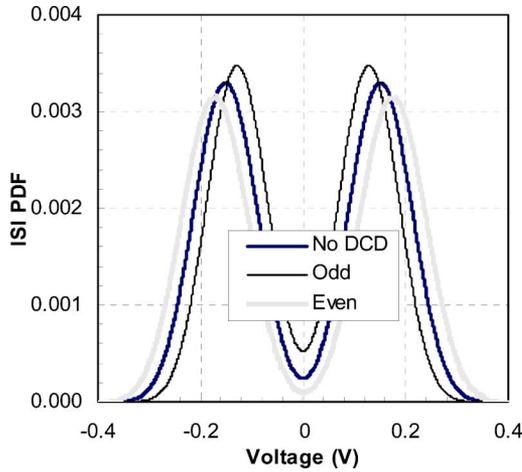


Fig. 7. ISI PDFs in presence of DCD and an ideal bit (cyan) without DCD.

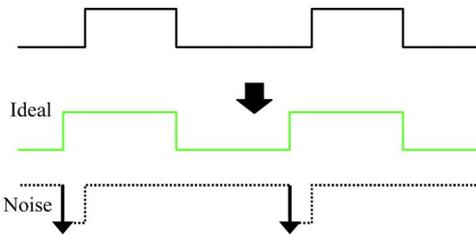


Fig. 8. Simple model of DCD.

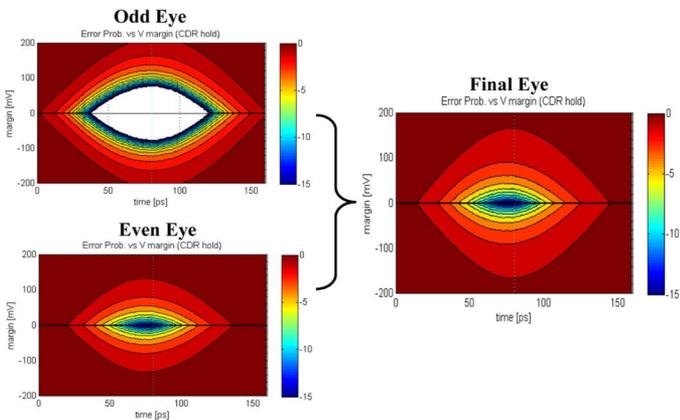


Fig. 9. BER calculation in the presence of DCD.

the odd and even eyes. As expected, the even eye is much worse than the odd eye, due to a smaller response and a larger ISI impact, and determines the final overall link performance in the example shown in Fig. 9.

V. VALIDATION

In order to validate the proposed statistical jitter modeling methodologies discussed above, we apply these models in LinkLab simulations. LinkLab is a state-of-the-art channel simulator that incorporates the complexities of both device behavior and channel characteristics in high speed links. Although other components within in LinkLab have already been validated, the simulation and lab measurement conditions are

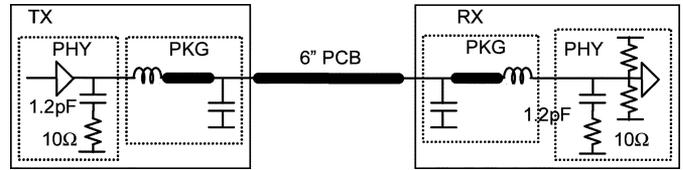


Fig. 10. FlexIO channel setup.

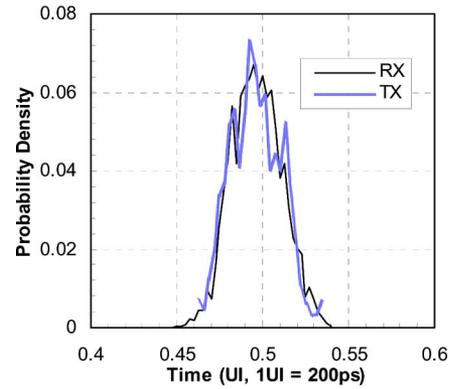


Fig. 11. FlexIO TX and RX timing measurements.

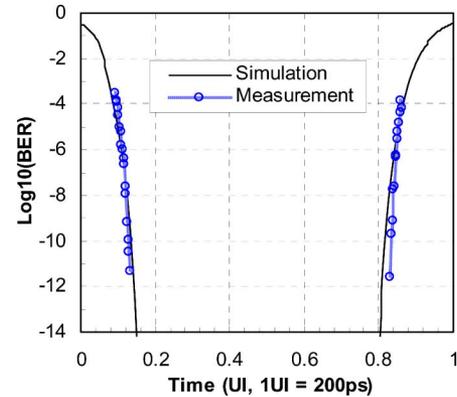


Fig. 12. FlexIO system-level correlation.

controlled to isolate the effects of jitter and CDR on system voltage and timing margins. The validation systems include a clock-forwarded Rambus parallel link called FlexIO™ [9], and a CDR-based Rambus serial link [3].

For the first system, FlexIO’s clock-forwarding produces a synchronous system which simplifies the jitter analysis by removing CDR interactions. The simulation and laboratory environment comprises a 6-in PCB link on a socket-based system test board running at 5 Gbps, as shown in Fig. 10. Parameters for the transmitter jitter distribution are measured directly using an Agilent DCA-J. Parameters for the receiver jitter distribution are obtained by differentiating measured cumulative sampling distributions. The TX and RX jitter distributions are shown in Fig. 11. Since the test system is synchronous, the measured jitter for clock and data directly impact the final sampling distributions. Incorporating a previously correlated S-parameter channel model, the LinkLab simulation produced a reasonably good estimation of actual link performance, as seen in Fig. 12. The mismatch in high BER region of the bathtub curve may be

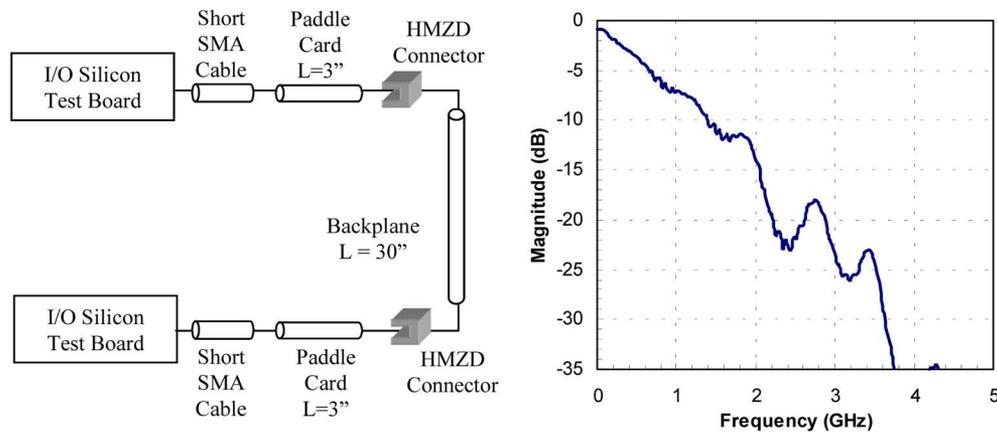


Fig. 13. Typical high speed backplane channel and its transfer function.

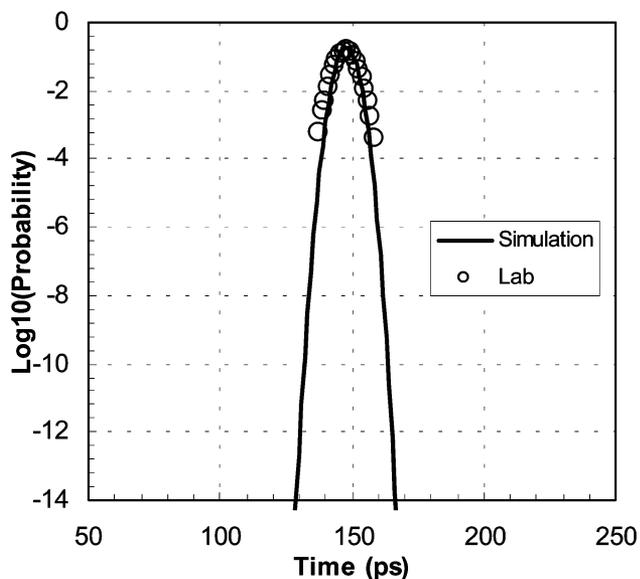


Fig. 14. Lab versus simulation comparison for CDR phase probability.

due to the fact that individual circuit components such as PLL noise, clock path, and phase nonlinearity of TX and RX are not modeled in detail.

For the next system, we consider the serial link with more detailed circuit components including the CDR sampling distribution. The simulation and lab environment comprises a 14 layer, 30-in FR4 backplane channel running at 5 Gbps shown in Fig. 13. The voltage transfer function for a 50- Ω reference is plotted (insertion loss over frequency). Although length and transfer characteristic is typical for a backplane serial links, the 100 mil backplane via stub and the 60 mil linecard via stub results in a 22 dB insertion loss at 2.5 GHz. While transmitter jitter parameters are again captured by the DCA-J, the receiver jitter parameters are extracted from the circuit model. To compare the modeled CDR processes to the real CDR behavior, we measured data on the clock recovery circuitry in the lab by collecting position information over some amount of time. The comparison between the lab measurement and LinkLab simulation of the CDR phase position in Fig. 14 shows very good correlation. The CDR position

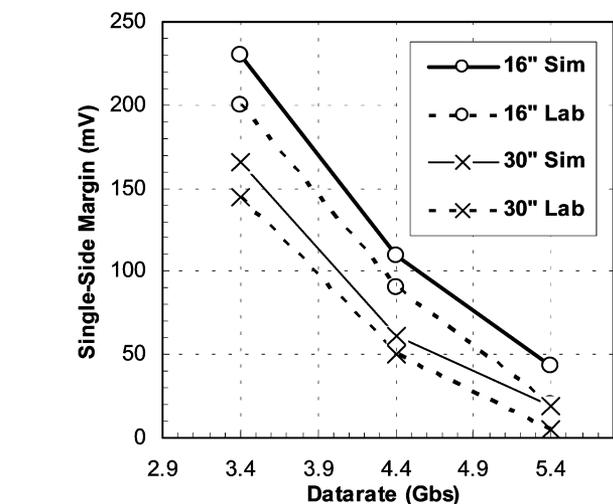


Fig. 15. Lab versus simulation comparison for extrapolated margin.

is critical as it determines the sampling position and thus the behavior of much of the receiver circuitry. Performance comparisons between lab measurement and LinkLab simulation are shown in Fig. 15. In addition to the 30-in backplane channel results are shown for a shorter 16-in backplane trace. This (\pm mV) voltage margin is defined to be at the bit error rate of 10^{-15} . This can also be thought of as an additional offset that can be applied to the receiver which would make the BER 10^{-15} . For the measurement data, we have extrapolated from 10^{-6} data by fitting with an error function. Again, the LinkLab simulation produced a good estimate of actual link performance.

Fig. 16 shows the system voltage margin data with additional simulation results using a simple receiver model which assumes ideal sampling location at the center of eye rather than using the more complete CDR behavioral model. As can be seen in this plot, the difference between including and not including the CDR model has an effect of ± 5 to 19 mV or 10 to 38 mV peak-to-peak for given channel and data rates. This difference is not constant across frequency and also varies between channels. Therefore, a simplified single offset term could lead to inaccurate simulation results.

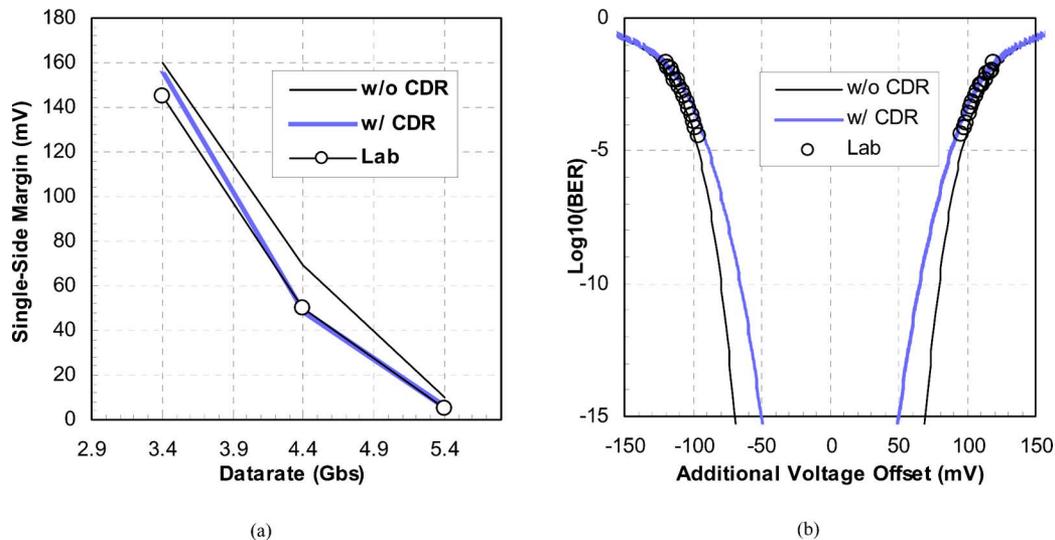


Fig. 16. (a) Margin results versus data rate for receiver models with and without stochastic CDR model, and lab measurement and (b) sample voltage bathtub plot for same three data sets at 4.4 Gbps frequency point.

VI. CONCLUSION

This paper presented an accurate way to simulate and estimate high-speed link performance. The methods presented efficiently account for both deterministic and random jitter. A general formulation to model the jitter spectrum was described along with a rigorous approach to model transmitter DCD error. Correlation data with lab measurements also demonstrate the accuracy of the presented methods for jitter modeling and channel estimation.

REFERENCES

- [1] B. K. Casper, M. Haycock, and R. Mooney, "An accurate and efficient analysis method for multi-gb/s chip-to-chip signaling schemes," in *IEEE VLSI Circuits Symp. Tech. Papers*, Jun. 2002, pp. 54–57.
- [2] B. Ahmad, "Performance specification of interconnect," presented at the DesignCon, Santa Clara, CA, Feb. 2003.
- [3] A. Sanders, M. Resso, and J. D'Ambrosia, "Channel compliance testing utilizing novel statistical eye methodology," presented at the DesignCon, Santa Clara, CA, Feb. 2004.
- [4] V. Stojanovic and M. Horowitz, "Modeling and analysis of high-speed links," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2003, pp. 589–594.
- [5] J. Caroselli and C. Liu, "An analytic system model for high speed interconnects and its application to the specification of signaling and equalization architectures for 10 gbps backplane communication," presented at the DesignCon, Santa Clara, CA, Feb. 2006.
- [6] B. Ahmad and J. Cain, "Performance evaluation of high speed serial links," presented at the DesignCon, Santa Clara, CA, Feb. 2001.
- [7] S. Sercu and J. D. Geest, "BER link simulations," presented at the DesignCon, Santa Clara, CA, Feb. 2003.
- [8] D. Oh, "Multiple edge responses for fast and accurate system simulations," in *IEEE 15th Topical Meeting Electr. Performance Electron. Packag.*, Scottsdale, AZ, Oct. 2006, pp. 163–166.
- [9] W. Kim, J.-H. Kim, D. Oh, and C. Yuan, "Implementation of broadband transmission line models with accurate low-frequency response for high-speed system simulations," presented at the DesignCon, Santa Clara, CA, Jan. 2006.
- [10] J. R. Barry, E. A. Lee, and D. G. Messerschmitt, *Digital Communication*, 3rd ed. Boston, MA: KAP, 2004, ch. 7, pp. 298–299.
- [11] H. Hatamkhani, F. Lambrecht, V. Stojanovic, and C. K. K. Yang, "Power-Centric design of high-speed i/os," presented at the Design Autom. Conf., San Francisco, CA, Jul. 24–28, 2006.



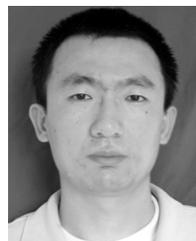
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