SYNOPSYS®

DATASHEET

Custom Compiler

Best-in-Class Technology for Analog, RF and Mixed-Signal Design

Accelerating robust analog design

Overview

Synopsys Custom Compiler™ is a modern design environment tuned for analog, mixed-signal, custom digital, and RF integrated circuit (IC) design. The platform delivers an integrated solution for design entry, simulation management and analysis, layout editing, with in-design verification and analysis.

Custom Compiler is engineered to meet the demands of planar CMOS, BiCMOS, SiGe, BCD, advanced FinFET, Gate all-around (GAA) and emerging process technologies, delivering industry-leading productivity, performance, and ease-of-use—while remaining intuitive and easy to adopt for users of legacy design environments.

AI-Powered Analog Layout Synthesis

Custom Compiler introduces a breakthrough AI-powered analog layout synthesis capability that transforms one of the most manual and expertise-driven stages of chip design.

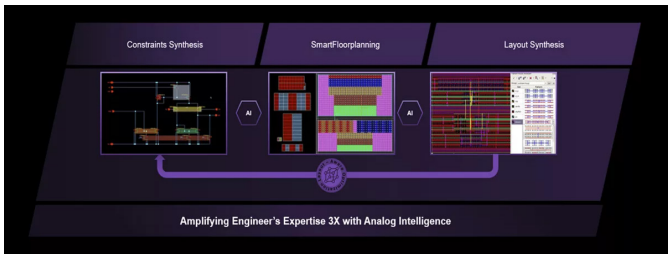

Figure 1: AI-powered Custom Compiler layout synthesis

Powered by Synopsys.ai™, Custom Compiler layout synthesis uses analog intelligence to automatically generate layout implementations from schematic intent. The new solution is composed by four key technologies:

- **Constraints Synthesis:** AI-powered technology that automatically identifies analog topologies on schematics by leveraging best practices and design team knowledgebase to generate layout constraints for downstream automation
- **Synopsys SmartFloorplanning™**: Graphical, constraint-driven technology abstracted environment with AI-guided placement recommendations system to accelerate floorplanning task of complex analog layout circuits
- **Layout Synthesis**: One-click synthesis from SmartFloorplan to layout, transforming abstract intent into a technology-specific implementation with built-in layout features such as guard-ring insertion, dummy generation, AI-Guided automated device routing

- **Layout-Aware Optimization:** AI-powered circuit optimization that incorporating layout parasitics that help reduced layout iterations and ECO cycles and improve correlation with post-layout simulation results

By accelerating layout creation, improving consistency, and minimizing iteration cycles, AI-powered analog layout synthesis helps teams overcome a long-standing productivity bottleneck and scale analog design development for next-generation mixed-signal, RF, and high-speed applications delivering:

- Up to 3× faster layout implementation with fewer iterations
- Consistent, high-quality analog layout across designers and nodes
- AI-powered automation from schematic intent to optimized layout

Design Entry, Schematics, Simulation, and Analysis

Custom Compiler Schematic Editing and PrimeWave Design Environment provides a highly productive solution for mixed-signal design entry, debug, simulation management, analysis, waveform analysis and reporting.

Key capabilities include:

- Streamlined schematic entry with automatic wiring, symbol generation, and parameter editing directly on-canvas
- Advanced debug features such as power domain analysis and hierarchical net tracing
- Design comparison tools to quickly identify schematic changes
- Unified support for schematic and text-based design (including Verilog), with cross-probing and back-annotation

PrimeWave Design Environment features include:

- Tight integrated with Synopsys PrimeSim™ technologies: PrimeSim HSPICE®, PrimeSim SPICE, PrimeSim Pro, and PrimeSim XA
- Support for third-party SPICE simulators
- Simulation of multiple PVT corner and Monte Carlo statistical analysis, and multi-testbench analysis
- Grid-enabled simulation distribution and monitoring
- Advanced waveform visualization, statistical analysis, and HTML-based reporting
- AI-powered Multi-Objective analog circuit optimization with layout aware optimization capabilities
- AI-powered WaveForm analysis for enabling fast detection of outlier signals waveform in large PVT corner analysis and/or statistical analysis

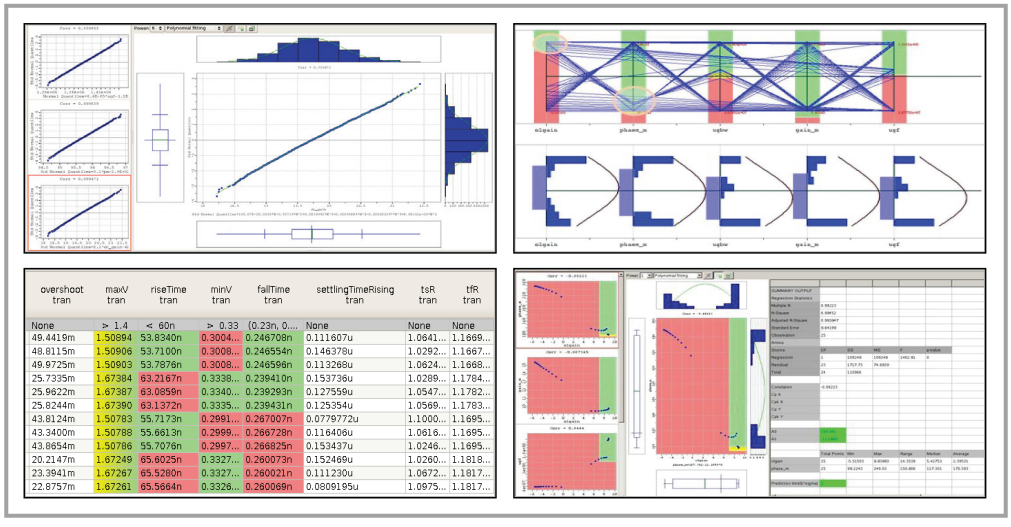

Figure 2: Charting, reporting, and statistical analysis

High Performance Layout Editing and Automation

Custom Compiler enhances layout productivity with a fast, intuitive editing environment and AI-powered analog layout synthesis capability.

Key innovations include:

- Familiar, high-performance layout editing
- Schematic-driven layout with real-time connectivity and devices parameter validation
- Pattern-based device placement for analog structures
- Automated routing with intelligent pattern routers

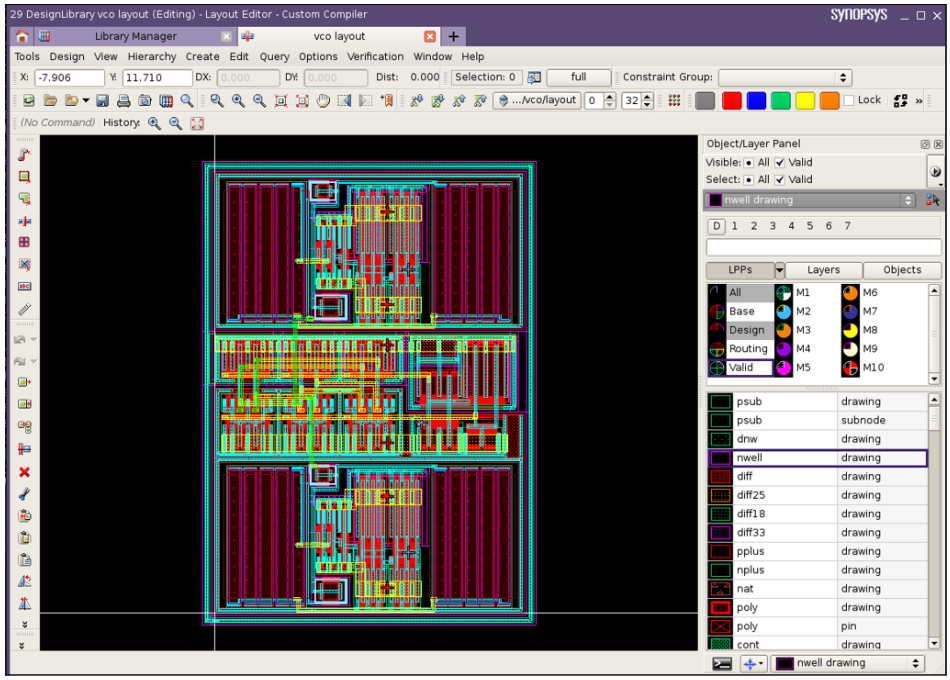

Figure 3: Fast and user-friendly custom layout editing

The visually-aware automation (VAA) flow delivers 2–10× productivity improvements, especially for complex advanced FinFET and GAA-based designs, by:

- Automating repetitive layout tasks
- Eliminating manual constraint entry
- Leveraging graphical workflows familiar to layout designers

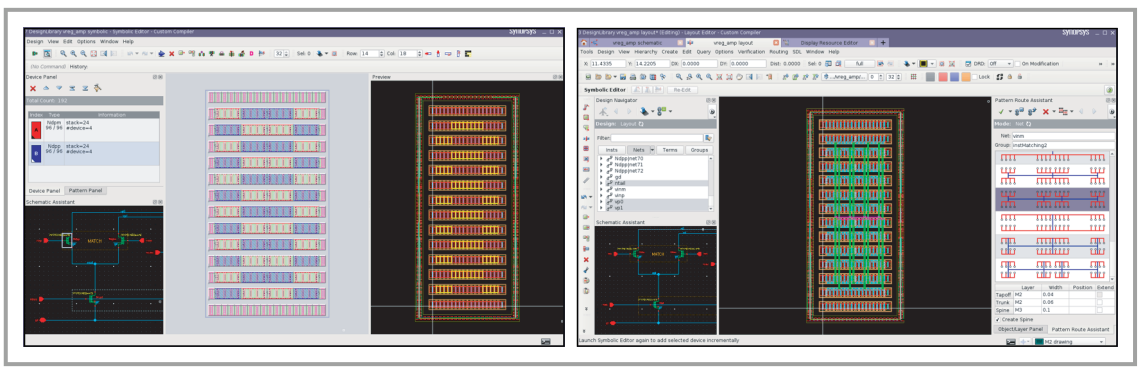

Figure 4: Advanced schematic-driven layout features: symbolic editor (L) and pattern router (R)

Improving productivity with signoff technologies integration:

- Extraction Fusion for early parasitic feedback from partial layouts
- DRC Fusion for real-time rule checking using Synopsys IC Validator™

These capabilities ensure tighter collaboration between circuit and layout designers and reduce rework across design iterations.

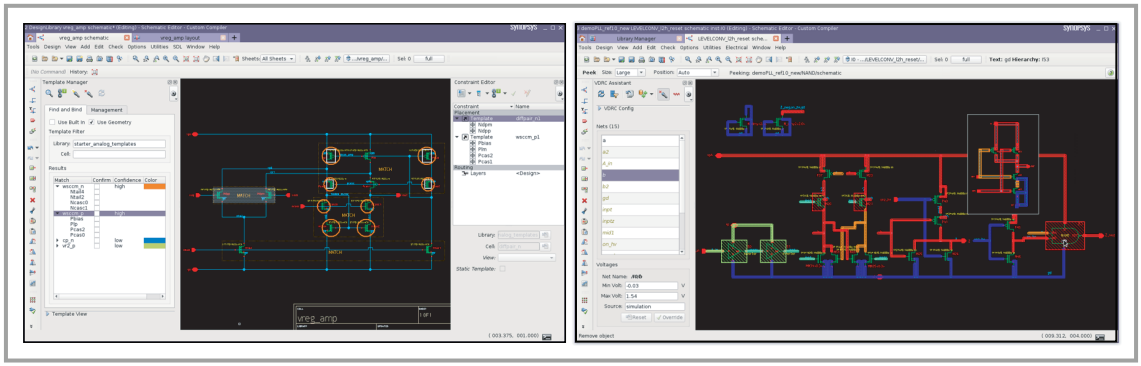

Figure 5: Design intent communicated via constraints (L) and current/voltage annotations (R)

Integrated Electromagnetic Analysis

Custom Compiler extends its multiphysics analysis capabilities with integration of multiphysics HFSS-IC technologies, providing a trusted, high-fidelity, electromagnetic insight throughout the design flow.

This integration enables:

- Simplify electromagnetic analysis and RF simulations by integrating HFSS-IC solvers with the Synopsys Custom Compiler layout environment
- Intelligent passive components synthesis and validation with accurate EMAG modeling, producing editable PyCell devices in Custom Compiler layout and schematic environments
- On-chip electromagnetic analysis and optimization of critical structures such as inductors, interconnects, transmission lines, and passive devices
- Accurately capture on-chip high-frequency parasitics and layout-dependent effects that shape analog and mixed-signal behavior
- Detect electromagnetic-induced signal integrity, performance, and reliability issues earlier in the design cycle

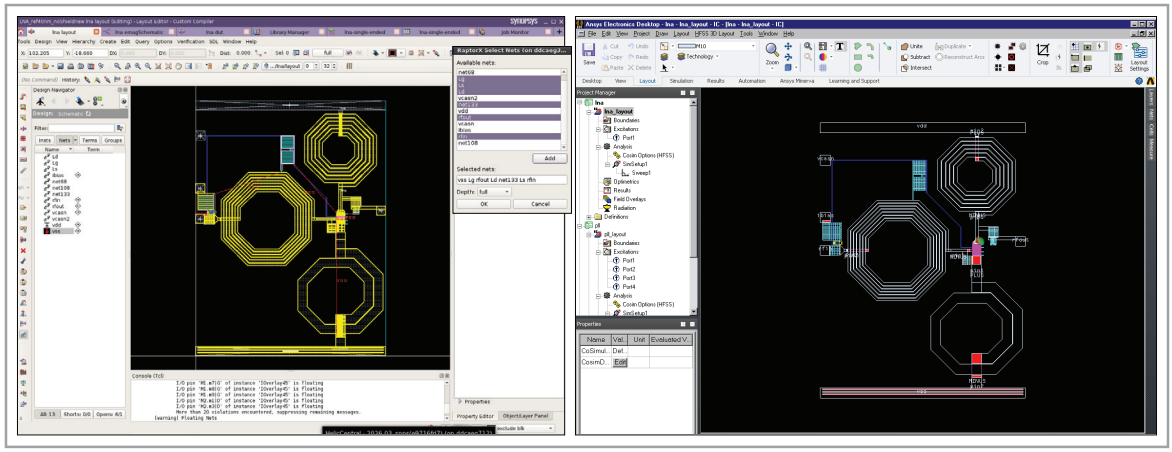

Figure 6: LNA analysis with RaptorX in Custom Compiler (L) and with HFSS in AEDT (R)

By embedding electromagnetics directly into the design environment, Custom Compiler eliminates manual handoffs between tools, allowing designers to:

- Evaluate electromagnetic effects earlier in the design cycle
- Reduce costly late-stage iterations
- Increase confidence in highspeed analog and RF circuit performance

In-Design Verification and Early Parasitic Insight

Custom Compiler includes built-in verification technologies that enable designers to detect and resolve issues earlier in the design process:

- Dynamic design rule checking (DRC) during layout editing
- Electromigration (EM) analysis with current-aware annotation
- Resistance and capacitance extraction using Synopsys StarRC™
- Early parasitic extraction through Extraction Fusion technology

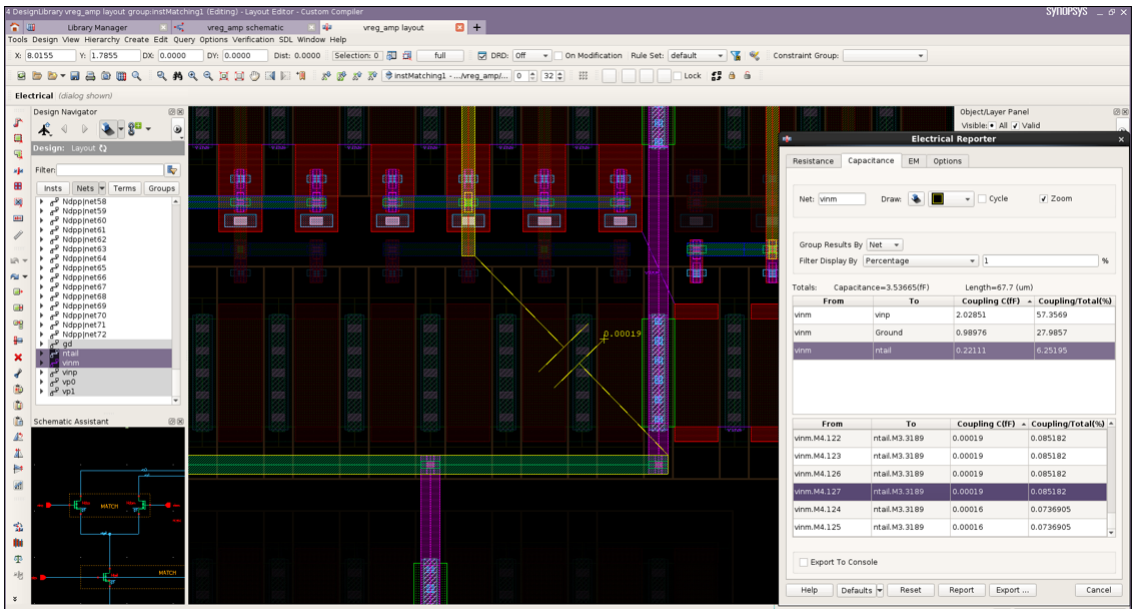

Figure 7: Electrical reporter checks resistance, capacitance, and electromigration during layout

These capabilities provide immediate feedback during layout creation, enabling:

- Early validation of design intent
- Reduced late-stage iterations
- Faster convergence to signoff-quality designs

Unified Custom and Digital Implementation

Custom Compiler integrates seamlessly with IC Compiler™ II, providing a unified design environment for analog and digital implementation:

- Open, edit, and refine shared design databases at any stage
- Perform full-custom edits on digital blocks
- Integrate custom analog blocks into digital flows

This bi-directional flow ensures synchronization between analog and digital domains, enabling efficient mixed-signal design development.

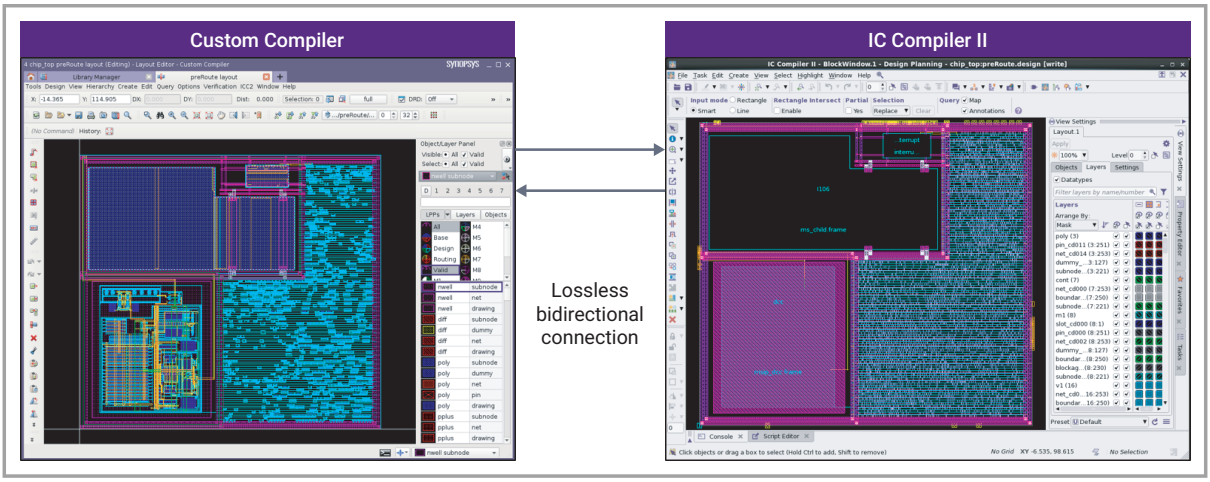

Figure 8: Custom Compiler can open, edit, and save IC Compiler II design databases

Open and Customizable Environment

Custom Compiler is built on the OpenAccess database, enabling straightforward adoption and interoperability with third-party tools.

Key benefits:

- Rich APIs for customization and automation
- Support for TCL, Python, and C++ extension languages
- Integration with third-party tools for simulation, verification, extraction, and data management
- Support for industry-standard iPDK process design kits across advanced nodes

For more information about Custom Compiler, visit https://www.synopsys.com/implementation-and-signoff/custom-design-platform/custom-compiler.html.