

Accelerating Toshiba's Advanced System-on-Chip (SoC) Design with Synopsys' Fusion Compiler

Early access to the industry's only RTL-to-GDSII solution enables Toshiba to speed time-to-market for their latest, advanced, automotive SoC

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Introduction

Toshiba Electronic Devices & Storage Corporation, part of the broader Toshiba, Kawasaki Japan, has long been a technology leader in Advanced SoCs spanning multiple, key market verticals. This includes automotive, communications, IoT and ASIC applications. Although the specific demands for each of these verticals is varied, what is common among all of them is the need to hit increasingly short market-opportunity windows. For that, what is key to Toshiba is having a predictable and convergent design experience with the shortest time to optimal results.

Toshiba Electronic Devices & Storage Corporation Focusing Area

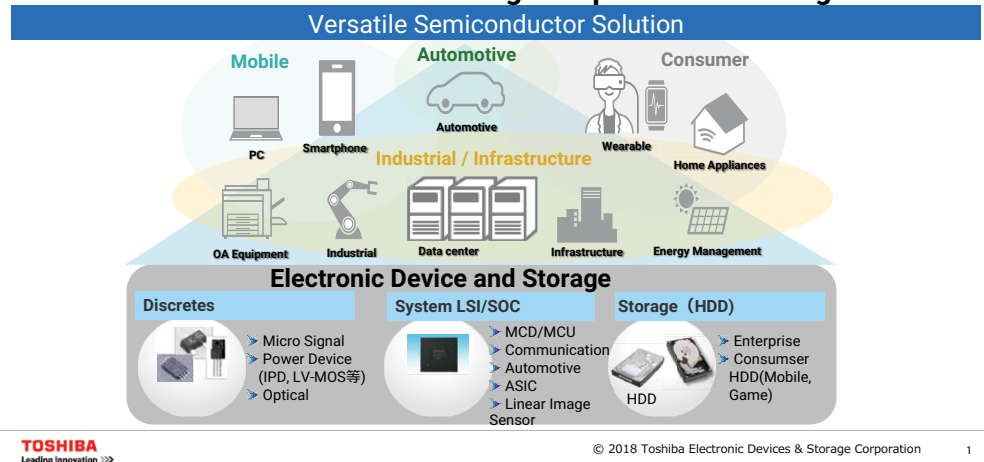


Figure 1: Toshiba provides diverse semiconductor solutions on a world-wide basis as described above.

Toshiba has long been a close collaboration partner with Synopsys with an overarching goal to always deliver to our customers, the most differentiated SoC solutions through early access and fast deployment of the industry's newest and best technology advancements.

This collaborative work brought early access to IC Compiler™ II place-and-route technology and now, following continuous innovations from Synopsys, Toshiba has been enabled to deploy Fusion Compiler™—the industry's only RTL-to-GDSII solution—into its internal design flows and broader ASIC design-service offering.

This paper describes how Toshiba and Synopsys worked closely to bring-up Fusion Compiler and deploy it throughout Toshiba's proprietary, class-leading Tachyon Design System. With improved PPA, faster time-to-results and a predictable design flow, this new technology has been validated on our latest, differentiated SoC ASIC products and is being more broadly deployed throughout Toshiba to bring these benefits across our entire solution offering.

Fusion Compiler - The Industry's Only Fully-Integrated RTL-to-GDSII Solution

Tracking the path of Moore's law brings increasingly pervasive designer challenges that span the entire design-to-implementation space. Attaining the optimal PPA in a convergent manner - in the context of these increasing constraints - has become a key focus of leading design teams who need to deliver highly differentiated SoCs. Un-optimized flows-and-methodologies often leave PPA on the table through margins and over-design which is becoming increasingly hard to manage and mitigate for.

Fusion Compiler heralds in a new era in SoC design by leveraging not only the PPA and productivity benefits of the broader Synopsys Fusion Design Platform™ but is the industry's only, fully-integrated RTL-to-GDSII solution. Through the fusing of fast, novel, high-capacity synthesis with proven place-and-route on a single, unified data-model, predictability and PPA are guaranteed. Deployment of common engines throughout enables a full-flow, unified physical optimization framework. This scalable framework is complemented by common, golden-signoff-infused timing, extraction and power analysis technologies that enables best-in-class PPA and the ability for designers to move to a zero-margin methodology.

Toshiba's Industry-Shaping Tachyon5 Design Kit is Fully Integrated with Fusion Compiler

Toshiba and Synopsys recognized a compelling, automotive-market opportunity and extended their already close partnership to enable and accelerate this innovative SoC solution. The Tachyon design kit from Toshiba, is a comprehensive implementation methodology which guides the user from early product development to final design implementation. As part of the partnership, Toshiba adopted Fusion Compiler for the most challenging mega-block designs in advanced automotive SoC design.

The Tachyon5 design kit from Toshiba was developed with Fusion Compiler at its core, bringing fastest time-to-results and highly differentiated PPA. Fusion Compiler provided the tight integration Toshiba needed between early RTL-based architectural refinement and final design implementation. Figure 3 illustrates how Toshiba integrates Fusion Compiler into the Tachyon5 design system with advanced Toshiba SoC design know-how targeted for all Toshiba SoC products including automotive applications.

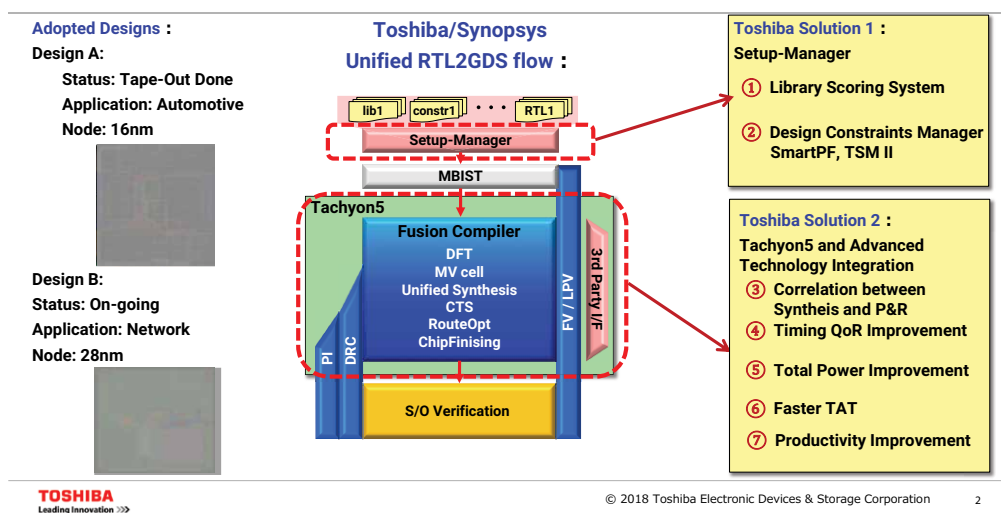


Figure 2: Toshiba Tachyon5 design kit integration with Fusion Compiler (source: SNUG Japan 2018)

Toshiba Tachyon5 Design kit system with Fusion Compiler provides:

- Automatic Library cell characteristic scoring
- Design inputs and design constraints management
- Timing correlation configuration along RTL synthesis, place-and-route, and PrimeTime® static timing analysis (STA)
- New Unified Physical Synthesis (UPS) optimization techniques
- Aggressive power management and reduction
- Improved design turn around time (TAT) with higher productivity
- Automatic parameters/flow sets for nodes (130nm ~ 7nm).
- Handles third parties interfaces flexibility
- Supports second sign-off interface and flow/QoR monitoring system

One of the key elements of the new design system is to minimize over-design by eliminating the margin between RTL synthesis and place-and-route processes. Toshiba and Synopsys could achieve perfect timing correlation between front-end and back-end stages. Figure 4 shows the results of a taped-out mega-block design, Design-A (approximately 4.2M instances). The table captures the perfect correlation between synthesis and place-and-route. Fusion Compiler can achieve this result because it provides a common timer, delay calculator, RC extractor and UPS engines on a compact and efficient common data model.

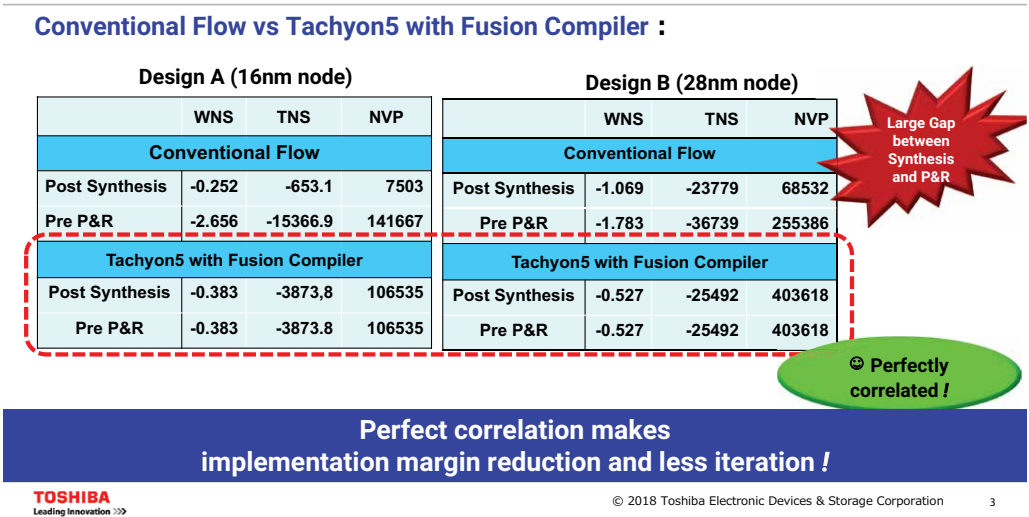


Figure 3: Fusion Compiler with the Tachyon5 design kit showed perfect Timing Correlation (@ Worst Corner) (source from SNUG Japan 2018)

All results and comparison tables are based upon:

- Evaluation and design period: ~January/2018. Taped-out on February/2018
- Conventional flow: DCG M-2016.12-SPx and/or N-2017.09-SPx
- Fusion Compiler RTL-to-GDS flow: v-2.75.x

Fusion Compiler also provides revolutionary, RTL physically-aware synthesis technology to boost synthesis runtime as well as improving PPA target.

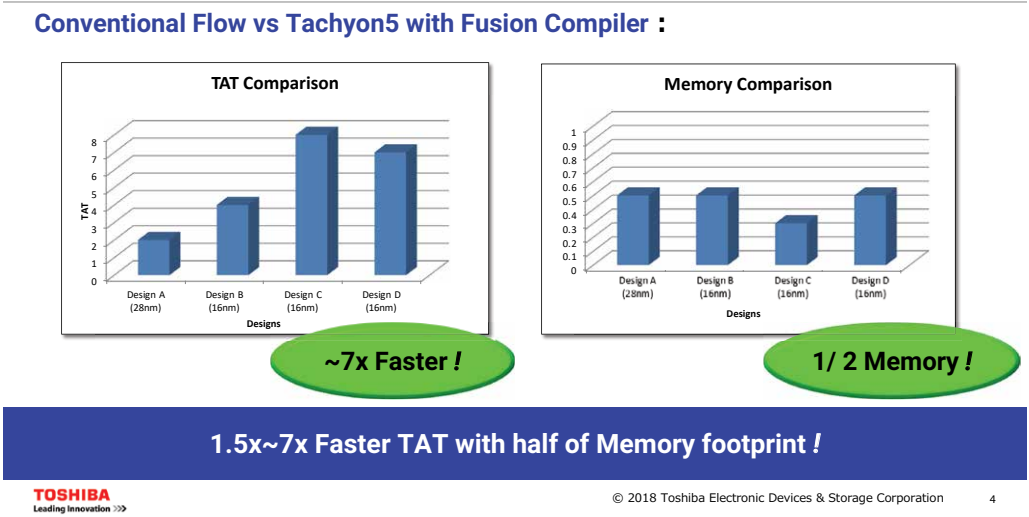


Figure 4: Fusion Compiler with the Tachyon5 design kit synthesis runtime improvement

As shown below, Fusion Compiler delivers on its QoR promise while also reducing runtime on large, complex designs. Figure 4 shows the runtime speedup that was achieved on a taped-out design with Fusion Compiler. Compared to the current synthesis plus implementation approach, it provided 7x faster runtime while improving QoR which is summarized in Figure 5.

Conventional flow vs Tachyon5 with Fusion Compiler :

Design A (16nm)				Design B (28nm)			
Timing result comparison at Pre-CTS				Timing result comparison Pre-CTS			
	WNS	TNS	NVP		WNS	TNS	NVP
Conventional Flow	-0.493	-6329	51057	Conventional Flow	-0.468	-4155	112285
Tachyon5 with Fusion Compiler	-0.138	-142	23655	Tachyon5 with Fusion Compiler	-0.258	-717	17935
Improvement	1 / 3	1 / 50	1 / 2	Improvement	1 / 2	1 / 5	1 / 8

☺ Excellent timing QoR !

Excellent Timing QoR Improvement, TNS = 1/50

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Figure 5: Fusion Compiler with the Tachyon5 design kit timing QoR improvement result after place-and-route

Figure 5 shows that the ultra-fast RTL physical synthesis improved all timing QoR metrics, such as, worst negative slack (WNS), TNS total negative slack (TNS) and numbers of violated paths (NVP) by Fusion Compiler.

Conventional Flow vs Tachyon5 with Fusion Compiler :

Design A (16nm)						Design B (28nm)			
Pre-CTS result						Pre-CTS result			
	Total	HVT	LVT	IVN/BUF	ICG		Total	HVT	SVT
Conventional Flow	2247293	1005286	1242007	372842	46729	Conventional Flow	8615	4762	3853
Tachyon5 with Fusion Compiler	1967549	1139084	828465	242531	13640	Tachyon5 with Fusion Compiler	7803	5104	2699
Improvement	-13%	+13%	-33%	-35%	-70%	Improvement	-10%	+7%	-30%

☺ Significant Area and Power Reduction

Significant Power and Area reduction
Total area= 10% LVT=30%, ICG=70% reduction

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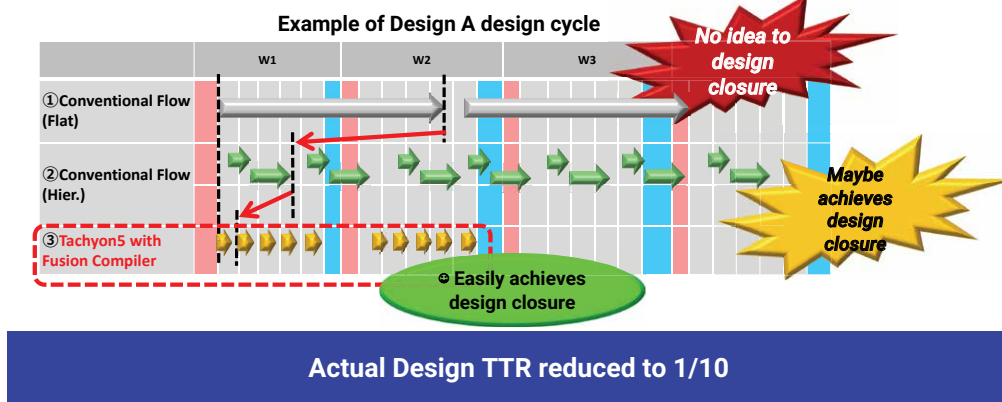
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Figure 6: Fusion Compiler with the Tachyon5 design kit area and power improvement result after place-and-route

The Toshiba Tachyon5 methodology, built on Fusion Compiler, delivered smaller area and lower power on the taped-out design. Figure 6 shows this new approach significantly reduce power by delivering a 13% area reduction with a 33% smaller Low Vth cell count.

What is the actual impact from Fusion Compiler flow :

It's not only tool TAT improvement, tralizes total design cycle reduction.



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Figure 7: Fusion Compiler with the Tachyon5 design kit contributes significant improvement of TTR to 1/10

Through the real design adoption (Design-A), Toshiba and Synopsys confirmed the actual TTR was improved 1/10 by the combination of Fusion Compiler with the Tachyon5 design kit. This impacts the significant design productivity improvement for Toshiba and we successfully tape this challenging design out.

Toshiba Current Activities

Based on this successful tape-out experience that Toshiba and Synopsys collaborated on to bring to fruition, Toshiba is aggressively deploying the Fusion Compiler enabled Tachyon5 design kit for multiple high-value projects spanning nodes from 130nm right down to 7nm.

Summary

Toshiba and Synopsys collaborated to develop a new methodology for advanced SOC designs powered by Fusion Compiler and the Toshiba Tachyon5 design kit. This new comprehensive RTL-to-GDSII design methodology and technology significantly improves designer productivity, as well as, provides higher PPA results. Toshiba will widely deploy the Fusion Compiler with the Tachyon5 design kit on many, upcoming, flagship designs.

Fusion Compiler with the Toshiba Tachyon5 design kit provides:

- 7x Faster runtime in RTL physical synthesis
- 66% WNS, 50x TNS and 50% NVP timing QoR improvement
- 13% Area reduction
- 35% Buffer reduction
- 33% of Low Vth cell usage

To learn more about Fusion Compiler visit: www.synopsys.com/fusioncompiler