

Synopsys TestMAX Family of Test Products

Redefining Expectations for Test

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Introduction

New and rapidly expanding applications, such as artificial intelligence and automotive, are increasing in design size and complexity. These evolving market segments require unprecedented levels of quality and long-term reliability, which has created a fundamental shift in both the importance and need for integration of advanced semiconductor test. Synopsys unveiled a new family of test products that aligns with this shift and addresses overall test challenges. The Synopsys TestMAX™ family of test products delivers innovative test and diagnostic capabilities for all digital, memory, and analog portions of a semiconductor device. The Synopsys TestMAX family contains unique capabilities for automotive test and functional safety, as well as technologies that unlock new levels of test bandwidth and efficiency by leveraging high-speed interfaces common on many designs. A powerful and highly configurable test automation flow provides seamless integration of all Synopsys TestMAX capabilities. These new features, combined with comprehensive support for early testability analysis and planning, hierarchical ATPG compression, physically-aware diagnosis, logic BIST, memory self-test and repair, and analog fault simulation, ensure that the Synopsys TestMAX product family addresses critical test issues while enabling effective test for future demanding applications.

RTL Flow Linked into Implementation

The TestMAX family supports a comprehensive RTL-to-GDSII DFT implementation flow allowing DFT to be integrated early during the RTL design phase or as part of synthesis with Synopsys Design Compiler® or Synopsys Fusion Compiler™.

Synopsys TestMAX Advisor, built on SpyGlass® technology, performs RTL testability analysis and optimization, enabling designers to fine-tune RTL early in the design cycle to predictably meet manufacturing and in-system test coverage goals. The tool's extensive design-for-test (DFT) rule checking and RTL fault coverage estimation capabilities pinpoint testability issues early in the flow, thereby enabling designers to avoid test bottlenecks downstream that can lead to time-consuming design iterations. TestMAX Advisor identifies areas in the design with hard-to-test ATPG faults and provides a report of test points to improve test coverage and reduce patterns and test costs.

TestMAX Manager provides a complete, integrated RTL implementation and verification flow. Figure 1 shows an overview of the primary flow steps and processes. In conjunction with the Synopsys Fusion Design Platform, TestMAX Manager output seamlessly integrates with the Synopsys RTL to GDSII flow. The Synopsys Fusion technology achieves significant quality of results (QoR) through shared engines across tools within the platform. TestMAX Manager via the Fusion Design Platform delivers significant benefits through physical awareness, reordering scan chains based on physical clustering, compressor placement optimization to reduce congestion as well as physical clustering of test points.

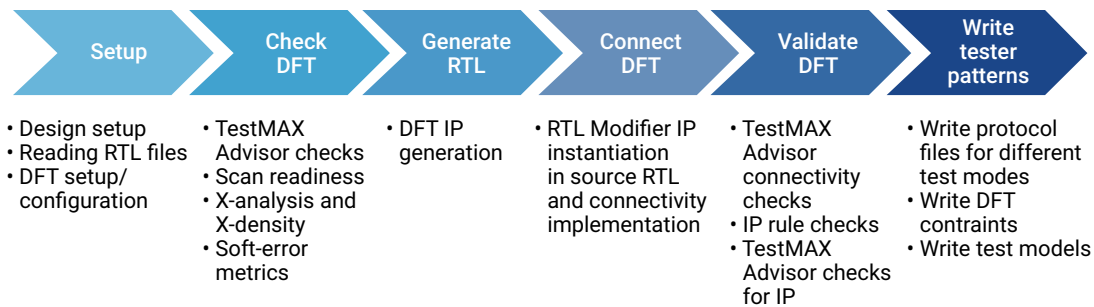


Figure 1: TestMAX Manager flow

TestMAX DFT reduces the costs of testing by providing high test data volume compression. Using Synopsys' patented DFTMAX combinational and sequential compression architectures, TestMAX DFT saves test time and makes it possible to include high defect-coverage test patterns in tester configurations where memory is limited. With the industry's most area-efficient solution, TestMAX DFT has virtually no impact on design timing and results in the same high-test coverage as provided by standard scan. For additional test time and data reduction, TestMAX DFT implements test points within synthesis, via its transparent links to TestMAX Advisor for powerful test point analysis and selection.

Advanced Scan Pattern Generation and Diagnosis

TestMAX ATPG is the leading, state-of-the-art pattern generator that lets design teams meet their test quality and cost goals with unprecedented speed. Pattern generation is built upon algorithms that exploit today's multicore compute servers using fine-grain multithreading. Additional heuristic selection techniques enable optimal results. As a result, TestMAX ATPG delivers an order of magnitude faster runtime, ensuring patterns are ready when early silicon samples are available for testing. Additionally, patterns are typically 25 percent less versus non-threaded techniques, allowing IC design teams to shorten the time and lower the cost of testing silicon parts or, depending on design requirements, increase test quality for the same cost.

Many manufacturing defects will not be caught without additional high defect-coverage tests that specifically target subtle nanometer defects to further reduce defective parts per million (DPPM). TestMAX ATPG utilizes advanced fault models such as standard and slack-based transition, cell-aware, static bridging, dynamic bridging, path delay, and hold-time to generate high defect-coverage test patterns. Some of these models use data generated by other Fusion Design Platform tools. For example, cell-aware models leverage physical data from StarRC extraction and detailed timing information from HSPICE simulations for TestMAX ATPG to target timing-critical defects inside.

TestMAX ATPG limits power consumption during scan and capture by automatically reducing switching activity to levels consistent with normal operation, based on designer-specified power budgets. Scan testing typically increases transistor switching activity by many times their peak functional-mode levels, leading to excessive power consumption. Too much power consumption during test can lead to the failure of good devices on the tester and unnecessary yield loss. Power reduction is achieved without compromising test coverage. For more aggressive power-savings, TestMAX ATPG also supports hardware-assisted shift power reduction, which decreases average shift power and pattern count compared to an ATPG-only approach using independently controlled scan chain groups implemented with TestMAX DFT.

TestMAX Diagnosis is the companion to TestMAX ATPG to determine likely silicon defect locations of failing devices. While the basic goal of delivering fully functional parts requires only stop-on-first-failure testing, further testing of failing devices can provide useful, detailed information as to why the part failed. When this data is collected and analyzed over a significant volume of failing parts, systematic issues causing lower manufacturing yields can be statistically separated from the “noise” of random defects. Correlating the defect locations from a large number of devices, prioritizing those with the highest yield impact, and taking immediate corrective action has enormous potential cost benefits, and enables faster time to market when new designs are being ramped up in manufacturing. This first step in the process starts with diagnostics of a single failed die with TestMAX Diagnosis. To provide future defect isolation within a library cell, TestMAX Diagnosis supports the use of cell-aware fault models. These fault models are created with utilities for TestMAX ATPG. Once available, cell-aware fault models are utilized on any type of TestMAX ATPG patterns and not limited to cell-aware test patterns. The defect search area within the cell is often reduced by 3-5X compared to standard diagnostic techniques. The result is faster turn-around time for physical failure analysis.

For emerging process nodes there is a higher probability that during scan testing of a design, more than one scan chain will capture ‘faulty’ values - binary values different than what is expected if the chip were fully functional. Scan compression raises the difficulty of diagnosing which faults are associated to specific chains because of the XOR gates used to compress the chain data. TestMAX Diagnosis utilizes masking logic to provide chain isolation, ensuring diagnosability of multiple failing scan chains (see Figure 2).

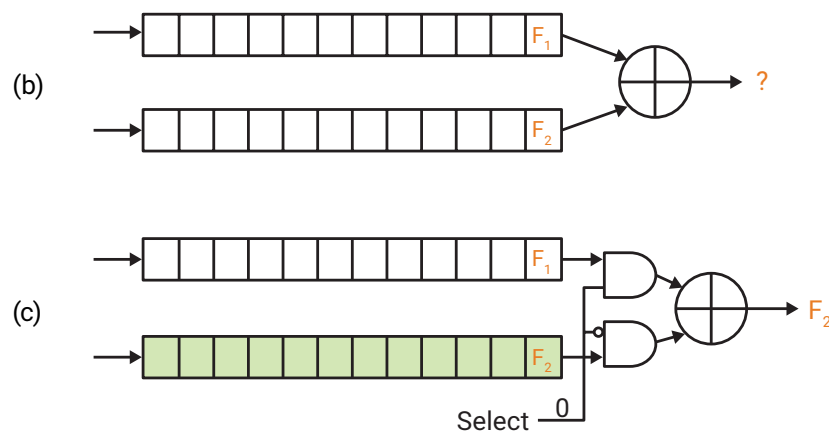


Figure 2: TestMAX Diagnosis utilizes compression hardware to isolate multiple failing scan chains

Advanced Automotive Functional Safety Solutions

The TestMAX family addresses the needs of the rapidly evolving automotive segment by providing key innovations related to early functional safety analysis as well as advanced in-field test.

Functional Safety Analysis

Transient faults caused by soft errors can cause catastrophic failures during the operation of a safety-critical electronic device. The probability that a soft error can propagate to a safety-related signal is measured by the Single Point Fault Metric (SPFM) defined by the ISO 26262 functional safety standard. Minimum required SPFM values are documented by the standard for each of the defined automotive safety levels.

Synopsys TestMAX FuSa performs soft-error analysis early in the design flow to provide guidance for design changes resulting in ISO 26262 functional safety metric improvements. Analysis can be performed either on RTL or gate-level netlists, minimizing impact to design schedules. TestMAX FuSa uses static analysis to estimate the probability that a soft error can reach a safety-related signal. It calculates controllability and observability of logic signals in functional mode and supports multi-time-frame analysis with user-defined parameters to control the number of propagation levels. The calculation is done with respect to any user-specified safety related registers and outputs and can be performed on any portion of the design, including top level. This provides the ability to identify and efficiently address SPFM hotspots. At the lowest level, a list of the design’s flip-flops is generated and ordered based on each flop’s contribution to SPFM loss (Figure 3). This makes it easier to determine the minimum number of regular flops that need to be replaced with error-tolerant flops to achieve the desired SPFM value. Flop substitutions are then performed within the synthesis and place-and-route flow based on the generated minimum list. Alternatively, larger blocks of logic contributing as a whole to SPFM loss can be managed using other techniques, such as adding redundant blocks or through the addition of safety monitors.

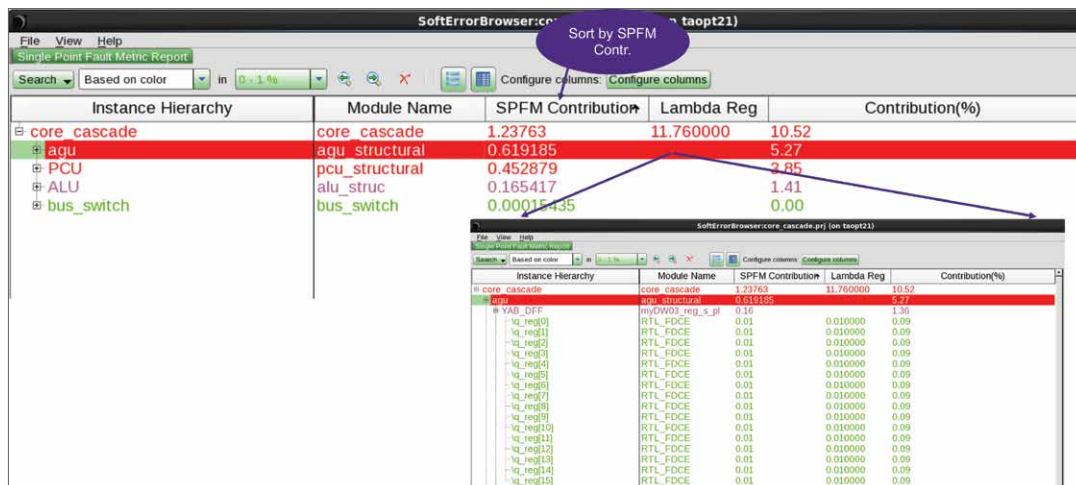


Figure 3: SPFM Browser identifies the blocks in the design with the highest probability causing functional safety failure

X-tolerant Logic BIST

To meet mandated functional safety levels, automotive devices must typically implement self-test mechanisms that operate at key-on and increasingly during the vehicle's operation. Logic BIST is usually used to check for safety faults in device logic but is unable to tolerate unknown circuit states, such as those arising due to post tape-out timing anomalies. Synopsys TestMAX introduces the industry's first X-tolerant logic BIST solution that operates in the presence of unknown states, removing the need to eliminate all Xs in a design, which can negatively impact cost and time-to-market. Figure 4 shows an architectural overview of the XLBIST logic implementation. The solution uses a novel re-seeding approach to selectively mask scan chain outputs during unloading into the MISR. This ability ensures that self-test will operate on the manufactured device with little impact to the operational time and fault coverage for most scenarios.

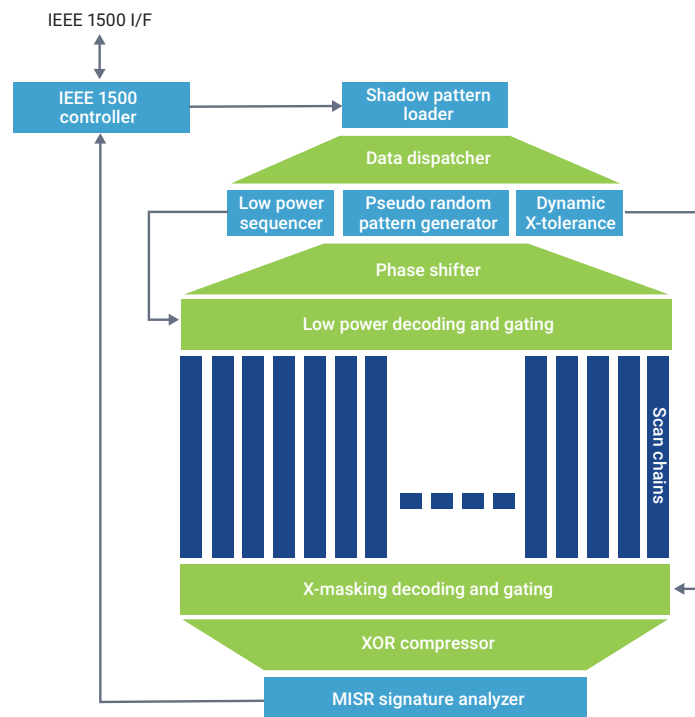


Figure 4: TestMAX XLBIST architecture

With the ability to re-seed the pseudo-random pattern generator (PRPG), dynamic x-tolerant logic, and lower power sequencer in an automatic, intelligent manner, it is possible to achieve significant increases in fault coverage in less time compared to traditional logic BIST solutions. Figure 5 shows a typical comparison of coverage versus pattern count for a given number of pattern seeds. As the number of bits required for a seed and associated response is in the order of 100s of bits, multiple seeds can be stored on-chip for in-system test or supplied externally.

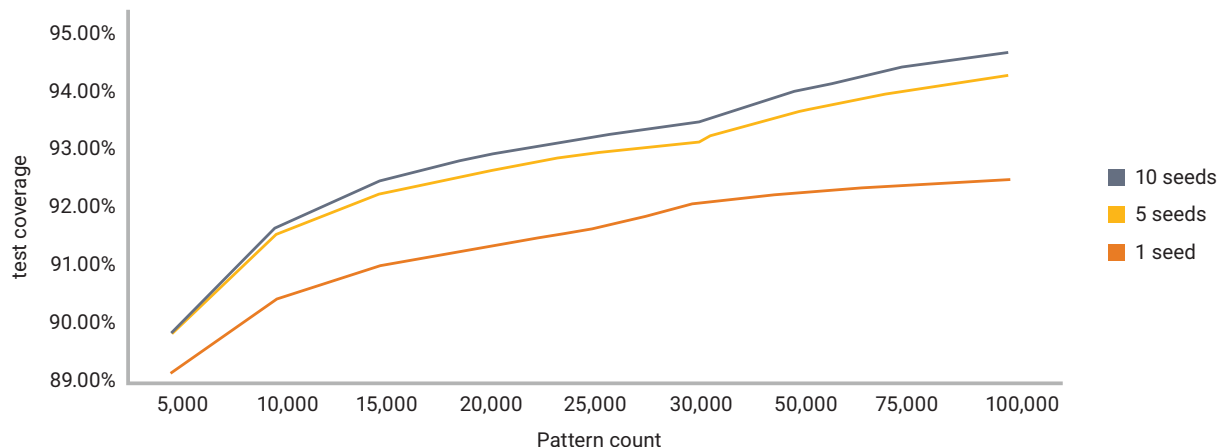


Figure 5: TestMAX XLBIST achieves high coverage with multiple seeds

Adaptive High-Bandwidth Test

Managing manufacturing test times has become increasingly problematic as design sizes continue to grow. Test application bandwidth is generally not scaling due to the limited growth in test pins and related clocking frequencies. Synopsys TestMAX ALE and TestMAX SLT make available a game-changing solution to this problem by leveraging high-speed functional interfaces like USB and PCI Express that exist on most devices today. Synopsys TestMAX provides the ability to apply all manufacturing tests through one or more of these functional interfaces, resulting in almost unlimited test bandwidth while reducing, if not eliminating, the overhead of dedicated test pins. Since functional interfaces are used, all tests become fully portable and can be used at all stages of the product life-cycle.

TestMAX SLT generates an on-chip interface between the existing high-speed interface IO (i.e., USB, PCIe, etc.) to the DFT logic (see Figure 6). This interface is necessary in order to re-use the HSIO for structural test and also serves as a potential interface mechanism for system-level tests. The specific type of HSIO incorporated into a design is dependent on its functional application. Indeed, the same design may have variants in which different HSIO are employed. To accommodate this and remain independent of the HSIO, the SLT logic interface utilizes the Advanced eXtensible Interface (AXI) interconnect serving as a slave to the HSIO. The data feeds from the AXI through a FIFO that accommodates the packet length suitable for the design's DFT. The SLT interface also contains logic to transform the data packet into the necessary DFT signals, including scan in data, scan out data, scan enable, and test clock. The scan out data port is an input into the SLT interface, enabling captured scan data to be processed into a packet using digital logic symmetrical to that of the AXI input processing logic.

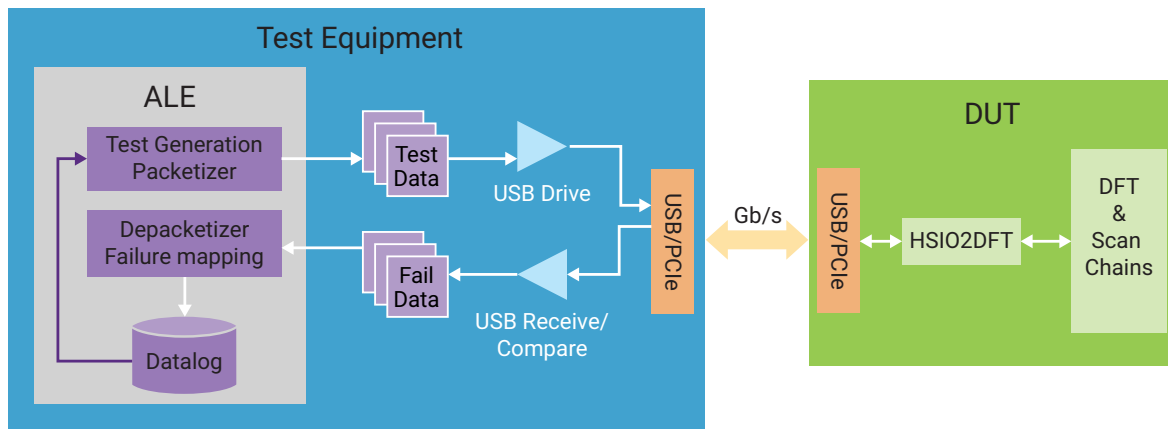


Figure 6: High-bandwidth test interface

TestMAX ALE provides the software interface to the HSIO similar to a software device driver. The main purpose of TestMAX ALE is enabling communication between the operating system file I/O and the software layer driving the host HSIO. Specifically, TestMAX ALE processes standard scan data in the IEEE 1450 (STIL) format and then packetizes the data for communication to the HSIO-driver software. Additionally, TestMAX ALE receives the packetized scan output data and processes it for viewing as well as file output. Several output formats (ex. STDF-v2007) are supported to avoid further processing by external programs utilizing data such as yield analysis tools. TestMAX ALE runs in conjunction with different tester environments and operating systems to ensure maximum portability.

Most Comprehensive Set of Test Products

The TestMAX family of products delivers the industry's most comprehensive set of test and DFT capabilities. A brief description of each TestMAX product is listed below. Please visit www.synopsys.com/testmax for more details on any of these products.

Product	Description
TestMAX Manager	Provides a comprehensive RTL integration flow for all TestMAX DFT; a Tcl-based framework enables flow automation and customization
TestMAX FuSa	Fast functional safety analysis to identify and address hotspots early in the design cycle and guide efficient design changes
TestMAX Advisor	Extensive RTL DFT rule checking analysis that help designers pinpoint testability issues early in the flow
TestMAX DFT	Physically-aware, timing-aware and power-aware DFT insertion ensures best PPA results
TestMAX SMS	STAR Memory System™ provides full memory defect coverage with minimum test time and efficient on-chip repair
TestMAX XLBIST	Enables logic BIST without the need for X-clean design, maximizing in-system test coverage and minimizes test times
TestMAX Access	Provides efficient access to on-chip DFT structures for in-system test and diagnosis
TestMAX ATPG	Fast generation of high-coverage test patterns; provides lowest test time for given coverage than any other solution
TestMAX Diagnosis	Layout-aware diagnosis of scan failure data provides accurate identification of defects; Results directly feed into Yield Explorer®
TestMAX SLT	On-chip interface between USB/PCIe and DFT enables very high test application bandwidth without the need of dedicated test pins
TestMAX ALE	Adaptive Learning Engine enables test efficiency improvements over time based on the analysis of past test results
TestMAX Vtran	Translation between various patterns formats ensures robust links between different tools in the design and test flow
TestMAX CustomFault	Fast analog fault simulation provides test coverage of analog and mixed-signal blocks needed for automotive applications