White Paper

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Achieving Faster Time to Tapeout with In-Design, Signoff-Quality Metal Fill

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Executive Summary

Many semiconductor foundries use design rule check (DRC) physical verification tools to generate metal fill. This allows the foundry to generate fill data and verify their corresponding DRC rules all in a single runset. Usually these fill creation flows read GDSII or other standard data formats and create fill data in the same format. Unfortunately in such cases, the design has to be streamed back into place and route tools to assess the timing impact of fill polygons. This process leads to excessive iterations between design and layout verification to meet timing requirements and DRC signoff requirements.

By providing foundry signoff metal fill generation in an interface that is familiar to the place and route engineer, a cumbersome collection of design tasks is turned into a pushbutton flow. The costly stream out and stream in process is eliminated when the layout verification tool operates directly within the place and route environment. Additionally, control over insertion and deletion of fill layers provides added benefit for engineering change orders (ECOs) when minimal schedule delay is imperative. Timing impact is considered as the fill is generated during the implementation stage so that both DRC's and timing are taken into account simultaneously. Achieving correct-by-construction results during implementation significantly reduces time to tapeout and avoids schedule delays. This paper presents a pushbutton flow to generate timing-aware, signoff quality metal fill during place and route.

Introduction

Until recently, layout engineers could delegate to other teams the responsibility for chip finishing steps such as metal fill. This is no longer the case as technology nodes become smaller and smaller and as chip frequencies go higher. The added metal fill can easily disrupt timing and therefore needs to be analyzed during the place and route stage. In addition to technical issues, aggressive time-to-market pressures demand processes and tools that are more efficient and intelligent. This paper will explore in details technical problems related to generated fill and possible solutions.

Today's Sign-off Metal Fill Challenges

Most place & route tools have some capability of generating fill. Although they may have algorithms that come close to generating the correct density, they are not a sign-off tool and are not intended to guarantee sign-off. Foundries rely on physical verification tools since they are built on efficient polygon engines that work well hierarchically to produce correct data quickly. The designer is left with two possibilities:

- Use the place & route tool to generate a first attempt at fill and do a second level fill with the verification tool or use hand-modification to achieve DRC closure
- Let the verification tool generate the fill and ignore timing effects

Either scenario often requires several iterations of exporting and importing the layout database between point tools to achieve convergence on an acceptable fill solution. Figure 1 shows the time consuming and cumbersome flow of going from a place & route tool to a separate, non-interfacing physical verification tool to generate fill. After completing place & route of a design, the engineer needs to first verify that the design is DRC clean. The whole design is then streamed out and read in by a physical verification tool which generates the fill. After the fill has been created, it is necessary to stream out of the physical verification tool, so that the fill can be read back into the place and route tool to verify that the timing has not been affected. Of course, there is always the possibility of ECOs that could require fill to be regenerated. This necessity of going back and forth between tools will need to be repeated every time an ECO is required. This flow is difficult and extremely time consuming.

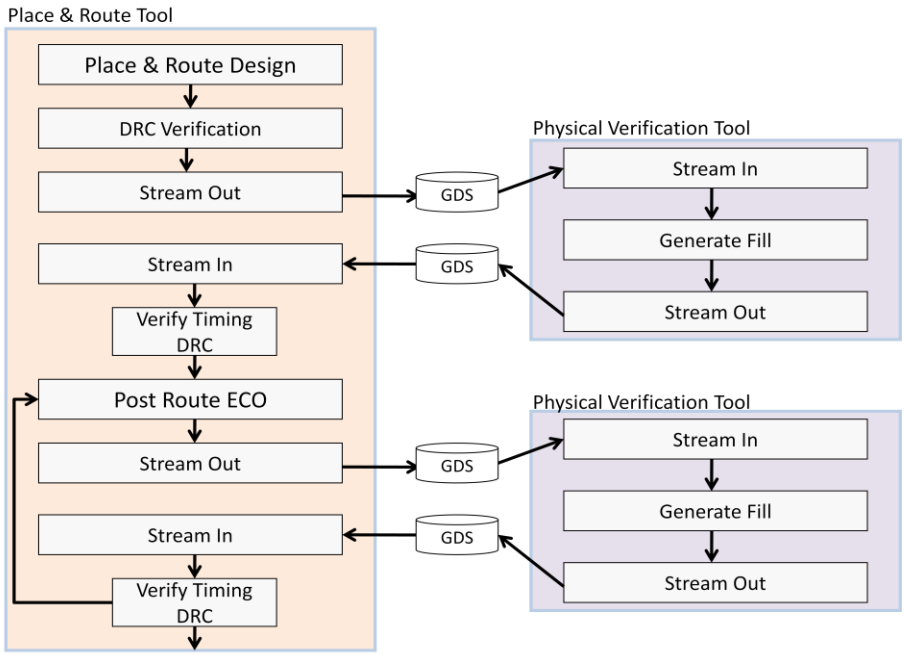


Figure 1: Typical place and route to physical verification flow

In addition, convergence between DRC clean and minimal timing impact of fill is difficult and time consuming when using different data representations between a place and route tool and a physical verification tool. As an example, consider the following case study of fill generated for a 2.3 by 2.3 mm^2 45 nm design having 1.6 M cells and a 2.14 GB GDSII file. Before generating fill, the design had a worst negative slack of -0.07 and a total negative slack of -25.03. Density violations were found on metals 4, 5 and 6. The following summarizes the results of each fill generation iteration for a timing path group:

1. On the first attempt, all metals were given the two times the minimum spacing to critical nets. All density violations were removed, but the worst negative slack and the total negative slack worsened.
2. On the second attempt, a spacing of 0.4 m was specified. In this case, the two slack values worsened and there were density violations on Metal 4 and Metal 5
3. On the third iteration, all spacing to critical nets on Metal 1, Metal 2, Metal 3, and Metal 6 were set at 1 µm, whereas the spacing for Metal 4 and Metal 5 were set at two times the minimum spacing. This time, all density violations were eliminated, but both the worst negative slack and the total negative slack worsened
4. Finally, a large spacing to critical nets, 1 µm, was specified. This spacing improved and timing, (as measured by worst negative slack and total negative slack, did not deteriorate. There remained density violations for Metal 4 and Metal 5 along the boundary of the block, but these are acceptable since the block in question will be placed in the top block and density will be corrected by the placement of neighboring blocks.

As can be seen, closing timing and generating fill to meet all density requirements takes many iterations. For this case study, each iteration required approximately 6.5 hours (1 hour for fill generation, two 2.5- hour runs for timing analysis and 20 minutes for the density check). Adding this time for all the iterations totals approximately twenty-six hours of processing.

Integrating Metal Fill Within the Design Process

To resolve the issues discussed above, it is necessary to find a solution that allows users to converge on DRC correct fill while checking for timing impact within an integrated tool environment. Figure 2 shows the fill flow if it could be run within such an environment. All fill would be generated within the environment of the place and route tool where timing would be verified and still be DRC clean. It would no longer be necessary to stream in/out many times between two tools, thus eliminating a first level of time-consuming iterations.

In addition, a second level of iterations would be greatly reduced if the fill generated was timing aware. If critical net information is known by the tool creating the fill polygons, adverse effects on the timing of the design can be avoided automatically.

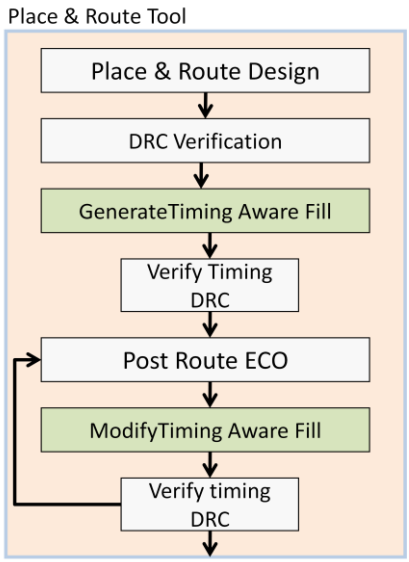


Figure 2: Integrated Metal Fill Flow

The high-level requirements of such an integrated fill solution are as follows:

- Fill needs to be generated within the native place & route environment using recognizable data structures
- Fill generated within the place & route environment must be DRC clean by construction
- Ability to generate fill that minimizes the impact on timing
- Easy solution to use, setup and learn
- It should be possible to incrementally modify fill in response to ECOs to reduce turnaround time and schedule impact
- Users must be able to view the generated fill within the place and route tool

IC Compiler/IC Validator In-Design Signoff Metal Fill Flow

To solve the complexities associated with using two point tools to create fill, Synopsys has integrated its signature implementation tool, IC Compiler, with its next generation physical verification tool, IC Validator. This solution allows users to create sign-off quality fill that is DRC clean, verify the timing impact of that fill, avoid creating fill near critical nets, and eliminate unnecessary streaming in/out while remaining within the native Milkyway database environment.

Figure 3 shows how IC Validator's fill generation and DRC checking capabilities are integrated into IC Compiler. Once a design has been routed and is DRC clean, an IC Validator fill runset is specified using a simple set_physical_signoff_options form. Next, fill generation is launched from the signoff_metal_fill form which invokes the foundry provided runset. The fill generated will be DRC clean by construction since the signoff fill runset is provided by the foundries. The resulting fill is placed hierarchically to minimized disk space usage of the resulting design and is saved into IC Compiler's Milkyway database. Now that the design contains fill, the layout engineer can do timing analysis. If a post-route ECO is required, fills can be regenerated for all layers or only those metal layers that were part of the ECO, using the same IC Validator runset.

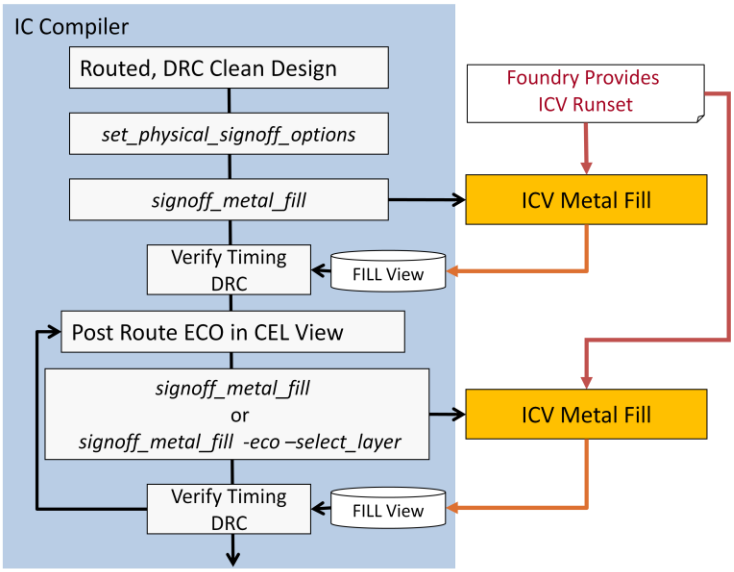


Figure 3: In-Design Metal Fill Flow in IC Compiler

User Benefits

Using the IC Compiler/IC Validator signoff metal fill flow, projects benefit from large time savings. Figure 4 summarizes the benefits realized on three different designs using fill generation for individual metal layers and using area-based fill generation during ECOs. As can be seen in the diagram, having the ability to generate fill incrementally for only one layer saves considerable time compared to full fill generation. When regenerating the top metal layer, the process is at least seven times faster. When using area based fill, the fill process runs more than twelve times faster as compared to full fill generation.

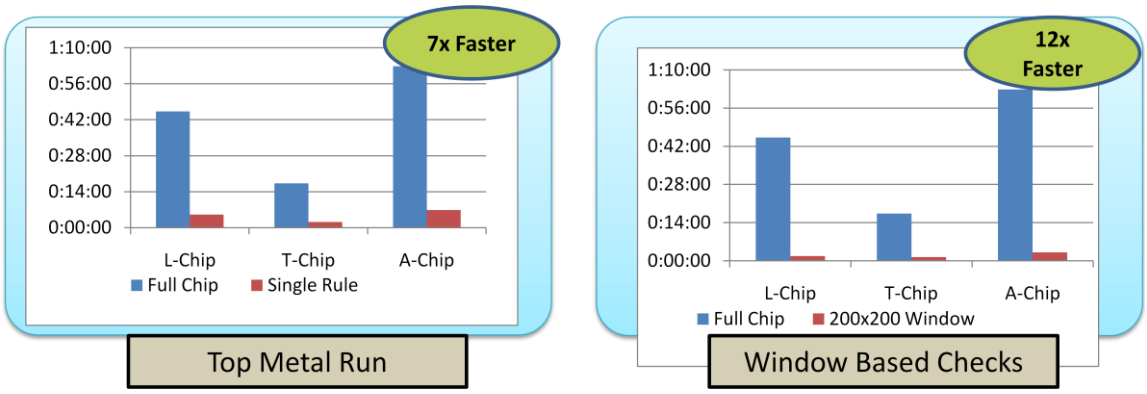


Figure 4: Faster Fill Generation

The time savings demonstrated above add up dramatically over the life of a project. Consider for example the metal fill process for designs having respectively 1.7 M instances, 5.4 M instances and 17.8 M instances. For each design, four 100 by 100 μm^2 area ECOs and three individual layer ECOs were done. Each design will benefit from:

- Time savings from avoiding streaming in and out of tools since the fill is generated directly into the Milkyway database.
- Time savings from running only area-based ECOs instead of running the full area. In addition, you also save stream out time.
- Time savings from running only layer-based ECOs instead of running all layers

Figure 5 shows a linear relationship between the stream in/out time savings and the size of the design. By remaining within the Milkyway database, for each of the seven ECOs, the costly stream in/out time (which increases with the size of the design) is saved. For the largest design, close to thirty hours were saved from not streaming in/out. The graphs in Figures 6 and 7 show an exponential time savings in terms of design size. In other words, the proportional time savings for area-based and layer-based fill becomes larger as the design size increases.

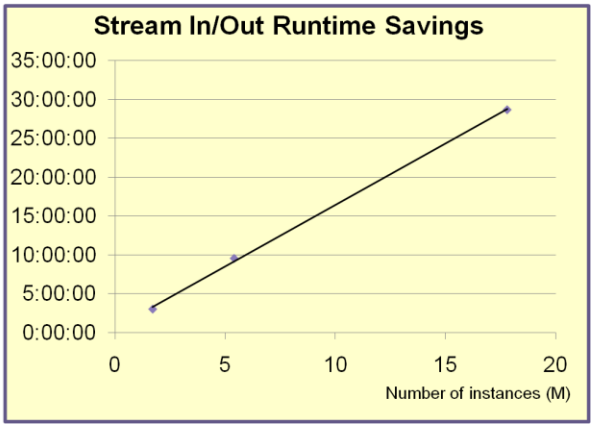
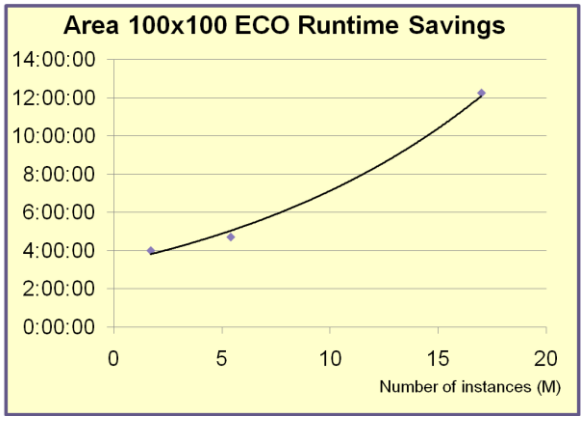
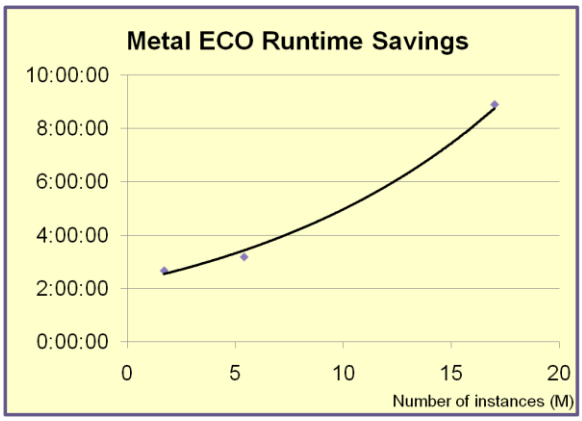


Figure 5: Linear Relationship Between the Stream In/Out Time Savings





Figures 6 and 7: Time Savings For Area ECOs and Layer ECOs

Table 1 shows the total savings for each design which is calculated by adding the stream in/out savings, the area based ECO savings and the layer based ECO savings. These add up to considerable amount of time. Almost fifty hours were saved for the 17.8 M instances design.

	Stream In/Out Savings	Area Based ECO Savings	Layer Based ECO Savings	Total Savings
1.7 M instances	**3:02:13**	**4:00:20**	**2:40:31**	**9:43:04**
5.4 M instances	**9:34:37**	**4:42:58**	**3:11:23**	**17:28:58**
17.8 M instances	**28:42:51**	**12:15:51**	**8:54:18**	**49:53:00**

Table 1: Total Time Savings

Summary

The IC Compiler/IC Validator In-Design Signoff metal fill feature provides a seamless solution to create, view and modify fill without having to leave the IC Compiler environment. Because this solution is based on the foundry' signoff metal fill runsets, the resulting fill meets density requirements and is DRC clean by construction. Hierarchical fill minimizes disk space usage. This flow is easy to set up and use, and it supports layer and area based ECOs flows. This solution helps generate fill which minimizes timing impacts. Because the signoff fill is generated directly into the Milkyway database, it is no longer necessary to stream in/out of different applications saving potentially weeks of work over the life a project.

To find out more about Synopsys and IC Validator, visit http://www.synopsys.com/icvalidator