White Paper

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Extraction Techniques for High-performance, High-capacity Simulation

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Executive Summary

Today's advanced process technologies and faster time-to-market schedules are pushing the limits of verification tools. Post-layout simulation runtimes are increasing 2x to 4x with every new process generation as chip transistor counts double and new parasitic effects come into play. Designers of custom digital, analog/mixed-signal (AMS) and memory integrated circuits (ICs) must now manage an ever-increasing volume of post-layout data while meeting the razor-thin design margins and tight project cycle times. These conflicting challenges are driving the need for more accurate and efficient parasitic extraction and simulation solutions to accelerate verification and achieve first time right silicon. The Synopsys StarRC™ extraction solution offers a wide range of features to boost the simulation performance and capacity of transistor-level designs while preserving signoff accuracy. This paper presents these innovative extraction techniques for high-performance and high-capacity simulation.

Introduction

Each new generation of process technology demands increased transistor-level accuracy, as well as simulation performance and capacity. Nanometer technology scaling enables designers to integrate more functionality but this integration comes at a cost. New materials and sub-wavelength manufacturing processes used for nanometer scaling have pushed the process dimensions to atomic-levels, thus requiring a very high-level of modeling accuracy to account for even the slightest process variations. Furthermore, the use of new device structures and an increasing number of metal layers are introducing millions of new parasitic effects in designs. The parasitics are also becoming "context-specific," that is, they are becoming more sensitive to the layout environment. In general, advancing process technology is magnifying several device and interconnect parasitics considered secondary in previous technologies to primary factors affecting circuit behavior. For instance, interconnect and device parasitic effects are estimated to account for over 60 percent of the delay at 28-nm (see Figure 1). Consequently, design margins (timing, noise, and power) are decreasing with technology progression, thus making accuracy an even more critical requirement for parasitic extraction and simulation tools.

However, increased accuracy is not the only requirement at advanced process nodes—productivity is an even more important requirement. The project cycle times are shrinking or remaining constant at 12 to 18 months, typically, but the chip transistor-counts and simulation runtimes are continuing to increase at each new process node. Also, the number of post-layout simulation runs is increasing with the increase in the number of process corners needed for timing, signal integrity and power signoff.

As a result, in today's environment nanometer process designers are faced with ever-increasing accuracy requirements, potentially unmanageable volumes of data (billions of transistors and billions of parasitics) and a severe loss of productivity. To ensure a high-yielding successful silicon design and to meet time-to-market constraints, IC designers need an advanced parasitic extraction solution to boost simulation performance and designer productivity, while delivering signoff accuracy. In addition, they need a solution that is versatile enough to manage the full design spectrum ranging from custom digital and custom AMS to large memories and SoC designs.

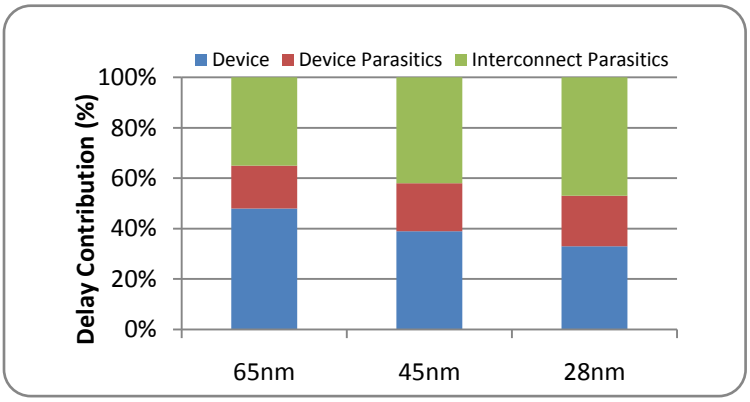

Figure 1: Parasitics have an increasing impact on delay (>60%) at advanced process nodes[1]

Post-layout Simulation Challenges

IC designers face three inter-related challenges in post-layout simulation, as listed below:

- Increasing extraction runtime and memory
- Increasing parasitic netlist size
- Increasing simulation runtime and memory

As the number of transistors increases, the number of nets in the design also increases proportionally. This means that the extraction tools need to extract, manage, and pass much more data to downstream simulation tools, resulting in an increase in parasitic extraction runtime. However, simulation runtime and capacity create larger bottlenecks in post-layout verification compared to parasitic extraction. Simulation runtime and capacity are directly related to the parasitic netlist size as well, that is, to the number of parasitic elements or nodes in the generated netlist. A full-chip parasitic extraction of all nets in a design can lead to unnecessary simulation inefficiency without improving accuracy. In order to meet this challenge, the extraction tools must have the ability to selectively extract only the nets that are important for circuit behavior and netlist only the parasitics that are needed for accuracy.

Another challenge is associated with the varying simulation methodologies and verification goals, due to the designer's specific application needs. For instance, designers may want to take advantage of the pre-layout schematic netlist hierarchy and use hierarchical back-annotation to boost simulation performance. They may also want to trade off accuracy for higher performance and capacity. Consequently, the extraction and simulation tools must have the ability to support various verification flows and provide adequate flexibility to make necessary accuracy vs. performance and capacity trade-offs, if needed.

Overall, post-layout simulation flows have multiple productivity challenges. The parasitic extraction tools must offer advanced techniques to optimize and address all key areas of bottlenecks—extraction runtime and capacity, parasitic netlist size and simulation runtime and capacity.

StarRC Features to Accelerate Simulation

Synopsys' StarRC parasitic extraction tool provides designers with an innovative set of features and techniques to boost simulation performance and capacity for their custom IC and memory design applications. These features and techniques are proven on customers' real design cases and have demonstrated up to 10x acceleration in simulation performance for most applications. In particular, StarRC's exclusive interface with Synopsys' CustomSim™ simulation solution provides unique productivity advantages to the users of the two tools. Some of the proven StarRC extraction techniques to increase post-layout verification productivity are presented in this paper, as follow.

[1] Source: IITC Short Course 2008/Nagaraj NS/Texas Instruments Inc.

- Active node extraction and simulation with CustomSim
- Post-layout acceleration with CustomSim hierarchical back-annotation
- Hierarchical parasitic extraction
- Selective parasitic extraction
- Selective parasitic netlisting

These techniques alleviate productivity challenges throughout the verification flow by addressing the key post-layout simulation challenges, as explained above: extraction runtime and capacity, parasitic netlist size, and simulation runtime and capacity. The following sections describe the techniques in detail and highlight the benefits of each for specific design applications.

Active Node Extraction and Simulation

StarRC's active node back-annotation flow with CustomSim provides an order of magnitude performance and capacity benefit for large transistor-level designs. Designers performing post-layout simulation may be sacrificing performance by extracting all nets in the design and passing full parasitics information to downstream simulators, even though only a fraction of the nets may actually impact timing or accuracy. This is especially true for signals that are not switching or might be inactive during the course of the simulation period. A comprehensive "all net" extraction may not be necessary in such situations, since the parasitics have no effect on circuit performance or on the functionality. Increased data volume only results in an increased extraction runtime, netlist size, and decreased simulation performance with no meaningful gain in accuracy or silicon predictability. This is particularly applicable to memory designs; a memory (such as an SRAM) generally has a small portion that is accessed at a given time, thus making memory designs very attractive for an active node extraction and simulation flow.

The active node flow between StarRC and CustomSim is shown in Figure 2. The flow consists of a push-button command in CustomSim that generates a list of nodes with voltages exceeding a user-specified value in pre-layout simulation. StarRC then directly reads the list and extracts the active nets and the nets coupled to the active nets. The extraction of the active nets only and its dominant coupling neighbors significantly reduces the runtime, as well as the netlist size while guaranteeing accuracy on each extracted net. As the simulation runtime is proportional to the number of nodes and parasitic elements in the netlist, the reduced netlist size improves simulation performance as well. In some design cases, this can reduce the extraction task from hundreds of thousands of nets to only a few thousand nets, thus significantly accelerating simulation. The StarRC and CustomSim active node flow is proven on large transistor-level designs, yielding greater than 10x productivity benefit, as shown in Figure 3.

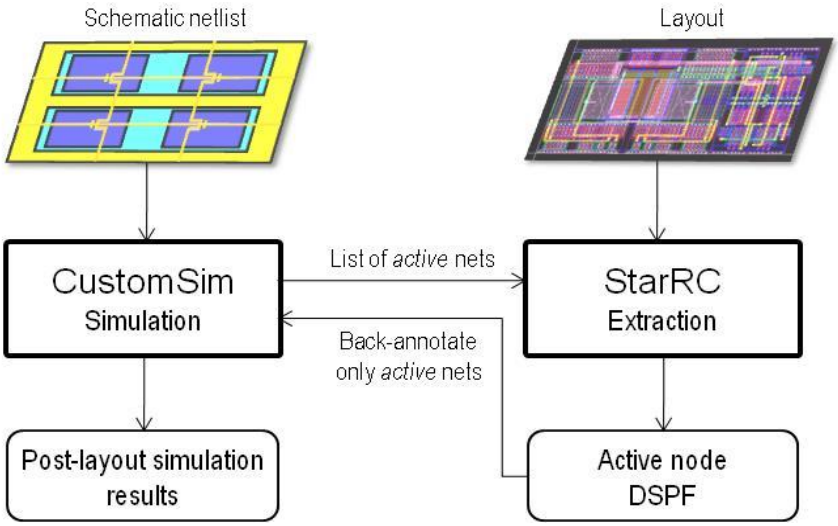

Figure 2: The active node flow between StarRC and CustomSim delivers push-button productivity

Custom IC Design	Flat flow	Active node flow	Results
Nets	274K	3.66 K	~1.3%
Timing delay	2.6535 ns	2.6451 ns	~0.32%
Simulation runtime	6.75 hrs	0.75 hrs	8.4x
Simulation memory	5568 MB	424 MB	13x

Figure 3: The active node flow enables significant simulation performance and capacity boost for large transistor-level designs[2]

Post-layout Acceleration with CustomSim Hierarchical Back-annotation

StarRC offers industry-leading performance and capacity combined with silicon-accurate flat parasitic extraction. StarRC's flat full-chip extraction in conjunction with CustomSim's hierarchical back-annotation enables designers of large memory and custom ICs to achieve the best combination of fastest simulation turn-around time and golden signoff accuracy.

Designers typically reuse the pre-layout simulation test-benches based on the schematic netlist for their post-layout simulation with the extracted parasitics. Hierarchical simulation in CustomSim is driven by the schematic netlist hierarchy, as well (see Figure 4). CustomSim takes advantage of the natural design hierarchy to provide the highest-efficiency simulation. CustomSim's advanced Post-layout Acceleration (PLX) option includes isomorphic hierarchical back-annotation technology that allows designers to easily annotate the post-layout parasitics onto the pre-layout schematic netlist, while preserving the original hierarchy. Combined with the flat extraction parasitics from StarRC, this offers the most effective flow to achieve the twin goals of higher simulation performance and signoff accuracy. StarRC's flat extraction technology accounts for all neighboring net coupling capacitances as well as thickness and width variation effects that are essential for signoff accuracy. On the other hand, the PLX technology provides the maximum annotation of the detailed parasitics using design matching of the post-layout netlist and schematic netlist. Figure 5 illustrates the benefits of StarRC's accurate flat extraction and hierarchical CustomSim back-annotation flow to post-layout simulation. As shown in the figure, the flow enables significant improvement in simulation performance with no change in accuracy. It is important to note that the majority of the improvement in the simulation runtime when using hierarchical back-annotation is during the transient analysis stage. This is due to the fact that CustomSim back-annotates the parasitics onto the original schematic netlist as explained above, thus allowing the simulation to take full advantage of the design hierarchy.

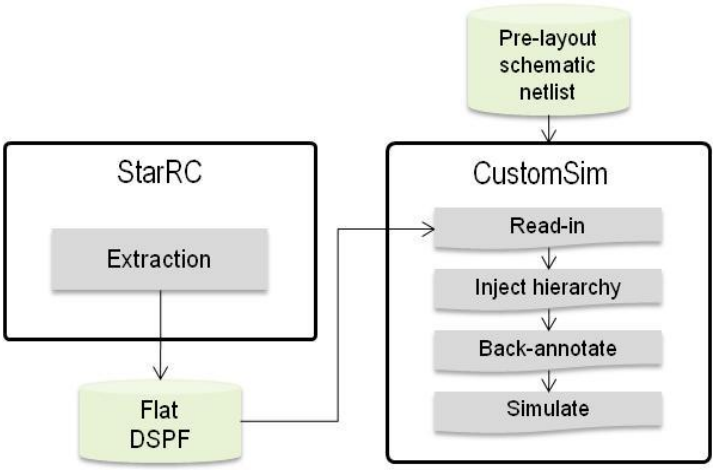

Figure 4: StarRC and CustomSim hierarchical back-annotation flow enables schematic netlist efficiency in post-layout simulation

[2] Source: Synopsys, Inc. April 2009

Figure 5: Flat extraction and hierarchical back-annotation accelerates post-layout simulation and preserves accuracy

Hierarchical Parasitic Extraction

StarRC's hierarchical extraction and netlisting offers circuit designers another option to improve their post-layout verification productivity. For most analysis, a flat parasitic extraction with hierarchical back-annotation provides the best combination of accuracy and performance. However, in cases such as the reliability analysis of large memory or custom system-on-chip (SoC) designs, designers may need to extract billions of signal and power net parasitics. Flat parasitic extraction, though most accurate, could be time-consuming in such cases; therefore, designers may prefer hierarchical extraction to speed the parasitic extraction process. StarRC's hierarchical extraction complements its flat extraction technology by providing optimized hierarchical parasitic data for high-capacity signal and power net analysis.

The hierarchical extraction technology allows designers to perform bottom-up or top-down simulations, depending on the demands of their methodology. As shown in Figure 6, hierarchical extraction improves the capacity and runtime by extracting only one instance of a block per hierarchy level while accounting for as much context specific capacitance at the cell boundary as possible. Generally, hierarchical extraction is best suited for simulation tools that can take advantage of the hierarchical data to improve runtime, or in situations where more flexibility in simulation netlist handling may be desired.

Figure 7 shows the runtime benefit of hierarchical extraction for large designs. As seen in the figure, the benefit of hierarchical extraction increases with the increase in the design size.

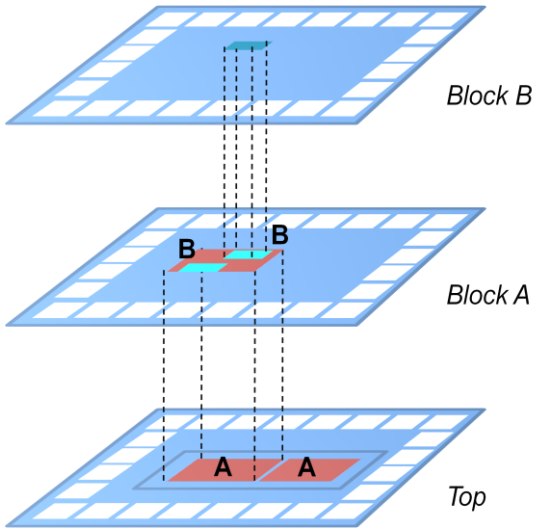

Figure 6: StarRC hierarchical parasitic extraction supports top-down or bottom-up methodology

	Design 1		Design 2	
	Hierarchical	**Flat**	**Hierarchical**	**Flat**
Extraction runtime	0.5 hr	1 hr	13 hr	Not available
Netlist size	0.9 GB	1.5 GB	7.6 GB	
Memory	751 MB	961 MB	6199 MB	
Design size	5 Million Devices		5 Billion devices	

Figure 7: StarRC hierarchical extraction enables signal and power net extraction of large designs[3]

Selective Parasitic Extraction

The selective device parasitic extraction feature of StarRC allows custom IC designers to choose and retain the critical device parasitics in their designs while ignoring less important coupling capacitances and power net parasitics. This increases simulation efficiency while meeting accuracy requirements.

At the 40-nm process technology, device parasitics such as gate-to-contact capacitance (C_{co}) and gate-to-diffusion capacitance (C_f) become context-specific (see Figure 8a), for example, they become more sensitive to the layout environment and have a pronounced impact on circuit performance. The magnitude of these capacitances is seen to increase by at least 2x compared to previous technology; therefore an accurate in-context device parasitic extraction becomes more important. In larger process nodes, these capacitances were generally included in device SPICE models, assuming pessimistic values with contact spacing at minimum and not differentiating shared source/drain diffusion. However, at advanced nodes, this pessimism must be removed and the device parasitics must be accurately extracted to achieve better silicon predictability.

Power net extraction has generally been assumed to be ideal in post-layout simulation flows, but this assumption may be inaccurate when predicting circuit behavior at smaller process nodes. To achieve signoff accuracy at smaller process nodes, designers may need to extract resistance and coupled capacitance for both power and signal nets, but this could prohibitively increase the simulation runtime. An effective alternative solution may be to simulate the design with grounded capacitance. However, due to the growing impact of context-specific device capacitances and due to the associated Miller effect, designers may prefer to selectively retain the gate-to-contact and gate-to-diffusion capacitances to ensure accuracy, but ground rest of the coupling capacitances between the interconnecting layers to improve efficiency.

Also, metal-to-diffusion contact resistance plays a major role in power network simulation at 40-nm (see Figure 8b). For example, diffusion contact resistance for a 40-nm process is of the order of tens of ohms, whereas metal sheet resistance is of the order of a few milli-ohms. Hence, power network resistance is dominated by contact resistance and the extraction tools must have the capability to accurately extract this resistance and also provide a selective extraction based on layers for productivity, if needed.

Overall, parasitic extraction tools must have the ability to selectively extract device parasitics that may dominate the circuit behavior to enable the most efficient simulation while preserving accuracy. StarRC provides an advanced feature to selectively choose device parasitic extraction based on database layers. The innovative reduction algorithms in StarRC allow designers to selectively retain device parasitics, such as diffusion resistance and gate-to-contact coupling capacitances, while treating interconnect on power nets as super conductive (ideal) and grounding other coupling capacitances—this produces the most efficient netlist for simulation. The selective extraction capability enables designers to achieve significant runtime savings as demonstrated by over 5x simulation speed-up on production designs (see Figure 9).

[3] Source: Synopsys, Inc. April 2009

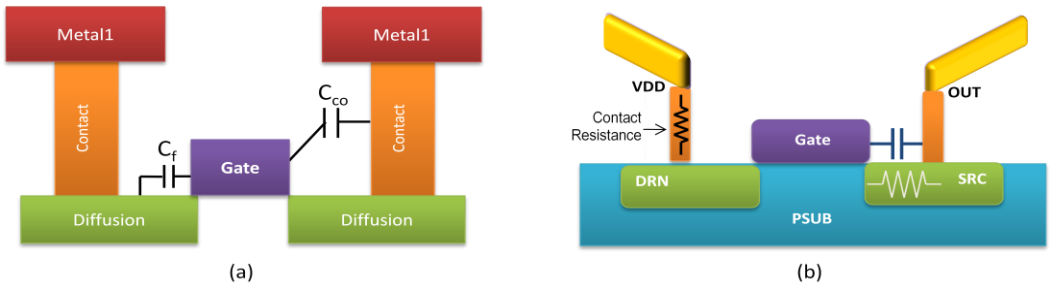

Figure 8: Context-specific device parasitics have pronounced impact on circuit performance at advanced nodes and therefore must be accurately extracted

	Full extraction	Selective device parasitic extraction	Results
Simulation runtime	152 mins	29 mins	Over 5x speed-up
Delay	12 ps	11.8 ps	~2% accuracy

Figure 9: StarRC selective device parasitic extraction offers significant runtime savings and golden accuracy[4]

Selective Parasitic Netlisting

StarRC provides flexible netlisting options to reduce the parasitic netlist size and proportionally increase simulation performance. As mentioned earlier, the simulation runtime is proportional to the number of nodes or parasitic elements in the netlist. The circuit behavior and functional requirements of the designs determine which nodes or parasitic information need to be passed to post-layout simulation tools.

StarRC's proven netlist reduction techniques allow designers to selectively filter the parasitics that may have negligible or no impact or circuit performance based on their design knowledge. It offers easy-to-use resistance and capacitance filtering as well as net filtering based on user-defined values. For instance, the user can easily reduce the number of nets in the netlist by filtering the nets based on total capacitance. The netlist reduction in StarRC preserves the total grounded and coupling capacitance, point-to-point resistance, and user-defined circuit delay to achieve the desired accuracy.

The benefits of StarRC's flexible filtering techniques to control netlist size and enhance simulation performance are evident from the results shown in Figure 10. As shown in the figure, there is a reduction in the number of elements in the parasitic netlist when the selective netlisting is switched on. This reduction enables significant simulation speed-up with no accuracy loss.

	No netlist reduction	Selective netlisting	Results
Number of elements	20125	12583	37% reduction
Simulation runtime	3009 s	1608 s	46% speed-up
Delay	1.996 ns	1.985 ns	< 0.6% change

Figure 10: Selective parasitic netlisting feature delivers significant simulation speed-up with no change in accuracy[5]

[4] Source: Synopsys, Inc. April 2009

Conclusion

As the complexity of transistor-level design continues to rise with advanced process technologies, the ability of the parasitic extraction and simulation tools to address increasing performance and capacity challenges has become a non-negotiable requirement. Designers of memory, custom digital and custom analog/mixed-signal ICs need more efficient extraction and simulation tools to address the problems of growing design sizes, new process effects, increasing parasitic count and accuracy, to effectively meet their design and project schedule challenges. Synopsys' StarRC parasitic extraction solution provides advanced process modeling and innovative techniques to boost post-layout simulation performance and capacity, while preserving signoff accuracy. StarRC, in conjunction with the Synopsys CustomSim simulation solution, delivers unmatched productivity to post-layout verification engineers while meeting their most complex technology and design requirements.

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[5] Source: Synopsys, Inc. April 2009