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WHITE PAPER

Faster and Smarter LVS for the SoC Era

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Overview

Development of a modern system-on-chip (SoC) device is a long and incredibly complex process. Design teams rely on a huge range of tools, technologies, and methodologies to get the job done. Given the ongoing advances in silicon technology and design architecture, the tools are in a constant state of evolution. Logic-versus-schematic (LVS) checking is one of those tools. This is one of the earliest automated steps in chip development, and some unfamiliar with its complexity might consider it "a solved problem." However, the reality is far different. In fact, modern SoCs pose significant challenges to traditional LVS methods, and in recent years there has been considerable innovation in LVS tools. This white paper describes some of these challenges and outlines an innovative solution that addresses them.

Challenges for Physical Verification

Today's advanced applications such as deep learning, autonomous driving vehicles, and mobility on 5G networks fuel the need for continuous advancements in IC integration. Growing design complexity, pressure on design cycle time, process advancements, and increasing verification requirements are driving the need for faster, more efficient physical verification flows. The current state-of-the-art FinFET processes at 7nm, 5nm, and 3nm are complex feats of engineering. As has been the "law" for some time, IC manufacturers can fit more and more transistors within the lithography reticle limit. Foundries utilize complicated layer stacks and deploy multi-patterning lithography on many masks. This means more and more masks are required for advanced processes.

These massive SoC designs present challenges at many steps in the development process, but advanced nodes and more masks are particularly daunting when it comes to physical verification of the layout, one of the key design steps on the critical path to chip tapeout. If physical verification is not closed on time, it almost certainly leads to schedule delays and a longer time to market (TTM). Delaying product introduction can compromise business plans or even render the chip uncompetitive in the market. Thus, on-time physical verification closure is a very important goal. This puts pressure on chip development teams, but it also means that electronic design automation (EDA) vendors need to continue to innovate on physical verification and not deem it a solved problem.

While the focus of this white paper is on LVS, it is important to understand the role that this step plays in the overall physical verification flow. Other key steps in the flow include design rule checking (DRC) and design for manufacturing (DFM). All steps must be considered as early in the chip development schedule as possible in order to avoid unpleasant surprises during full-chip signoff late in the project.

The Scope of a Solution

Shifting physical verification left in the project schedule is accomplished partly by tacking it in multiple stages. Waiting until the complete SoC has been routed before running DRC, DFM, and LVS is no longer sufficient. The development team must run physical verification seamlessly and cleanly as they proceed through the macro, intellectual property (IP), and block-level design phases. Many issues can be detected locally, within a block or subsystem, without having the context of the complete chip. Finding and fixing these issues early accelerates the physical verification process and makes future runs at higher levels of hierarchy much cleaner.

It is also not necessary or desirable to wait until the end of the project to run full-chip physical verification. As soon as the bulk of the SoC is assembled, DRC and LVS runs can begin. The physical verification process occurs in parallel with full-chip assembly. It is important that these runs be efficient so that they do not delay parallel progress on completing the design and so that the team can rapidly converge on a clean design that is ready for tapeout. Both early and final signoff runs are more efficient if physical verification can be run in parallel on more resources.

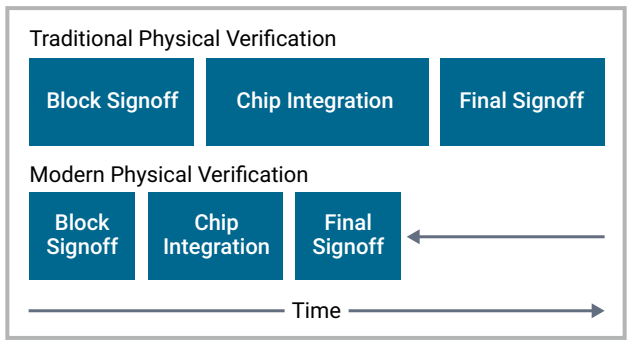

Figure 1: Accelerating SoC physical verification signoff

EDA developers tackled the challenges of SoC-era DRC before LVS, and it is instructive to see how the process evolved. Both tools must work at the macro/IP/block level and then rapidly assess the status of a full chip design and give useful and actionable feedback to fix problems. Today's large chips consist of hundreds of components, including place-and-route blocks, analog cells, memory, third-party IP, and I/O cells. While each may have been verified independently as it was designed, when complied into the full chip there are often high-level problems. These includes missing blockages, block placement errors, pad ring misalignment, and block revision control issues that must be identified and fixed. A handful of high-level issues often results in an unworkable number of low-level DRC violations. It is common for the first-time top-level run to encounter millions of DRC errors. This first "dirty" run may take multiple days on hundreds of cores to complete in a traditional DRC tool, as it brute-forces its way through detailed over-analysis. This could cause the tapeout team to waste weeks of compute time at the very end of the project.

A modern DRC solution must be able to automatically run fundamental rules from the foundry runset and apply additional methodology to rapidly assess the health of the design. If the design is relatively clean, the tool continues progressively towards completing all required DRC signoff checks. The solution must include an error heatmap for rapid and intuitive visual topological assessment of the design. Within minutes, designers can often identify the macro-problems to fix (such as overlaps), instead of getting stuck in the weeds of millions of errors. The heatmap shows hot areas (where there are many violations) in red, progressing to cool areas (with relatively few violations) in blue. Often, designers immediately recognize where errors correspond to problems with specific blocks, such as overlaps or incorrect fill.

In many ways, the trends and requirements for an SoC-era LVS solution are similar. For a large circuit design with the latest foundry technologies, it is common for LVS to run over several tens of hours or even several days. Depending on the cleanliness of the design, it is also common to entail several iterations of debugging errors, fixing the design, and rerunning LVS. Overall, this iteration is time-consuming and difficult to manage, even for a skilled designer, due to the sheer complexity of the circuit. This difficulty of running LVS, debugging, and iterating is often the root cause of unwanted schedule slip during the final phases of the chip project.

This iteration is generally worse when LVS runs over the layout that merges all the design components for the first time because there are many possible new issues that can only be found after the merge. These include:

- Macro/IP issues
  - Out of sync with shared library version
  - Out of sync with layer stack
  - Ports off the routing grid
  - Port shapes not compatible with design rules
  - Dummy fill shapes out of boundary horizontally or vertically
  - Macro/IP size not as planned
  - Macro/IP not DRC-clean
- Integration errors in the top hierarchical design
- Interface pin alignment errors
- Top-level shorts
- Design components developed with different technology or library
- Shortcuts due to signoff team under pressure

The fixes for those errors may not be necessarily hard to find once LVS has finished running, but those errors make LVS runtime longer and machine requirements greater, preventing designers from swiftly iterating the debugging/fixing/rerunning of their design.

These challenges can be addressed by an LVS solution that is faster and smarter than traditional tools, improving productivity, performance, and debugging. It must be aware of what is the most critical for design signoff, providing a fast and automated way to find root causes for issues found in early full-chip LVS runs. By swiftly detecting design issues that would have made traditional LVS slower and more time-consuming, the turnaround time for each run is reduced dramatically. This enables more frequent and shorter iterations of the running/debugging/fixing design cycle and will eventually lead to an earlier signoff than possible with previous-generation tools.

The Solution from Synopsys

When it comes to physical verification, Synopsys meets all the requirements outlined in the previous sections, and more, for modern SoC designs. Synopsys IC Validator™ physical verification is a comprehensive and high-performance signoff solution that improves productivity for customers at all process nodes, from mature to advanced. Its performance and scalability have enabled some of the industry's largest reticle limit chips with billions of transistors. IC Validator's Explorer technology is an innovative approach and the industry's first solution to accelerate verification during full-chip integration.

Synopsys introduced Explorer DRC technology in 2018 to bring same-day design rule checking to development teams and to isolate key design weaknesses within hours during SoC integration. Its unrivalled performance brings a dramatic change in compute efficiency on dirty designs versus the traditional DRC flow: five times faster runtime with five times fewer cores used. In practice, this means that typical full-chip 5nm designs can be run in several hours with 16 or 32 cores, even when dirty. This enables tapeout engineers to do an overnight run to detect fundamental design problems and begin fixing them immediately.

Explorer LVS technology, introduced in 2019, is the industry's first modern LVS solution for the SoC era. Explorer LVS can be used anytime during signoff preparation whenever the top hierarchical design integrity needs to be checked. However, its maximum benefit and performance can be achieved when running right after full chip integration is done for the first time. That is when the most unexpected results are coming out, traditionally producing long and tedious LVS running/debugging/fixing/rerunning iteration, and often creating tons of error and log files. With Explorer LVS, any critical issues can be detected in a fast and efficient manner so that signoff engineers can make progress without all the inefficiencies of a traditional LVS tool.

Although Explorer LVS's main design target is a full-chip layout for signoff, it can apply to any design regardless of size or complexity. The larger and the more complex the design is, the better the performance over previous-generation tools. Explorer LVS consists of three different stages, as shown in Figure 2.

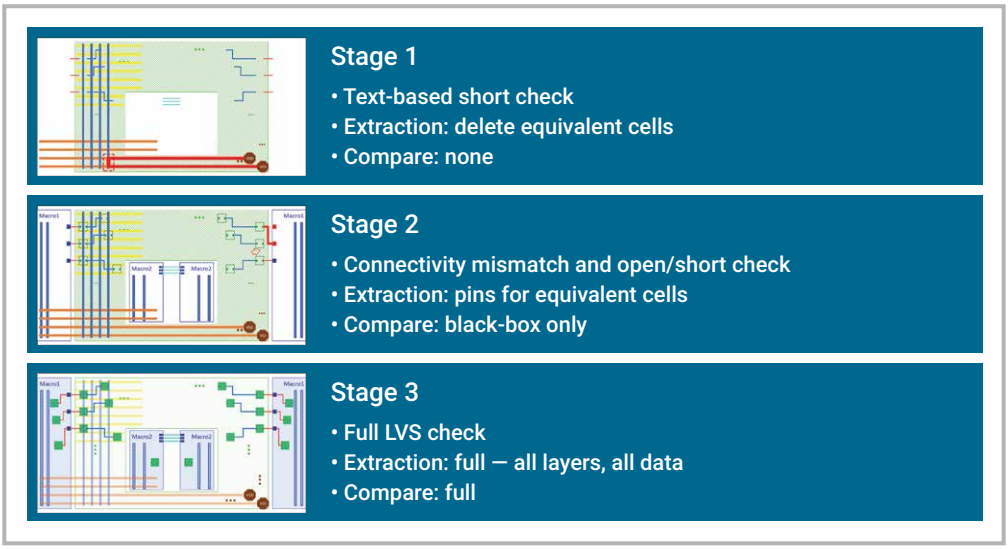

Figure 2: Stages of Explorer LVS checking

Once Explorer LVS executes on a design, it produces a summary file to give engineers an overall idea of what is going on with the design. They can use the summary file to check the overall quality of a full-chip design in terms of signoff preparedness. Each individual error can be checked and debugged from either the text format log file or an interactive tool. For debugging of shorts in the design, Explorer LVS results can be immediately loaded into IC Validator ShortFinder for quick and easy GUI-based interactive debugging, as shown in Figure 3. Similarly, Explorer LVS connectivity errors can be interactively debugged within IC Validator VUE. Debugging of issues found by Explorer LVS uses all the proven visual methods developed for full LVS.

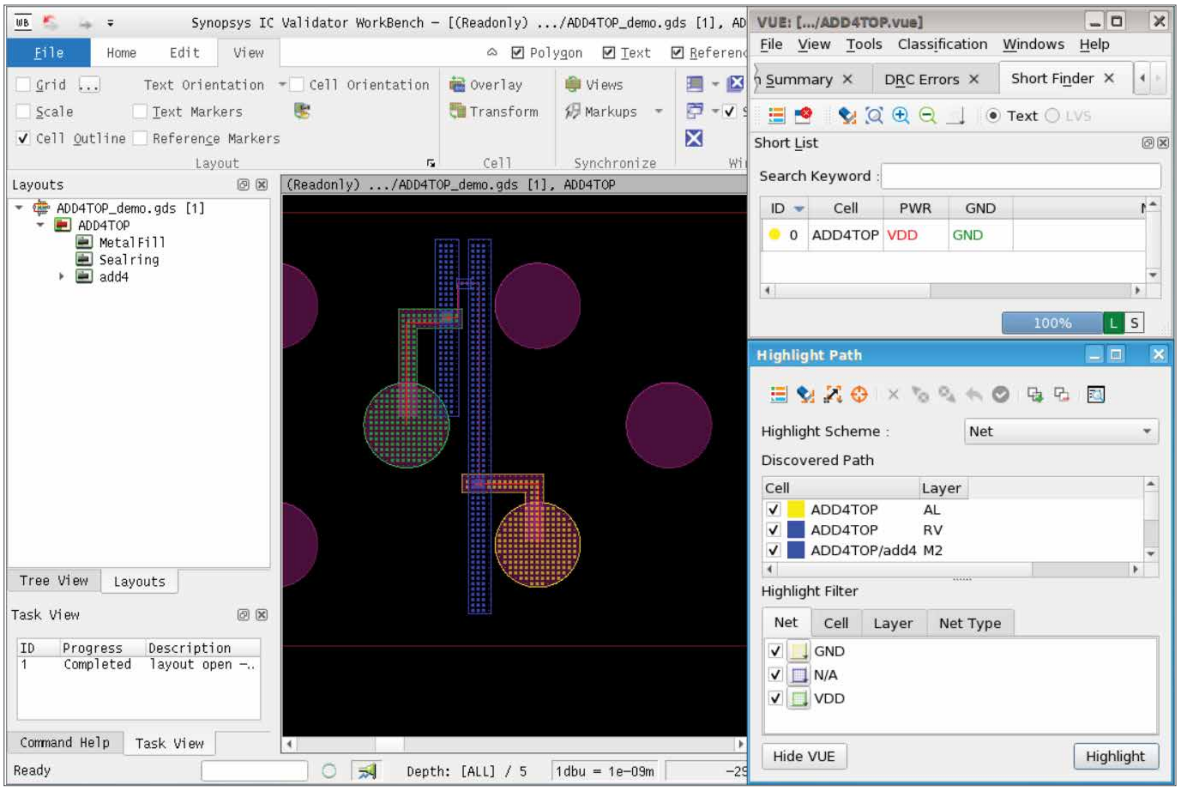

Figure 3: Debugging a design short in Explorer LVS

Explorer LVS is fully complementary with full LVS. In a typical flow, full LVS might be run on blocks/macros/IP after floorplanning and place-and-route to detect issues early in the project. As soon as the pieces are assembled into a full chip, Explorer LVS provides short runtime and intuitive debug to clean up the design as much as possible before final signoff with full LVS. If engineering change orders (ECOs) or last-minute macro/IP updates happen before signoff, Explorer LVS ensures that the integrity of the design has not been compromised. The results are very impressive. As shown in in Figure 4, on actual customer designs in production use, Explorer LVS runs up to 30X faster and consumes up to 30X less memory usage compared to full LVS.

Customer Design	Explorer LVS Runtime	Speedup over Full LVS	Memory Savings over Full LVS
7nm	3 hours	12X	3X
7nm	0.5 hours	11X	57X
16nm	0.67 hours	25X	18X
16nm	0.57 hours	29X	10X
14nm	0.25 hours	30X	30X

Figure 4: Real-world performance results of Explorer LVS

Conclusion

Modern SoC devices present many challenges to design and verification flows, and to the EDA tools that execute the many steps through the process. Physical verification, and LVS in particular, has required a major upgrade in capabilities. Synopsys has stepped up the plate to provide a fast and automated way to find root causes of early full-chip LVS issues. By swiftly detecting design problems, Explorer LVS delivers up to 30X faster turnaround time, enabling more frequent and shorter iterations. Proven with successful deployment and signoffs on numerous customer designs, Explorer LVS provides innovation and real change to the physical verification flow. SoC designers can tape out earlier with full confidence that all LVS issues have been detected and fixed.

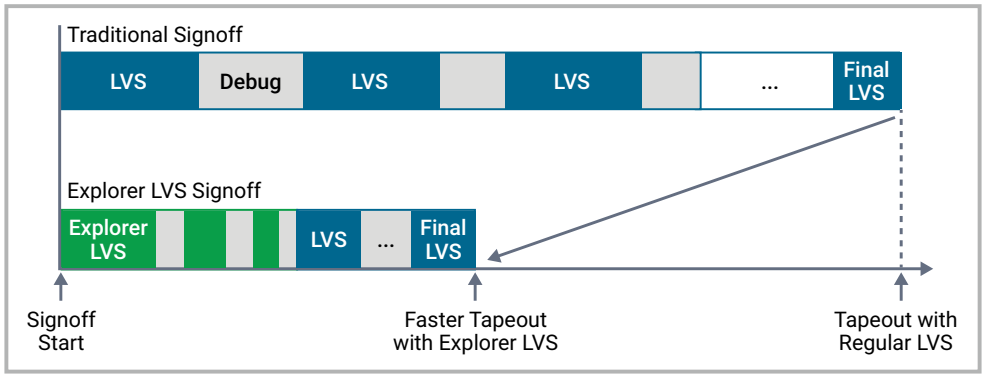

Figure 5: Accelerated tapeout schedule with Explorer LVS

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