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DFTMAX Ultra

New Technology to Address Key Test Challenges

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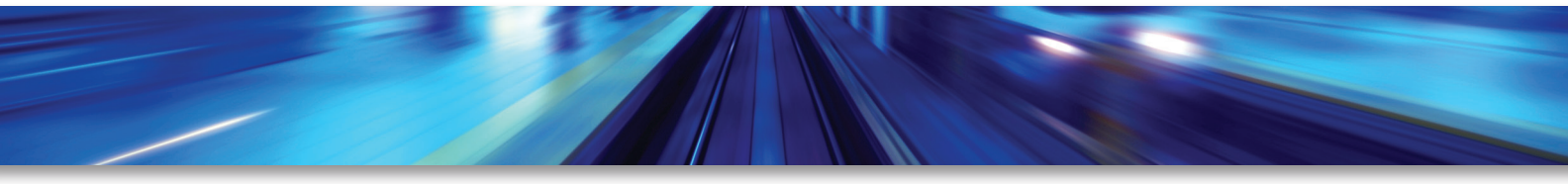

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Introduction

For most design-for-test (DFT) and test engineers, achieving very high defect coverage with minimal design impact and low manufacturing test cost are fundamental objectives. Almost all of today's large digital designs require scan compression to meet these goals. This paper explains how DFTMAX™ Ultra delivers new scan compression technology that further reduces test cost and simplifies design impact, providing improvements in test quality.

Achieving High Test Quality

Advanced manufacturing process nodes introduce new types of defects that require additional test patterns to detect. There are several reasons why additional test patterns are needed, and why higher levels of scan compression are required to manage test cost. First, the test coverage of traditional fault models, such as stuck-at and transition faults, needs to increase. Even a 1% increase in test coverage for these fault models can sometimes double the number of patterns generated. ATPG coverage versus pattern count is an asymptotic function because each additional pattern detects fewer and fewer previously undetected faults.

Second, new fault models need to be included in the test generation flow to detect defect types that are not sufficiently covered by the established fault models already mentioned: bridging and dynamic bridging faults for metal shorts, internal cell faults for complex library cells, and slack-based transition faults for small delay defects. These new fault models are more difficult to sensitize, meaning the number of detections per pattern will be lower. Thus, achieving even nominal coverage of these new fault models requires a significant increase in the total number of test patterns.

Delivering Higher Compression and Faster Shift Speeds

DFTMAX Ultra uses a new compression architecture to reduce total scan test data and test time by 2-3X over existing compression technologies. DFTMAX Ultra also achieves higher compression when fewer chip pins or tester channels are available for manufacturing test. The architecture uses streaming, bidirectional compressors and decompressors (CODECs) for the scan input and scan output data. This new CODEC design allows both very efficient test generation that maximizes the number of faults detected per pattern, as well as independent control over unknown values that typically degrade compression efficiency. Figure 1 shows a high-level view of the new architecture.

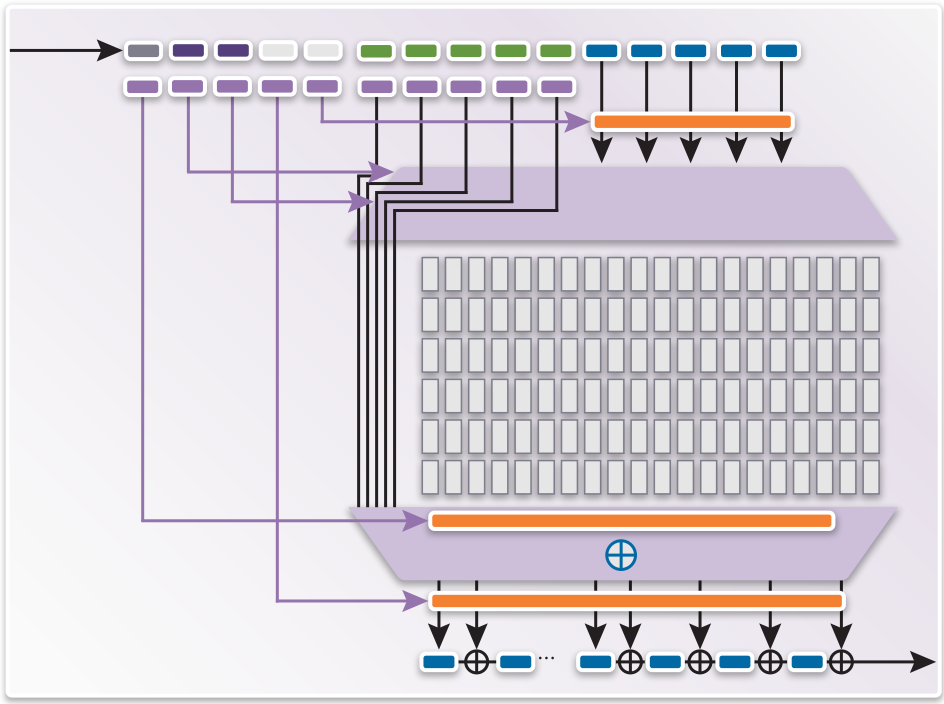

Figure 1: DFTMAX Ultra compression architecture

Other existing compression architectures typically rely on either serialization and de-serialization registers or linear feedback shift registers to achieve good compression on designs with a limited number of test pins. However, these techniques either reduce scan data bandwidth or increase the number of scan patterns. DFTMAX Ultra streams and decompresses/compresses scan data at the same time, which maximizes the efficiency of each test cycle. Figure 2 shows that DFTMAX Ultra achieves 100X or more compression on a range of customer designs.

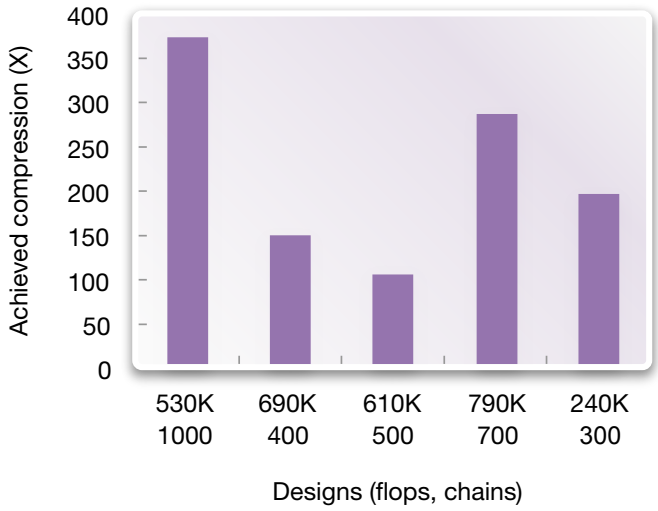

Figure 2: Greater than 100X compression on many designs

Using compression to reduce the number of scan test cycles is one factor in reducing overall test time. Another factor is reducing the time for each test cycle. The DFMTAX Ultra compression architecture shown in Figure 1 is highly pipelined to minimize per-cycle timing delays from the chip pins, through the CODECs, and to the scan chains. To maximize scan shift frequency, multicycle paths are used on all signals that might require significant routing length. These optimizations mean that scan shift speeds are limited by external factors, such as timing and power limitations of the tester or the device under test, rather than by the scan compression logic. A higher scan shift frequency provides additional and significant test cost reductions.

Reducing Test Cost with Multisite Testing and Fewer Test Pins

The widespread use of multisite testing has shifted the requirements for scan compression. Compared to using all available tester channels on a single die, testing multiple dies in parallel has proven to be a more effective and predictable method for reducing manufacturing test cost. This is because the former method relies on a large number of available chip pins and very wide CODEC configurations (with more routing congestion) to achieve the same total cost reduction.

Several important trends are reducing the number of chip pins available for test. Smaller form factors and tighter packaging for today's mobile electronics mean that the total number of pins is shrinking relative to the increase in device gate counts. And, more analog functions are being integrated into many of these designs, further reducing the number of digital chip pins available for scan test.

DFTMAX Ultra is specifically optimized to provide high compression even on designs with one scan input and one scan output per CODEC. Because the achieved compression is dependent only on the ratio of internal scan chains and not on the number of test pins, designers and DFT engineers have less uncertainty and greater freedom in defining scan compression partitions and implementing the resulting chain configurations. Figure 3 shows that the achieved compression remains nearly constant with different configurations of a 50:1 internal scan chain to test pin ratio.

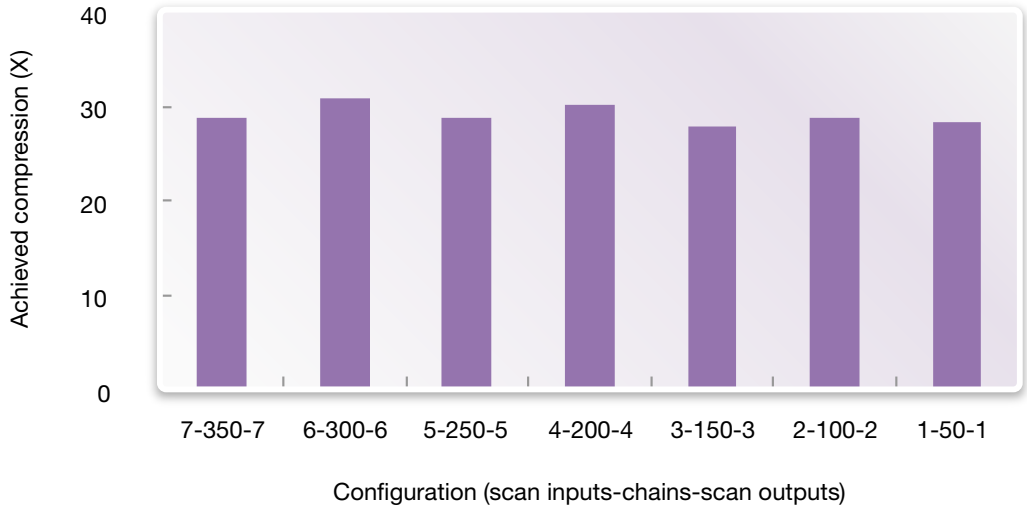

Figure 3: Predictable compression with different configurations

Simplified DFT Implementation on Large SoC Designs

Today's largest designs contain tens or even hundreds of cores, each with potentially independent clock and/or power domains. For such designs, top-level integration becomes particularly cumbersome and unpredictable. DFTMAX Ultra greatly simplifies the task of top-level DFT integration. Foremost, the flexibility of this new architecture enables each core to have one or more dedicated CODEC, regardless of the size of the core. This means that all of the scan compression logic for a core is fully contained within that core, and that CODECs do not need to be shared across multiple cores.

Just like traditional scan, DFTMAX Ultra uses a single clock for shifting tester scan data, CODEC pipelines, and internal scan chains. Thus, no additional clock generation or clock gating is required within each core, and more importantly, at the top level. Also like traditional scan, this architecture uses a single scan-enable signal for CODECs and scan chains. This simplifies DFT connections between each core and the top-level test control module.

Because all CODECs can be fully contained within a single core, there is no dependency on completion of other cores or top-level logic for each core's DFT closure. The result is that ATPG and timing closure (including all test modes) can be run on each core as soon as it is completed.

Conclusion

DFTMAX Ultra delivers significant new technology to simplify DFT implementation and reduce manufacturing test cost in the face of increasing design sizes and test quality requirements. This technology builds on the strengths of the Synopsys synthesis-based test platform and is easily deployed in the industry's most common design flows. For customers already using DFTMAX, DFTMAX Ultra requires only incremental changes to existing DFT synthesis scripts. Lastly, TetraMAX ATPG is fully optimized for both test pattern generation and failure diagnostics for DFTMAX Ultra designs.

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